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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	6KB (6K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj06gs102-e-sp">https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj06gs102-e-sp</a>

# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

FIGURE 2-6: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER

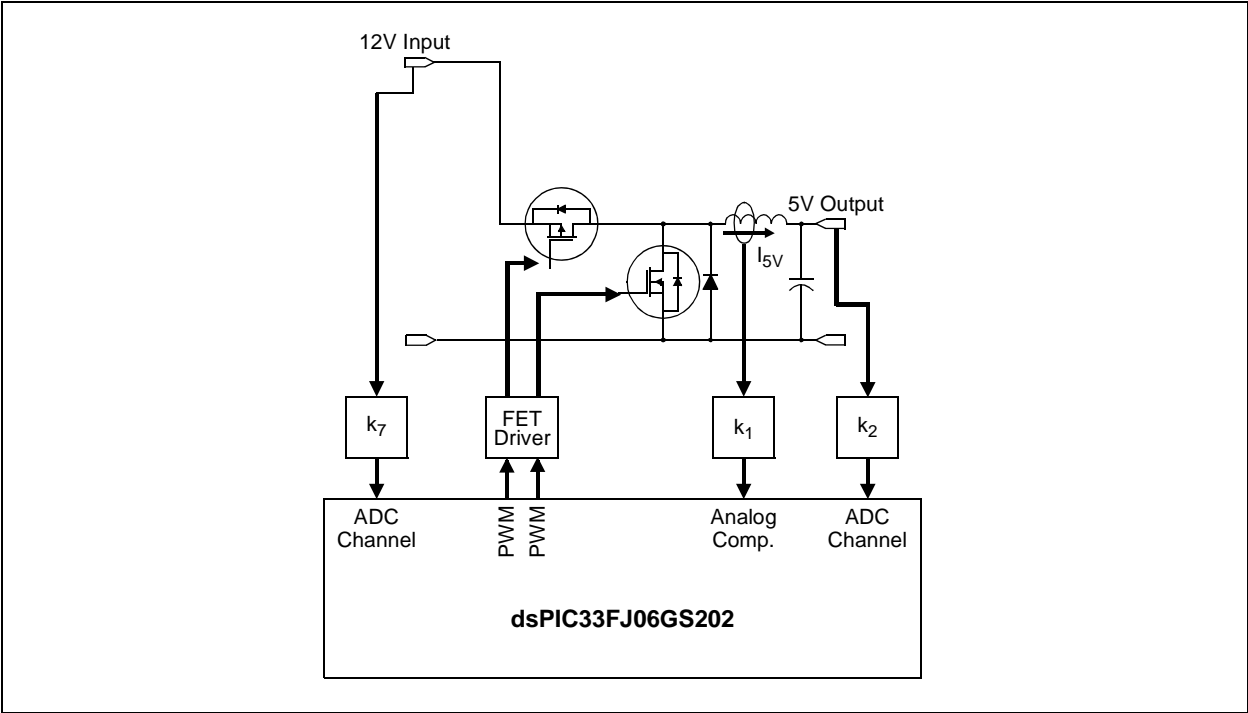
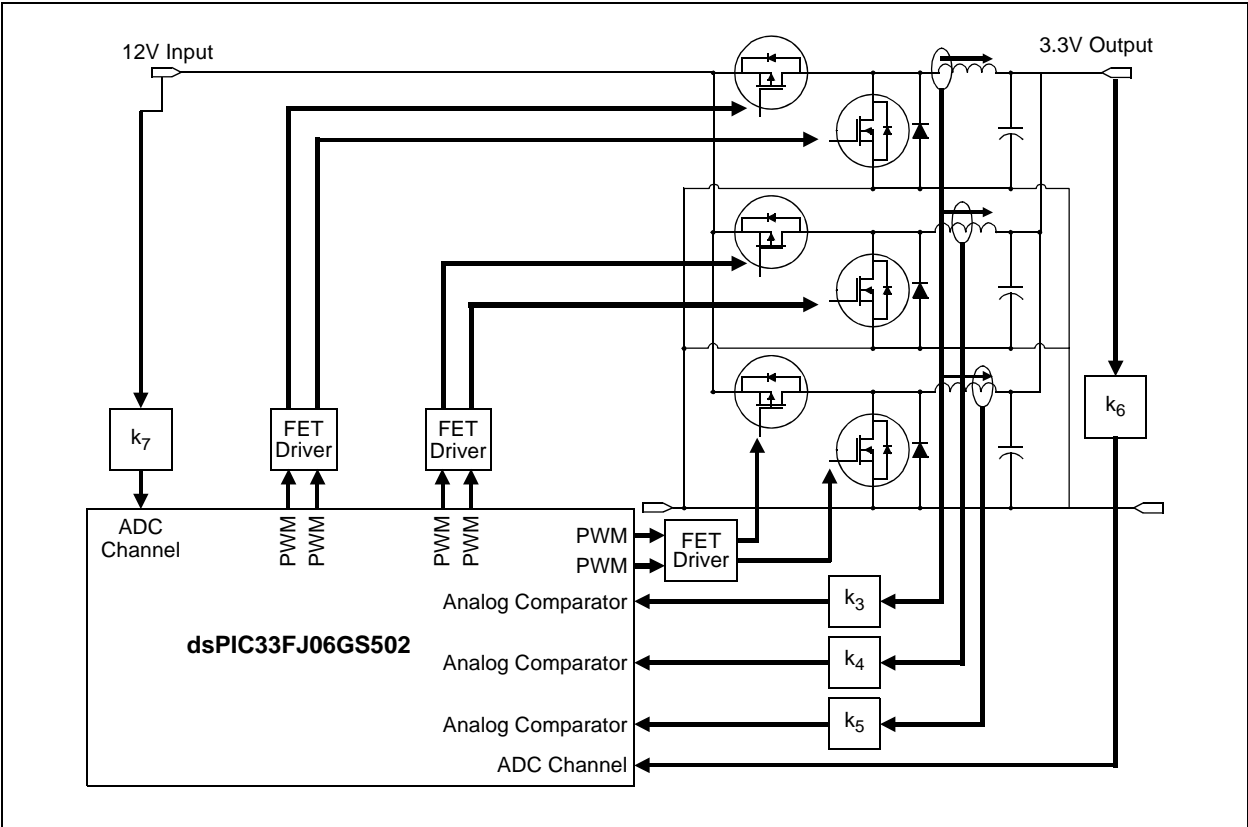


FIGURE 2-7: MULTI-PHASE SYNCHRONOUS BUCK CONVERTER



**TABLE 4-22: I2C1 REGISTER MAP**

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	0200	—	—	—	—	—	—	—	—	I2C1 Receive Register								0000
I2C1TRN	0202	—	—	—	—	—	—	—	—	I2C1 Transmit Register								00FF
I2C1BRG	0204	—	—	—	—	—	—	—	Baud Rate Generator Register									0000
I2C1CON	0206	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1STAT	0208	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
I2C1ADD	020A	—	—	—	—	—	—	I2C1 Address Register										0000
I2C1MSK	020C	—	—	—	—	—	—	AMSK<9:0>										0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-23: UART1 REGISTER MAP**

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART1 Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	0228	Baud Rate Generator Prescaler																0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-24: SPI1 REGISTER MAP**

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	—	—	—	—	SPIROV	—	—	—	—	SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	—	0000
SPI1BUF	0248	SPI1 Transmit and Receive Buffer Register																0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## 4.6.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program space without going through data space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit wide word address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

- TBLRDL (Table Read Low):
  - In Word mode, this instruction maps the lower word of the program space location ( $P<15:0>$ ) to a data address ( $D<15:0>$ ).

- In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when byte select is '1'; the lower byte is selected when it is '0'.

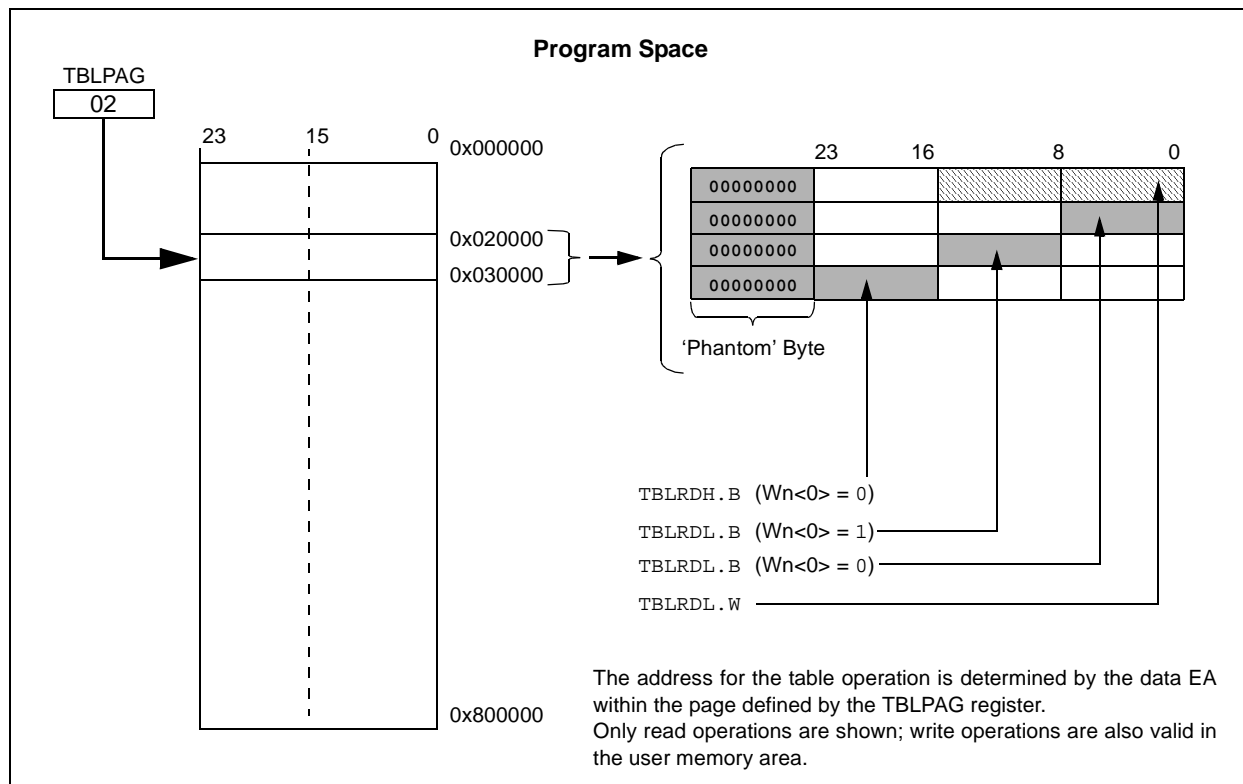
- TBLRDH (Table Read High):

- In Word mode, this instruction maps the entire upper word of a program address ( $P<23:16>$ ) to a data address. Note that  $D<15:8>$ , the 'phantom byte', will always be '0'.
- In Byte mode, this instruction maps the upper or lower byte of the program word to  $D<7:0>$  of the data address, in the TBLRDL instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

Similarly, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When  $TBLPAG<7> = 0$ , the table page is located in the user memory space. When  $TBLPAG<7> = 1$ , the page is located in configuration space.

**FIGURE 4-10: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS**



# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

## 5.0 FLASH PROGRAM MEMORY

**Note 1:** This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “Flash Programming” (DS70191) in the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Run-Time Self-Programming (RTSP)

ICSP allows a dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx, and three other lines for

power (VDD), ground (VSS) and Master Clear ( $\overline{\text{MCLR}}$ ). This allows customers to manufacture boards with unprogrammed devices and then program the Digital Signal Controller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data, either in blocks or ‘rows’ of 64 instructions (192 bytes) at a time, or a single program memory word, and erase program memory in blocks or ‘pages’ of 512 instructions (1536 bytes) at a time.

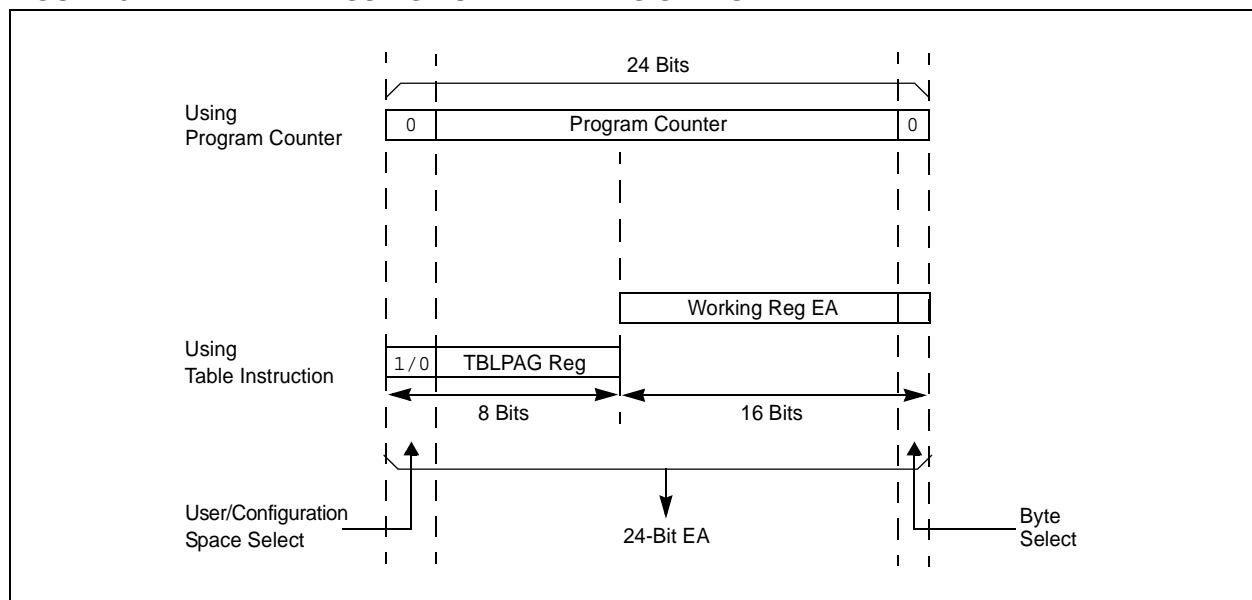
### 5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

**FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS**



# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

## REGISTER 15-18: LEBCONx: LEADING-EDGE BLANKING CONTROL REGISTER<sup>(1)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	LEB6	LEB5
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
LEB4	LEB3	LEB2	LEB1	LEB0	—	—	—
bit 7						bit 0	

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15      **PHR:** PWMxH Rising Edge Trigger Enable bit  
1 = Rising edge of PWMxH will trigger the LEB counter  
0 = LEB ignores the rising edge of PWMxH
- bit 14      **PHF:** PWMH Falling Edge Trigger Enable bit  
1 = Falling edge of PWMxH will trigger the LEB counter  
0 = LEB ignores the falling edge of PWMxH
- bit 13      **PLR:** PWML Rising Edge Trigger Enable bit  
1 = Rising edge of PWMxL will trigger the LEB counter  
0 = LEB ignores the rising edge of PWMxL
- bit 12      **PLF:** PWML Falling Edge Trigger Enable bit  
1 = Falling edge of PWMxL will trigger the LEB counter  
0 = LEB ignores the falling edge of PWMxL
- bit 11      **FLTLEBEN:** Fault Input LEB Enable bit  
1 = Leading-Edge Blanking is applied to selected Fault input  
0 = Leading-Edge Blanking is not applied to selected Fault input
- bit 10      **CLLEBEN:** Current-Limit LEB Enable bit  
1 = Leading-Edge Blanking is applied to selected current-limit input  
0 = Leading-Edge Blanking is not applied to selected current-limit input
- bit 9-3      **LEB<6:0>:** Leading-Edge Blanking for Current-Limit and Fault Inputs bits  
The value is 8.32 nsec increments.
- bit 2-0      **Unimplemented:** Read as '0'

**Note 1:** Configure this register in word format.

# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

**REGISTER 17-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER**

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	AMSK<9:8>	
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AMSK<7:0>							
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10

**Unimplemented:** Read as '0'

bit 9-0

**AMSK<9:0>:** Mask for Address bit x Select bits

1 = Enables masking for bit x of incoming message address; bit match is not required in this position

0 = Disables masking for bit x; bit match is required in this position

# **dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04**

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NOTES:

## 19.0 HIGH-SPEED 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

**Note 1:** This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **“High-Speed 10-Bit Analog-to-Digital Converter (ADC)”** (DS70000321) in the *“dsPIC33/PIC24 Family Reference Manual”*, which is available on the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices provide high-speed, successive approximation Analog-to-Digital conversions to support applications, such as AC/DC and DC/DC power converters.

### 19.1 Features Overview

The ADC module comprises the following features:

- 10-bit resolution
- Unipolar inputs
- Up to two Successive Approximation Registers (SARs)
- Up to 12 external input channels
- Up to two internal analog inputs
- Dedicated result register for each analog input
- $\pm 1$  LSB accuracy at 3.3V
- Single supply operation
- 4 Msps conversion rate at 3.3V (devices with two SARs)
- 2 Msps conversion rate at 3.3V (devices with one SAR)
- Low-power CMOS technology

### 19.2 Module Description

This ADC module is designed for applications that require low latency between the request for conversion and the resultant output data. Typical applications include:

- AC/DC power supplies
- DC/DC Converters
- Power Factor Correction (PFC)

This ADC works with the high-speed PWM module in power control applications that require high-frequency control loops. This module can sample and convert two analog inputs in a 0.5 microsecond when two SARs are used. This small conversion delay reduces the “phase lag” between measurement and control system response.

Up to five inputs may be sampled at a time (four inputs from the dedicated Sample-and-Hold circuits and one from the shared Sample-and-Hold circuit). If multiple inputs request conversion, the ADC will convert them in a sequential manner, starting with the lowest order input.

This ADC design provides each pair of analog inputs (AN1, AN0), (AN3, AN2), ..., the ability to specify its own trigger source out of a maximum of sixteen different trigger sources. This capability allows this ADC to sample and convert analog inputs that are associated with PWM generators operating on Independent Time Bases (ITBs).

The user application typically requires synchronization between analog data sampling and PWM output to the application circuit. The very high-speed operation of this ADC module allows “data on demand”.

In addition, several hardware features have been added to the peripheral interface to improve real-time performance in a typical DSP-based application.

- Result alignment options
- Automated sampling
- External conversion start control
- Two internal inputs to monitor the INTREF internal reference and the EXTREF input signal

### 19.3 Module Functionality

The high-speed, 10-bit ADC module is designed to support power conversion applications when used with the high-speed PWM module. The ADC may have one or two SAR modules, depending on the device variant. If two SARs are present on a device, two conversions can be processed at a time, yielding 4 Msps conversion rate. If only one SAR is present on a device, only one conversion can be processed at a time, yielding 2 Msps conversion rate. The high-speed 10-bit ADC produces two 10-bit conversion results in a 0.5 microsecond.

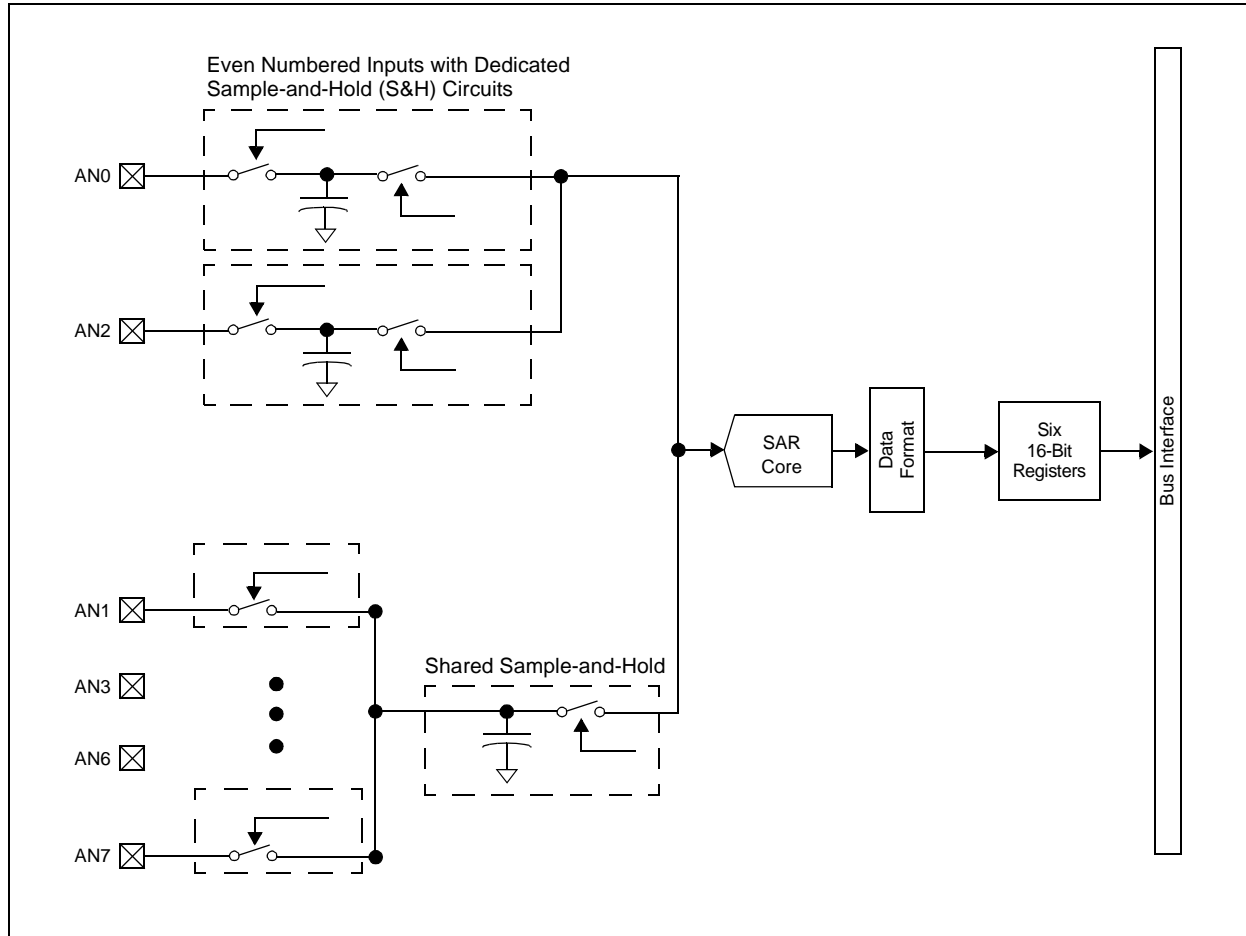
The ADC module supports up to 12 external analog inputs and two internal analog inputs. To monitor reference voltage, two internal inputs, AN12 and AN13, are connected to the EXTREF and INTREF voltages, respectively.

The analog reference voltage is defined as the device supply voltage (AVDD/AVSS).

Block diagrams of the ADC module are shown in Figure 19-1 through Figure 19-6.

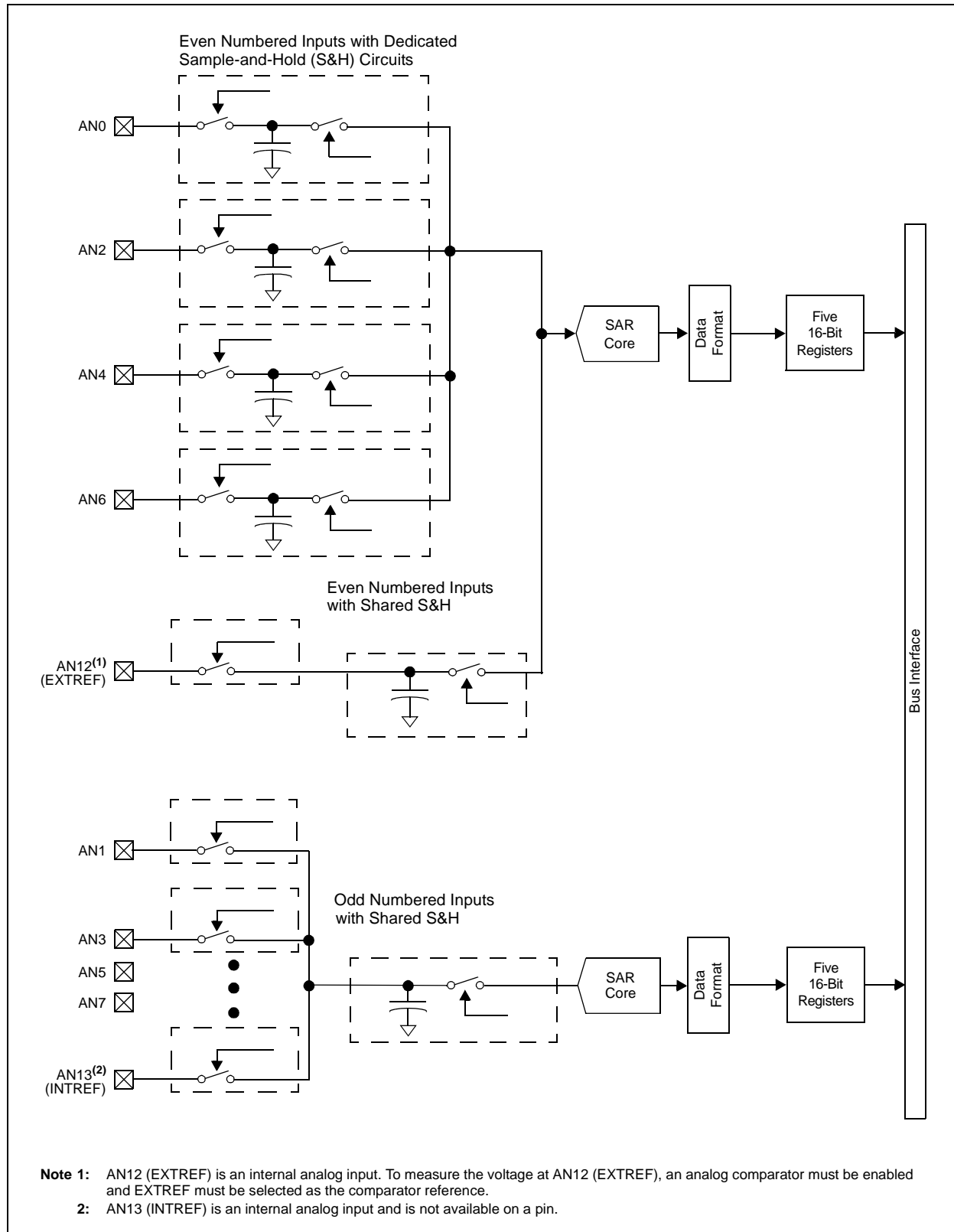
# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

FIGURE 19-1: ADC BLOCK DIAGRAM FOR dsPIC33FJ06GS101 DEVICES WITH ONE SAR



# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

**FIGURE 19-5: ADC BLOCK DIAGRAM FOR dsPIC33FJ16GS502 DEVICES WITH TWO SARs**



# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

## REGISTER 19-3: ADBASE: ANALOG-TO-DIGITAL BASE REGISTER<sup>(1,2)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADBASE<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
ADBASE<7:1>							—
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-1 **ADBASE<15:1>**: Analog-to-Digital Base bits

This register contains the base address of the user's ADC Interrupt Service Routine jump table. This register, when read, contains the sum of the ADBASE register contents and the encoded value of the PxRDY status bits.

The encoder logic provides the bit number of the highest priority PxRDY bits, where P0RDY is the highest priority and P6RDY is the lowest priority.

bit 0 **Unimplemented**: Read as '0'

**Note 1:** The encoding results are shifted left two bits, so bits 1-0 of the result are always zero.

**Note 2:** As an alternative to using the ADBASE register, the ADCP0-6 ADC Pair Conversion Complete interrupts can be used to invoke A to D conversion completion routines for individual ADC input pairs.

## REGISTER 19-4: ADPCFG: ANALOG-TO-DIGITAL PORT CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	PCFG<11:8> <sup>(1)</sup>			
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG<7:0> <sup>(1)</sup>							
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **Unimplemented**: Read as '0'

bit 11-0 **PCFG<11:0>**: Analog-to-Digital Port Configuration Control bits<sup>(1)</sup>

1 = Port pin in Digital mode; port read input is enabled, Analog-to-Digital input multiplexer is connected to AVSS

0 = Port pin in Analog mode; port read input is disabled, Analog-to-Digital samples the pin voltage

**Note 1:** Not all PCFGx bits are available on all devices. See Figure 19-1 through Figure 19-6 for the available analog pins (PCFGx = ANx, where x = 0-11).

# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

## 21.4 Watchdog Timer (WDT)

For the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

### 21.4.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a nominal WDT time-out period (TWDT) of 1 ms in 5-bit mode, or 4 ms in 7-bit mode.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>) which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSC<2:0> bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

**Note:** The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

### 21.4.2 SLEEP AND IDLE MODES

If the WDT is enabled, it will continue to run during Sleep or Idle modes. When the WDT time-out occurs, the device will wake the device and code execution will continue from where the PWRSAV instruction was executed. The corresponding SLEEP bit (RCON<3>) or IDLE bit (RCON<2>) will need to be cleared in software after the device wakes up.

### 21.4.3 ENABLING WDT

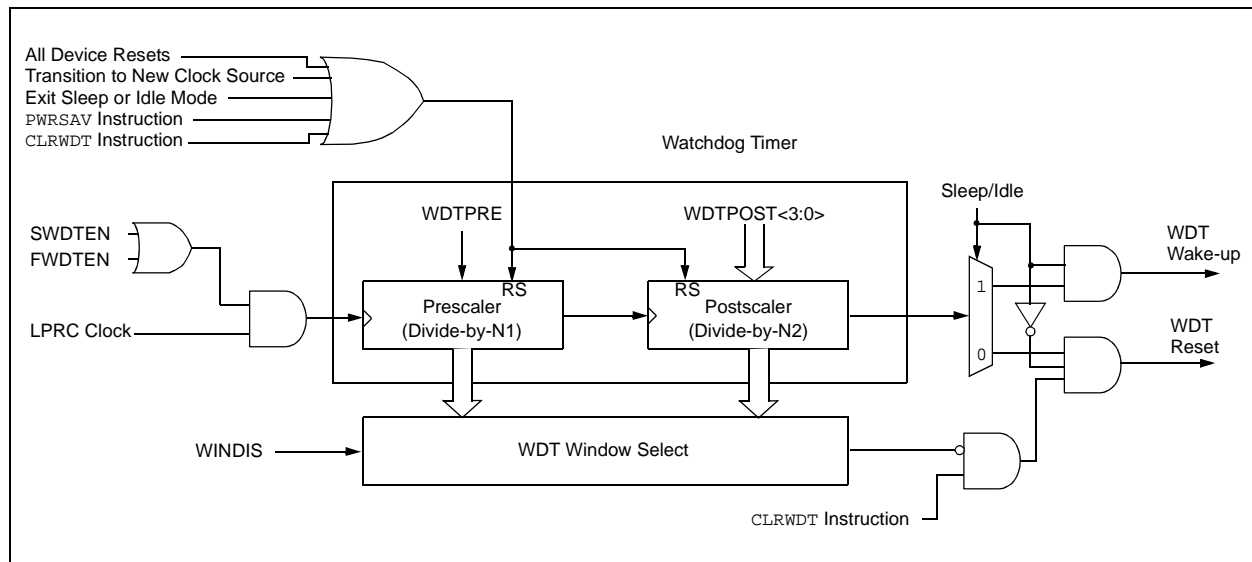
The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register. When the FWDTEN Configuration bit is set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

**Note:** If the WINDIS bit (FWDT<6>) is cleared, the CLRWDT instruction should be executed by the application software only during the last 1/4 of the WDT period. This CLRWDT window can be determined by using a timer. If a CLRWDT instruction is executed before this window, a WDT Reset occurs.

The WDT flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

FIGURE 21-2: WDT BLOCK DIAGRAM



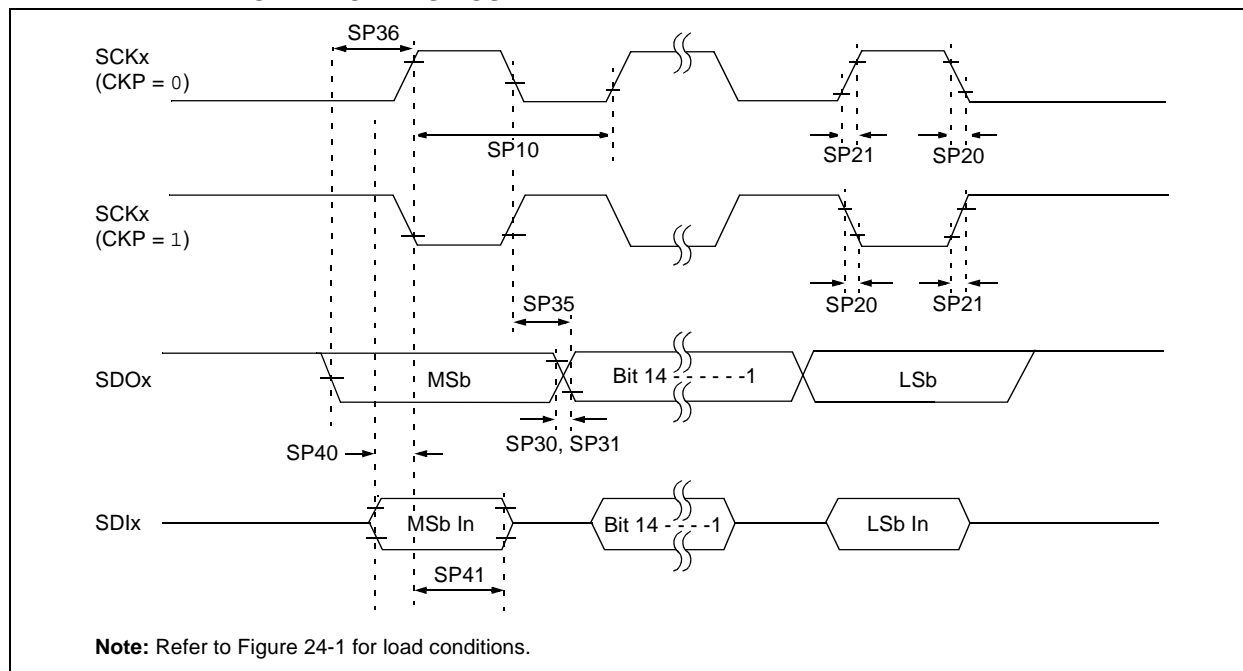
# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

**TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
29	DIV	DIV.S Wm, Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD Wm, Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U Wm, Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD Wm, Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF Wm, Wn	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO #lit14, Expr	Do code to PC + Expr, lit14 + 1 times	2	2	None
		DO Wn, Expr	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED Wm*Wm, Acc, Wx, Wy, Wxd	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB,SA,SB,SAB
33	EDAC	EDAC Wm*Wm, Acc, Wx, Wy, Wxd	Euclidean Distance	1	1	OA,OB,OAB,SA,SB,SAB
34	EXCH	EXCH Wns, Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL Ws, Wnd	Find Bit Change from Left (MSb) Side	1	1	C
36	FF1L	FF1L Ws, Wnd	Find First One from Left (MSb) Side	1	1	C
37	FF1R	FF1R Ws, Wnd	Find First One from Right (LSb) Side	1	1	C
38	GOTO	GOTO Expr	Go to Address	2	2	None
		GOTO Wn	Go to Indirect	1	2	None
39	INC	INC f	f = f + 1	1	1	C,DC,N,OV,Z
		INC f, WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC Ws, Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
40	INC2	INC2 f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2 f, WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2 Ws, Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
41	IOR	IOR f	f = f .IOR. WREG	1	1	N,Z
		IOR f, WREG	WREG = f .IOR. WREG	1	1	N,Z
		IOR #lit10, Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR Wb, Ws, Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR Wb, #lit5, Wd	Wd = Wb .IOR. lit5	1	1	N,Z
42	LAC	LAC Wso, #Slit4, Acc	Load Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
43	LNK	LNK #lit14	Link Frame Pointer	1	1	None
44	LSR	LSR f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR f, WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR Ws, Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR Wb, Wns, Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR Wb, #lit5, Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
45	MAC	MAC Wm*Wn, Acc, Wx, Wxd, Wy, Wyd, AWB	Multiply and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
		MAC Wm*Wm, Acc, Wx, Wxd, Wy, Wyd	Square and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
46	MOV	MOV f, Wn	Move f to Wn	1	1	None
		MOV f	Move f to f	1	1	N,Z
		MOV f, WREG	Move f to WREG	1	1	None
		MOV #lit16, Wn	Move 16-bit Literal to Wn	1	1	None
		MOV.b #lit8, Wn	Move 8-bit Literal to Wn	1	1	None
		MOV Wn, f	Move Wn to f	1	1	None
		MOV Wso, Wdo	Move Ws to Wd	1	1	None
		MOV WREG, f	Move WREG to f	1	1	None
		MOV.D Wns, Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D Ws, Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
47	MOVSAC	MOVSAC Acc, Wx, Wxd, Wy, Wyd, AWB	Prefetch and Store Accumulator	1	1	None

# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

**FIGURE 24-13: SPIx MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS**



**TABLE 24-32: SPIx MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Units	Conditions
SP10	TscP	Maximum SCKx Frequency	—	—	9	MHz	See <b>Note 3</b>
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32 and <b>Note 4</b>
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31 and <b>Note 4</b>
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and <b>Note 4</b>
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and <b>Note 4</b>
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2sch, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 111 ns. The clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

**TABLE 24-37: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Units	Conditions
SP70	TscP	Maximum SCKx Input Frequency	—	—	11	MHz	See <b>Note 3</b>
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and <b>Note 4</b>
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 and <b>Note 4</b>
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and <b>Note 4</b>
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and <b>Note 4</b>
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx $\uparrow$ or SCKx Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx} \uparrow$ to SDOx Output High-Impedance	10	—	50	ns	See <b>Note 4</b>
SP52	Tsch2ssH, TscL2ssH	$\overline{SSx}$ after SCKx Edge	1.5 TCY + 40	—	—	ns	See <b>Note 4</b>

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the Master must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

# **dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04**

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NOTES:

# **dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04**

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NOTES:

# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

## INDEX

### A

AC Characteristics .....	300, 338, 345
Internal FRC Accuracy .....	303
Internal LPRC Accuracy .....	303
Load Conditions .....	300, 338
ADC .....	
Control Registers .....	246
Functionality .....	239
Arithmetic Logic Unit (ALU) .....	38
Assembler .....	
MPASM Assembler .....	284
Auxiliary Clock Generation .....	138

### B

Barrel Shifter .....	42
Bit-Reversed Addressing .....	76
Example .....	77
Implementation .....	76
Sequence Table (16-Entry) .....	77
Block Diagrams .....	
16-Bit Timer1 Module .....	183
Connections for On-Chip Voltage Regulator .....	270
DSP Engine .....	39
dsPIC33F06GS101 Devices with 1 SAR .....	240
dsPIC33F06GS102 Devices with 1 SAR .....	241
dsPIC33F06GS202 Devices with 1 SAR .....	242
dsPIC33F16GS402/404 Devices with 1 SAR .....	243
dsPIC33F16GS502 Devices with 2 SARs .....	244
dsPIC33F16GS504 Devices with 2 SARs .....	245
dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 .....	18
dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 CPU Core .....	32
High-Speed Analog Comparator .....	263
I2CX Module .....	226
Input Capture x .....	191
Multiplexing of Remappable Output for RPN .....	159
Oscillator System .....	135
Output Compare x Module .....	193
Partitioned Output Pair, Complementary PWM Mode .....	200
PLL .....	137
Remappable MUX Input for U1RX .....	157
Reset System .....	89
Shared Port Structure .....	155
Simplified Conceptual High-Speed PWM .....	199
SPIx Module .....	219
Timer2/3 (32-Bit) .....	187
Type B Timer .....	185
Type C Timer .....	185
UART1 .....	233
Watchdog Timer (WDT) .....	271
Brown-out Reset (BOR) .....	94, 267, 270

### C

C Compilers .....	
MPLAB XC Compilers .....	284
Clock Switching .....	146
Enabling .....	146
Sequence .....	146

### Code Examples

Erasing a Program Memory Page .....	87
Initiating a Programming Sequence .....	88
Loading Write Buffers .....	88
Port Write/Read .....	156
PWRSV Instruction Syntax .....	147
Code Protection .....	267, 273
CodeGuard Security .....	267
Configuration Bits .....	267
Description .....	268
Configuration Register Map .....	267
Configuring Analog Port Pins .....	156
CPU .....	
Control Registers .....	34
CPU Clocking System .....	136
PLL Configuration .....	137
Selection .....	136
Sources .....	136
Customer Change Notification Service .....	392
Customer Notification Service .....	392
Customer Support .....	392

### D

DAC .....	264
Output Range .....	264
Data Accumulators and Adder/Subtractor .....	40
Data Space Write Saturation .....	42
Overflow and Saturation .....	40
Round Logic .....	41
Write Back .....	41
Data Address Space .....	45
Alignment .....	45
Memory Map for dsPIC33FJ06GS101/102 Devices with 256 Bytes of RAM .....	46
Memory Map for dsPIC33FJ06GS202 Device with 1-Kbyte RAM .....	47
Memory Map for dsPIC33FJ16GS402/404/502/504 Devices with 2-Kbyte RAM .....	48
Near Data Space .....	45
Software Stack .....	73
Width .....	45
Data Addressing .....	
Overview .....	31
DC and AC Characteristics .....	
Graphs and Tables .....	347
DC Characteristics .....	288, 342
Doze Current (IDOZE) .....	294, 344
High Temperature .....	334
I/O Pin Input Specifications .....	295
I/O Pin Output Specifications .....	297, 336
Idle Current (IDLE) .....	292, 343
Operating Current (IDD) .....	290, 342
Operating MIPS vs. Voltage .....	288, 334, 342
Power-Down Current (IPD) .....	293, 335
Program Memory .....	299, 337
Temperature and Voltage .....	334
Temperature and Voltage Specifications .....	289
Thermal Operating Conditions .....	334

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# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

dsPIC 33 FJ 06 GS1 02 T - 50 E / SP - XXX		
Microchip Trademark	_____	
Architecture	_____	
Flash Memory Family	_____	
Program Memory Size (Kbyte)	_____	
Product Group	_____	
Pin Count	_____	
Tape and Reel Flag (if applicable)	_____	
Speed (if applicable)	_____	
Temperature Range	_____	
Package	_____	
Pattern	_____	

Architecture:	33	=	16-bit Digital Signal Controller
Flash Memory Family:	FJ	=	Flash program memory, 3.3V
Product Group:	GS1	=	Switch Mode Power Supply (SMPS) family
	GS2	=	Switch Mode Power Supply (SMPS) family
	GS4	=	Switch Mode Power Supply (SMPS) family
	GS5	=	Switch Mode Power Supply (SMPS) family
Pin Count:	01	=	18-pin
	02	=	28-pin
	04	=	44-pin
Speed	50	=	50 MIPS
Temperature Range:	I	=	-40°C to+85°C (Industrial)
	E	=	-40°C to+125°C (Extended)
	H	=	-40°C to+150°C (High)
Package:	PT	=	Plastic Thin Quad Flatpack - 10x10x1 mm body (TQFP)
	ML	=	Plastic Quad Flat, No Lead Package - 8x8 mm body (QFN)
	MM	=	Plastic Quad Flat, No Lead Package - 6x6x0.9 mm body (QFN-S)
	SO	=	Plastic Small Outline - Wide - 7.50 mm body (SOIC)
	SP	=	Skinny Plastic Dual In-Line - 300 mil body (SPDIP)
	TL	=	Very Thin Leadless Array - 6x6 mm body (VTLA)

### Examples:

- a) dsPIC33FJ06GS102-E/SP:  
SMPS dsPIC33, 6-Kbyte program  
memory, 28-pin, Extended  
temperature, SPDIP package.