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#### Details

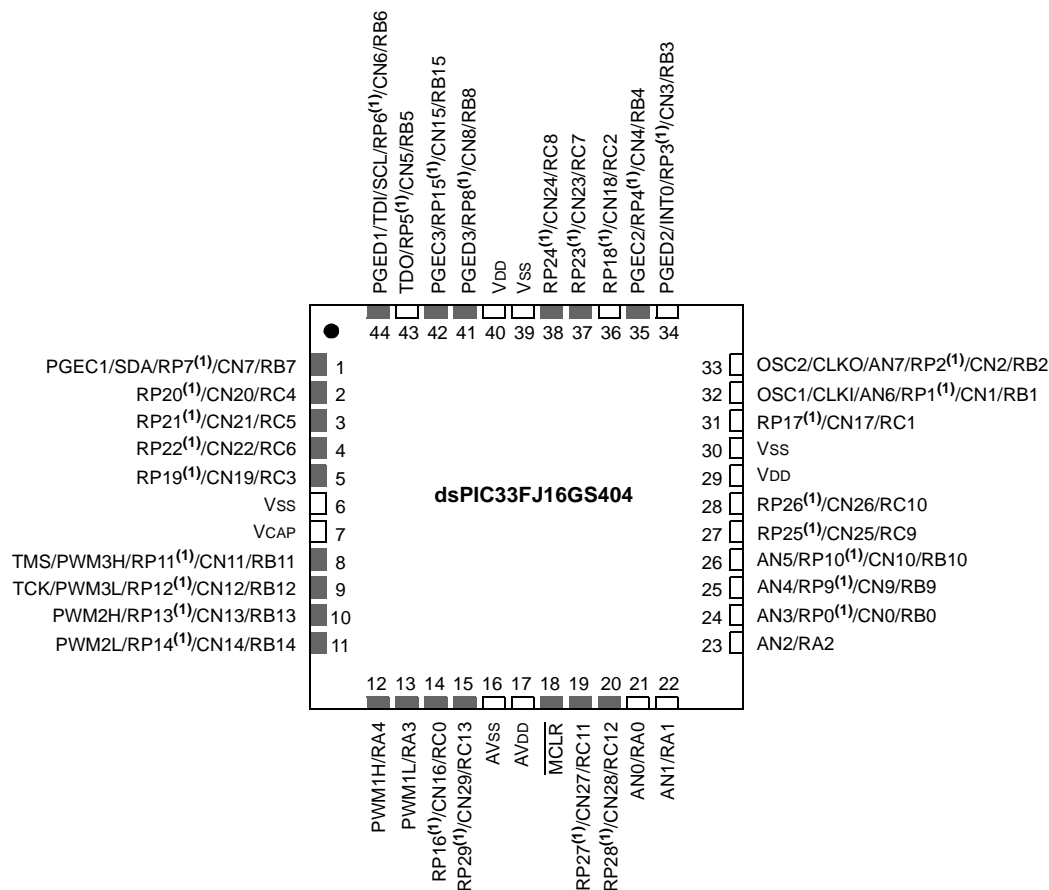
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	6KB (6K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj06gs202-e-sp">https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj06gs202-e-sp</a>

# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

## Pin Diagrams (Continued)

44-Pin QFN<sup>(2)</sup>

■ = Pins are up to 5V tolerant



- Note** 1: The RPN pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.  
 2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

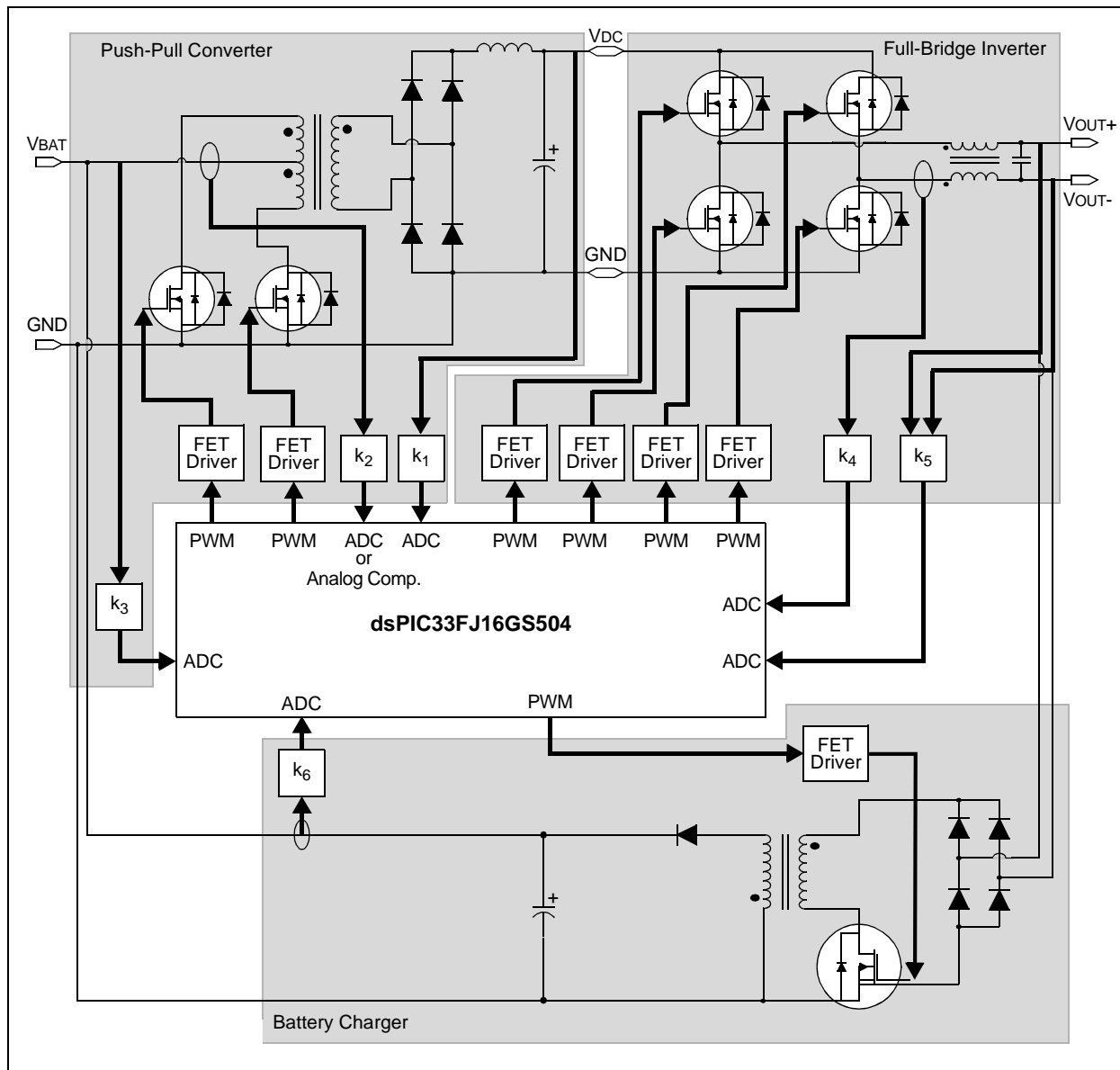
# **dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04**

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NOTES:

# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

**FIGURE 2-8: OFF-LINE UPS**



## 4.2.5 X AND Y DATA SPACES

The core has two data spaces, X and Y. These data spaces can be considered either separate (for some DSP instructions), or as one unified linear address range (for MCU instructions). The data spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X data space is used by all instructions and supports all addressing modes. X data space has separate read and write data buses. The X read data bus is the read data path for all instructions that view data space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y data space is used in concert with the X data space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY.N and MSC) to provide two concurrent data read paths.

Both the X and Y data spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X data space.

All data memory writes, including in DSP instructions, view data space as combined X and Y address space. The boundary between the X and Y data spaces is device-dependent and is not user-programmable.

All Effective Addresses are 16 bits wide and point to bytes within the data space. Therefore, the data space address range is 64 Kbytes, or 32K words, though the implemented memory locations vary by device.

**TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33FJ06GS102 DEVICES ONLY**

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFail	—	0000
INTCON2	0082	ALTVT	DISI	—	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	—	ADIF	U1TXIF	U1RXIF	SP1IF	SP1EIF	—	T2IF	—	—	—	T1IF	OC1IF	—	INT0IF	0000
IFS1	0086	—	—	INT2IF	—	—	—	—	—	—	—	—	INT1IF	CNIF	—	MI2C1IF	SI2C1IF	0000
IFS3	008A	—	—	—	—	—	—	PSEMIF	—	—	—	—	—	—	—	—	—	0000
IFS4	008C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIF	—	0000
IFS5	008E	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	0090	ADCP1IF	ADCP0IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS7	0092	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP2IF	0000
IEC0	0094	—	—	ADIE	U1TXIE	U1RXIE	SP1IE	SP1EIE	—	T2IE	—	—	—	T1IE	OC1IE	—	INT0IE	0000
IEC1	0096	—	—	INT2IE	—	—	—	—	—	—	—	—	INT1IE	CNIE	—	MI2C1IE	SI2C1IE	0000
IEC3	009A	—	—	—	—	—	—	PSEMIE	—	—	—	—	—	—	—	—	—	0000
IEC4	009C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIE	—	0000
IEC5	009E	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	00A0	ADCP1IE	ADCP0IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC7	00A2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP2IE	0000
IPC0	00A4	—	T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0	—	—	—	—	—	INT0IP2	INT0IP1	INT0IP0	4404
IPC1	00A6	—	T2IP2	T2IP1	T2IP0	—	—	—	—	—	—	—	—	—	—	—	—	4000
IPC2	00A8	—	U1RXIP2	U1RXIP2	U1RXIP0	—	SP1IP2	SP1IP1	SP1IP0	—	SP1EIP2	SP1EIP1	SP1EIP0	—	—	—	—	4440
IPC3	00AA	—	—	—	—	—	—	—	—	—	ADIP2	ADIP1	ADIP0	—	U1TXIP2	U1TXIP1	U1TXIP0	0044
IPC4	00AC	—	CNIP2	CNIP1	CNIP0	—	—	—	—	—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0	4044
IPC5	00AE	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0	0004
IPC7	00B2	—	—	—	—	—	—	—	—	—	INT2IP2	INT2IP1	INT2IP0	—	—	—	—	0040
IPC14	00C0	—	—	—	—	—	—	—	—	—	PSEMIP2	PSEMIP1	PSEMIP0	—	—	—	—	0040
IPC16	00C4	—	—	—	—	—	—	—	—	—	U1EIP2	U1EIP1	U1EIP0	—	—	—	—	0040
IPC23	00D2	—	PWM2IP2	PWM2IP1	PWM2IP0	—	PWM1IP2	PWM1IP1	PWM1IP0	—	—	—	—	—	—	—	—	4400
IPC27	00DA	—	ADCP1IP2	ADCP1IP1	ADCP1IP0	—	ADCP0IP2	ADCP0IP1	ADCP0IP0	—	—	—	—	—	—	—	—	4400
IPC28	00DC	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP2IP2	ADCP2IP1	ADCP2IP0	0004
INTTREG	00E0	—	—	—	—	ILR3	ILR2	ILR1	ILR0	—	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-41: SYSTEM CONTROL REGISTER MAP**

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	—	—	—	—	CM	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	xxxx <sup>(1)</sup>
OSCCON	0742	—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0	CLKLOCK	IOLOCK	LOCK	—	CF	—	—	OSWEN	0300 <sup>(2)</sup>
CLKDIV	0744	ROI	DOZE2	DOZE1	DOZE0	DOZEN	FRCDIV2	FRCDIV1	FRCDIV0	PLLPOST1	PLLPOST0	—	PLLPRE4	PLLPRE3	PLLPRE2	PLLPRE1	PLLPRE0	3040
PLLFBD	0746	—	—	—	—	—	—	—	PLLDIV<8:0>									0030
REFOCON	074E	ROON	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0	—	—	—	—	—	—	—	—	0000
OSCTUN	0748	—	—	—	—	—	—	—	—	—	—	—	TUN<5:0>					0000
ACLKCON	0750	ENAPLL	APLLCK	SELACLK	—	—	APSTSCLR2	APSTSCLR1	APSTSCLR0	ASRCSEL	FRCSEL	—	—	—	—	—	—	2300

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** The RCON register Reset values are dependent on the type of Reset.

**2:** The OSCCON register Reset values are dependent on the FOSC<sub>x</sub> Configuration bits and on type of Reset.

**TABLE 4-42: NVM REGISTER MAP**

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0760	WR	WREN	WRERR	—	—	—	—	—	—	ERASE	—	—	NVMOP3	NVMOP2	NVMOP1	NVMOP0	0000 <sup>(1)</sup>
NVMKEY	0766	—	—	—	—	—	—	—	—	—	NVMKEY<7:0>							0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Reset value shown is for POR only. The value on other Reset states is dependent on the state of memory write or erase operations at the time of Reset.

**TABLE 4-43: PMD REGISTER MAP FOR dsPIC33FJ06GS101 DEVICES ONLY**

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	—	—	—	T2MD	T1MD	—	PWMMD	—	I2C1MD	—	U1MD	—	SPI1MD	—	—	ADCMD	0000
PMD2	0772	—	—	—	—	—	—	IC2MD	IC1MD	—	—	—	—	—	—	OC2MD	OC1MD	0000
PMD3	0774	—	—	—	—	—	CMPMD	—	—	—	—	—	—	—	—	—	—	0000
PMD4	0776	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—	0000
PMD6	077A	—	—	—	—	PWM4MD	—	—	PWM1MD	—	—	—	—	—	—	—	—	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-44: PMD REGISTER MAP FOR dsPIC33FJ06GS102 DEVICES ONLY**

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	—	—	—	T2MD	T1MD	—	PWMMD	—	I2C1MD	—	U1MD	—	SPI1MD	—	—	ADCMD	0000
PMD2	0772	—	—	—	—	—	—	IC2MD	IC1MD	—	—	—	—	—	—	OC2MD	OC1MD	0000
PMD3	0774	—	—	—	—	—	CMPMD	—	—	—	—	—	—	—	—	—	—	0000
PMD4	0776	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—	0000
PMD6	077A	—	—	—	—	—	—	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

TABLE 4-48: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn forms the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn forms the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

## 4.3.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions and the DSP accumulator class of instructions to provide a greater addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

**Note:** For the `MOV` instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (register offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-bit Literal
- 16-bit Literal

**Note:** Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

## 4.3.4 MAC INSTRUCTIONS

The dual source operand DSP instructions (`CLR`, `ED`, `EDAC`, `MAC`, `MPY`, `MPY.N`, `MOVSAC` and `MSC`), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The two-source operand prefetch registers must be members of the set {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must, therefore, be valid addresses within X data space for W8 and W9 and Y data space for W10 and W11.

**Note:** Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the MAC class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

## 4.3.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, `BRA` (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the `DISI` instruction uses a 14-bit unsigned literal field. In some instructions, such as `ADD ACC`, the source of an operand or result is implied by the opcode itself. Certain operations, such as `NOP`, do not have any operands.



# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

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## REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

bit 2	<b>STKERR:</b> Stack Error Trap Status bit 1 = Stack error trap has occurred 0 = Stack error trap has not occurred
bit 1	<b>OSCFAIL:</b> Oscillator Failure Trap Status bit 1 = Oscillator failure trap has occurred 0 = Oscillator failure trap has not occurred
bit 0	<b>Unimplemented:</b> Read as '0'

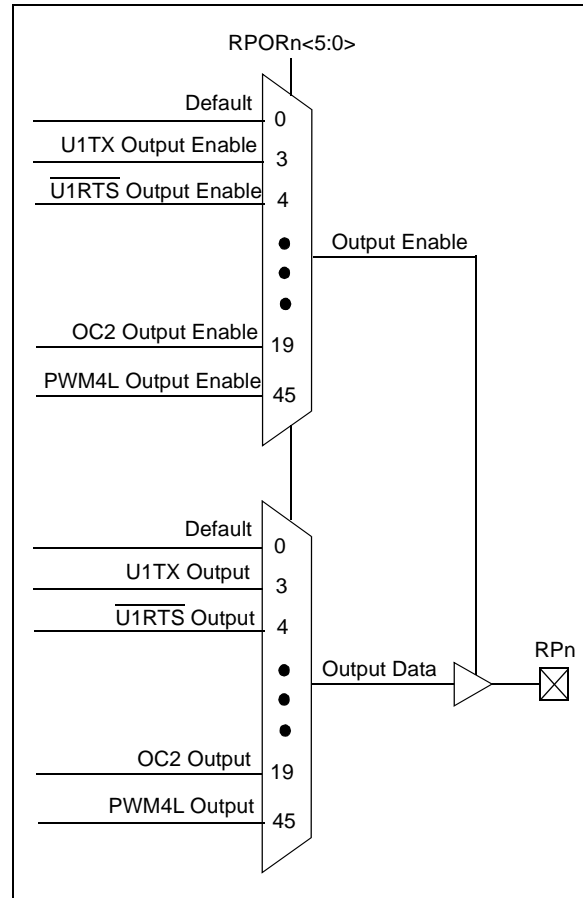
# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

## 10.6.2.2 Output Mapping

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 6-bit fields, with each set associated with one RPn pin (see Register 10-15 through Register 10-31). The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 10-2 and Figure 10-3).

The list of peripherals for output mapping also includes a null value of '00000' because of the mapping technique. This permits any given pin to remain unconnected from the output of any of the pin selectable peripherals.

**FIGURE 10-3: MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPn**



**TABLE 10-2: OUTPUT SELECTION FOR REMAPPABLE PIN (RPn)**

Function	RPORn<5:0>	Output Name
NULL	000000	RPn tied to default port pin
U1TX	000011	RPn tied to UART1 transmit
U1RTS	000100	RPn tied to UART1 Ready-to-Send
SDO1	000111	RPn tied to SPI1 data output
SCK1	001000	RPn tied to SPI1 clock output
SS1	001001	RPn tied to SPI1 slave select output
OC1	010010	RPn tied to Output Compare 1
OC2	010011	RPn tied to Output Compare 2
SYNCO1	100101	RPn tied to external device synchronization signal via PWM master time base
REFCLKO	100110	REFCLK output signal
ACMP1	100111	RPn tied to Analog Comparator Output 1
ACMP2	101000	RPn tied to Analog Comparator Output 2
ACMP3	101001	RPn tied to Analog Comparator Output 3
ACMP4	101010	RPn tied to Analog Comparator Output 4
PWM4H	101100	RPn tied to PWM output pins associated with PWM Generator 4
PWM4L	101101	RPn tied to PWM output pins associated with PWM Generator 4

# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

## 10.7 Peripheral Pin Select Registers

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices implement 34 registers for remappable peripheral configuration:

- 15 Input Remappable Peripheral Registers
- 17 Output Remappable Peripheral Registers

Not all output remappable peripheral registers are implemented on all devices. See the specific register description for further details.

**Note:** Input and output register values can only be changed if `OSCCON<IOLOCK> = 0`. See **Section 10.6.3.1 “Control Register Lock”** for a specific command sequence.

### REGISTER 10-1: RPNR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0		U-0		R/W-1		R/W-1		R/W-1		R/W-1		R/W-1			
—		—		INT1R5		INT1R4		INT1R3		INT1R2		INT1R1		INT1R0	
bit 15												bit 8			

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
—	—	—	—	—	—	—	—	
bit 7								bit 0

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **INT1R<5:0>:** Assign External Interrupt 1 (INTR1) to the Corresponding RPN Pin bits

111111 = Input tied to Vss  
100011 = Input tied to RP35  
100010 = Input tied to RP34  
100001 = Input tied to RP33  
100000 = Input tied to RP32

- 
- 
- 

00000 = Input tied to RP0

bit 7-0 **Unimplemented:** Read as '0'

# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

## 11.0 TIMER1

**Note 1:** This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “Timers” (DS70205) in the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer, which can serve as a time counter for the Real-Time Clock (RTC), or operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be operated from the low-power 32 kHz crystal oscillator available on the device
- Can be operated in Asynchronous Counter mode from an external clock source
- Optionally, the external clock input (T1CK) can be synchronized to the internal device clock and the clock synchronization is performed after the prescaler

The unique features of Timer1 allow it to be used for Real-Time Clock (RTC) applications. A block diagram of Timer1 is shown in Figure 11-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

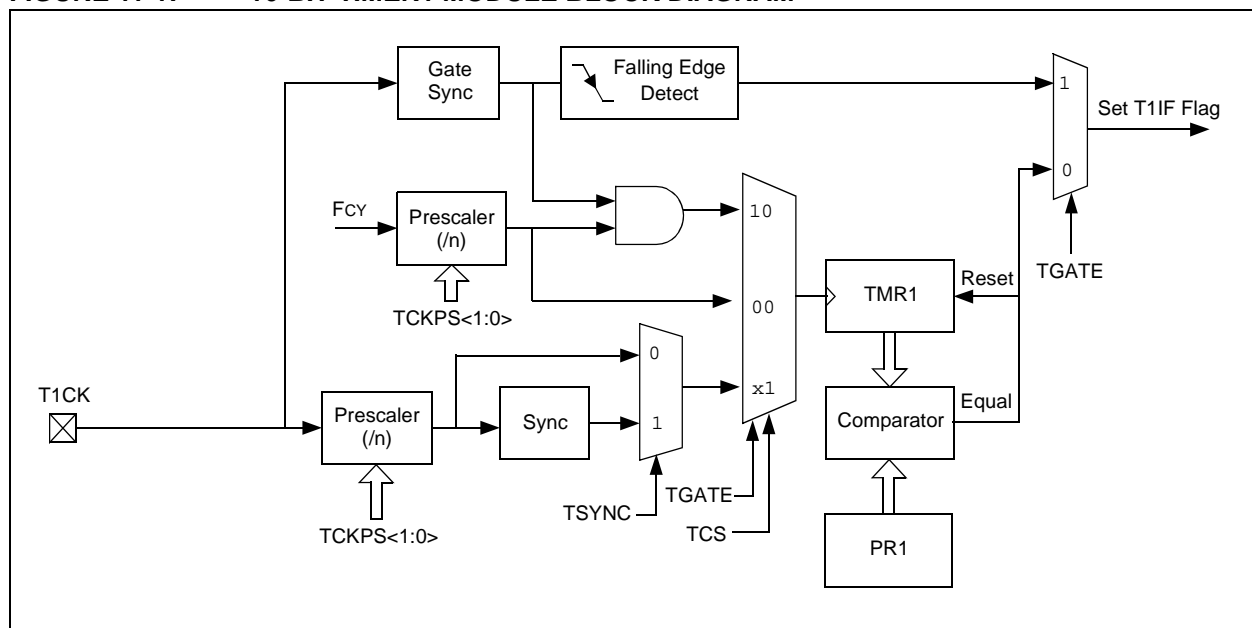
- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

The timer control bit settings for different operating modes are given in the Table 11-1.

**TABLE 11-1: TIMER MODE SETTINGS**

Mode	TCS	TGATE	TSYNC
Timer	0	0	x
Gated Timer	0	1	x
Synchronous Counter	1	x	1
Asynchronous Counter	1	x	0

**FIGURE 11-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM**



# **dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04**

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NOTES:

# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

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## REGISTER 16-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)

bit 4-2      **SPRE<2:0>**: Secondary Prescale bits (Master mode)<sup>(2)</sup>

111 = Secondary prescale 1:1

110 = Secondary prescale 2:1

•

•

•

000 = Secondary prescale 8:1

bit 1-0      **PPRE<1:0>**: Primary Prescale bits (Master mode)<sup>(2)</sup>

11 = Primary prescale 1:1

10 = Primary prescale 4:1

01 = Primary prescale 16:1

00 = Primary prescale 64:1

**Note 1:** The CKE bit is not used in the Framed SPI modes. Program this bit to '0' for the Framed SPI modes (FRMEN = 1).

**2:** Do not set both primary and secondary prescalers to a value of 1:1.

**3:** This bit must be cleared when FRMEN = 1.

# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

## REGISTER 17-1: I2CxCON: I2Cx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

<b>Legend:</b>	U = Unimplemented bit, read as '0'						
R = Readable bit	W = Writable bit		HC = Hardware Clearable bit				
-n = Value at POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown		

- bit 15      **I2CEN:** I2Cx Enable bit  
1 = Enables the I2Cx module, and configures the SDAx and SCLx pins as serial port pins  
0 = Disables the I2Cx module; all I<sup>2</sup>C™ pins are controlled by port functions.
- bit 14      **Unimplemented:** Read as '0'
- bit 13      **I2CSIDL:** I2Cx Stop in Idle Mode bit  
1 = Discontinues module operation when device enters an Idle mode  
0 = Continues module operation in Idle mode
- bit 12      **SCLREL:** SCLx Release Control bit (when operating as I<sup>2</sup>C slave)  
1 = Releases SCLx clock  
0 = Holds SCLx clock low (clock stretch)  
If STREN = 1:  
Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.  
If STREN = 0:  
Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of slave transmission.
- bit 11      **IPMIEN:** Intelligent Peripheral Management Interface (IPMI) Enable bit  
1 = IPMI mode is enabled; all addresses are Acknowledged  
0 = IPMI mode is disabled
- bit 10      **A10M:** 10-Bit Slave Address bit  
1 = I2CxADD is a 10-bit slave address  
0 = I2CxADD is a 7-bit slave address
- bit 9      **DISSLW:** Disable Slew Rate Control bit  
1 = Slew rate control is disabled  
0 = Slew rate control is enabled
- bit 8      **SMEN:** SMBus Input Levels bit  
1 = Enables I/O pin thresholds compliant with SMBus specification  
0 = Disables SMBus input thresholds
- bit 7      **GCEN:** General Call Enable bit (when operating as I<sup>2</sup>C slave)  
1 = Enables interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)  
0 = General call address is disabled
- bit 6      **STREN:** SCLx Clock Stretch Enable bit (when operating as I<sup>2</sup>C slave)  
Used in conjunction with the SCLREL bit.  
1 = Enables software or receive clock stretching  
0 = Disables software or receive clock stretching

# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

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## REGISTER 19-7: ADCPC2: ANALOG-TO-DIGITAL CONVERT PAIR CONTROL REGISTER 2<sup>(1)</sup> (CONTINUED)

bit 4-0      **TRGSRC4<4:0>**: Trigger 4 Source Selection bits  
Selects trigger source for conversion of Analog Channels AN9 and AN8.  
11111 = Timer2 period match  
•  
•  
•  
11011 = Reserved  
11010 = PWM Generator 4 current-limit ADC trigger  
11001 = PWM Generator 3 current-limit ADC trigger  
11000 = PWM Generator 2 current-limit ADC trigger  
10111 = PWM Generator 1 current-limit ADC trigger  
10110 = Reserved  
•  
•  
•  
10010 = Reserved  
10001 = PWM Generator 4 secondary trigger is selected  
10000 = PWM Generator 3 secondary trigger is selected  
01111 = PWM Generator 2 secondary trigger is selected  
01110 = PWM Generator 1 secondary trigger is selected  
01101 = Reserved  
01100 = Timer1 period match  
•  
•  
•  
01000 = Reserved  
00111 = PWM Generator 4 primary trigger is selected  
00110 = PWM Generator 3 primary trigger is selected  
00101 = PWM Generator 2 primary trigger is selected  
00100 = PWM Generator 1 primary trigger is selected  
00011 = PWM Special Event Trigger is selected  
00010 = Global software trigger is selected  
00001 = Individual software trigger is selected  
00000 = No conversion is enabled

**Note 1:** This register is only implemented in the dsPIC33FJ16GS504 devices.

**2:** The trigger source must be set as a global software trigger prior to setting this bit to '1'. If other conversions are in progress, then the conversion will be performed when the conversion resources are available.



# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

**TABLE 24-19: AC CHARACTERISTICS: INTERNAL FRC ACCURACY**

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature                   -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
Internal FRC Accuracy @ FRC Frequency = 7.37 MHz <sup>(1)</sup>							
F20a	FRC	-2	—	+2	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
F20b	FRC	-5	—	+5	%	-40°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V

**Note 1:** Frequency calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

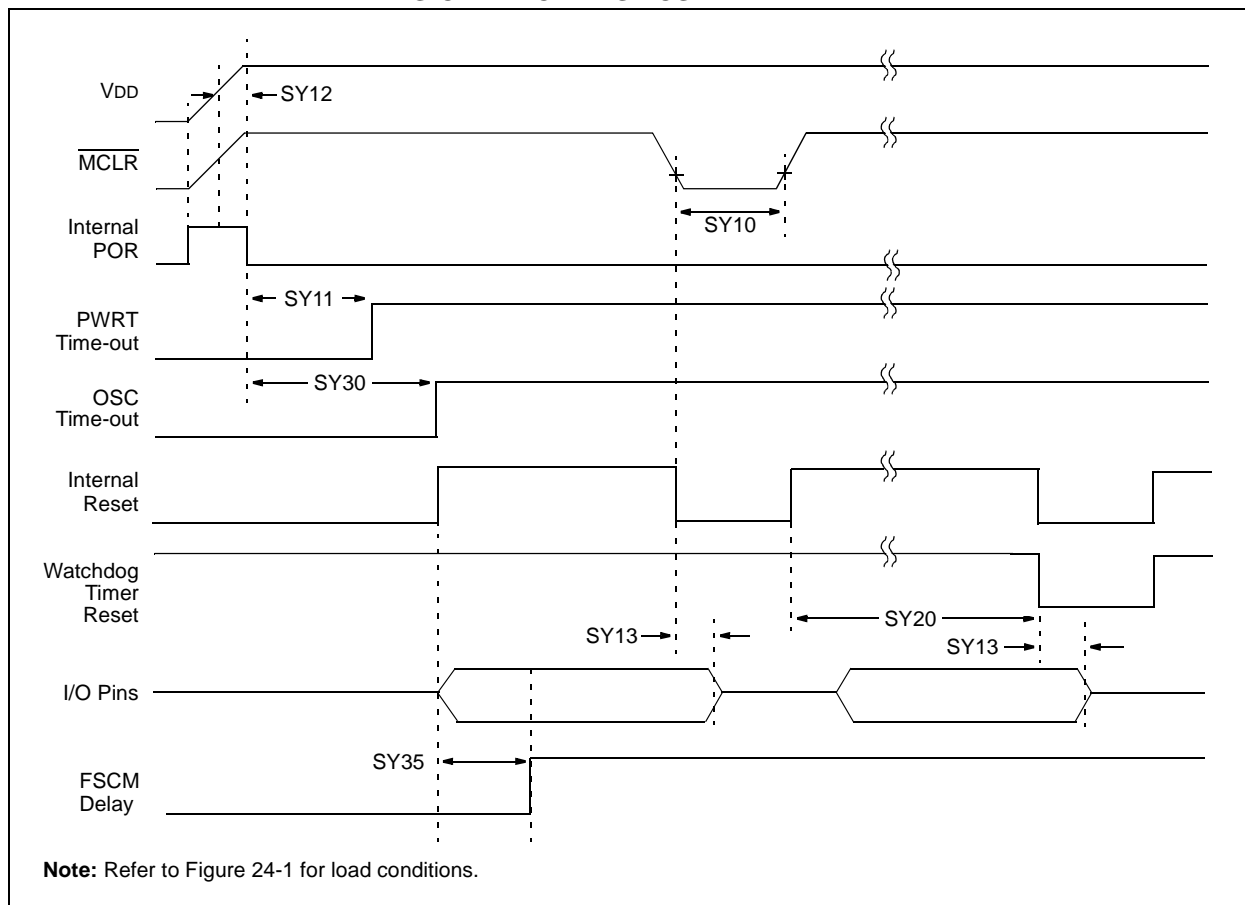
**TABLE 24-20: AC CHARACTERISTICS: INTERNAL LPRC ACCURACY**

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature    -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
LPRC @ 32.768 kHz <sup>(1)</sup>							
F21a	LPRC	-20	±6	+20	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
F21b	LPRC	-70	—	+70	%	-40°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V

**Note 1:** Change of LPRC frequency as V<sub>DD</sub> changes.

# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

**FIGURE 24-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING CHARACTERISTICS**



# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

**TABLE 24-37: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Units	Conditions
SP70	TscP	Maximum SCKx Input Frequency	—	—	11	MHz	See <b>Note 3</b>
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and <b>Note 4</b>
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 and <b>Note 4</b>
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and <b>Note 4</b>
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and <b>Note 4</b>
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx $\uparrow$ or SCKx Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx} \uparrow$ to SDOx Output High-Impedance	10	—	50	ns	See <b>Note 4</b>
SP52	Tsch2ssH, TscL2ssH	$\overline{SSx}$ after SCKx Edge	1.5 TCY + 40	—	—	ns	See <b>Note 4</b>

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the Master must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

# **dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04**

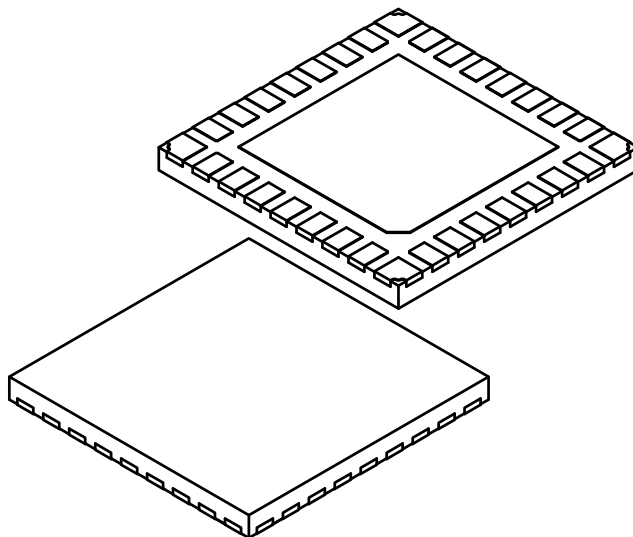
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NOTES:

# dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

## 28-Lead Plastic Quad Flat, No Lead Package (MX) - 6x6x0.5mm Body [UQFN] Ultra-Thin with 0.40 x 0.60 mm Terminal Width/Length and Corner Anchors

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	0.40	0.50	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	(A3)	0.127 REF		
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2		4.00	
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2		4.00	
Terminal Width	b	0.35	0.40	0.45
Corner Pad	b2	0.25	0.40	0.45
Terminal Length	L	0.55	0.60	0.65
Terminal-to-Exposed Pad	K	0.20	-	-

### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.
4. Outermost portions of corner structures may vary slightly.