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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

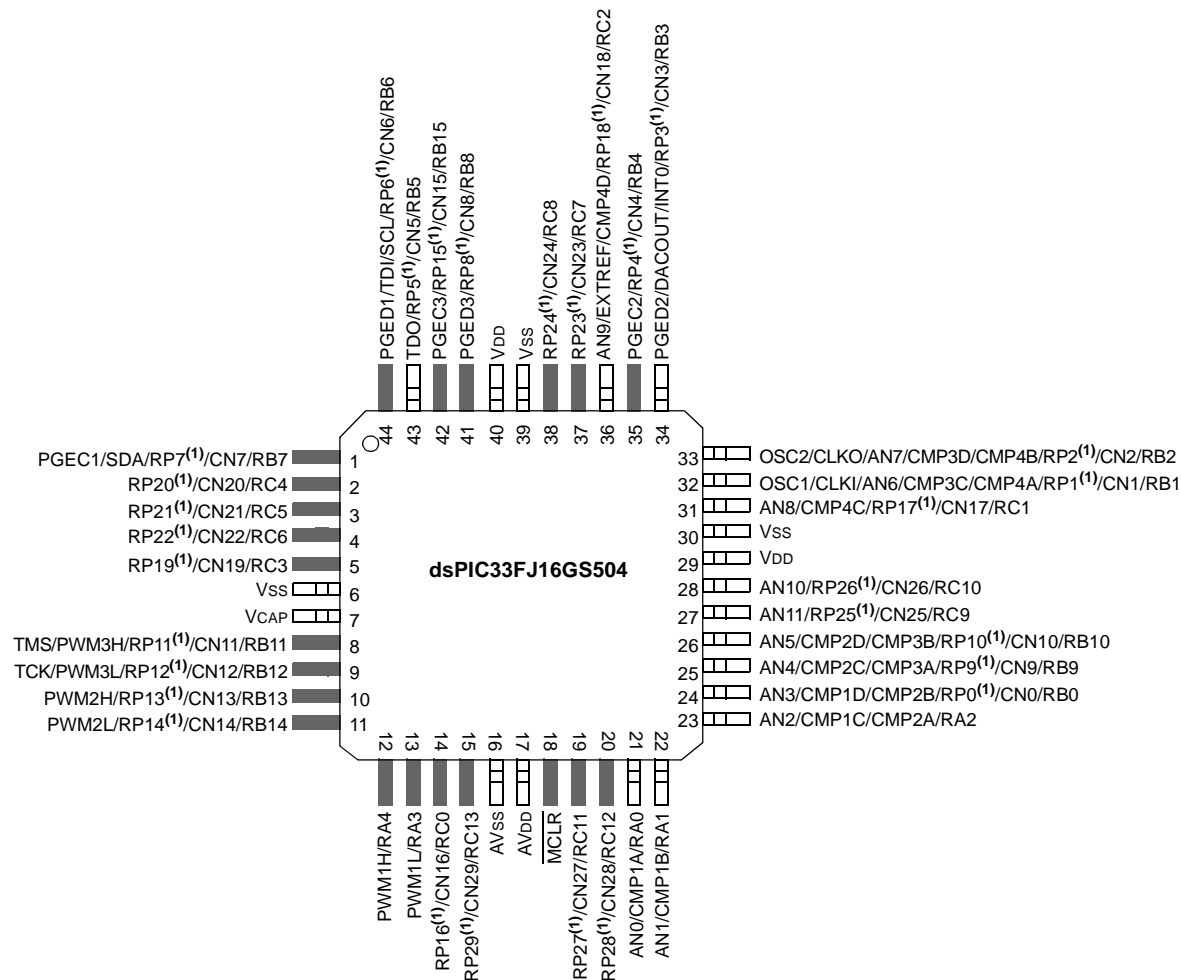
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	6KB (6K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj06gs202-i-so

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

Pin Diagrams (Continued)

44-Pin TQFP

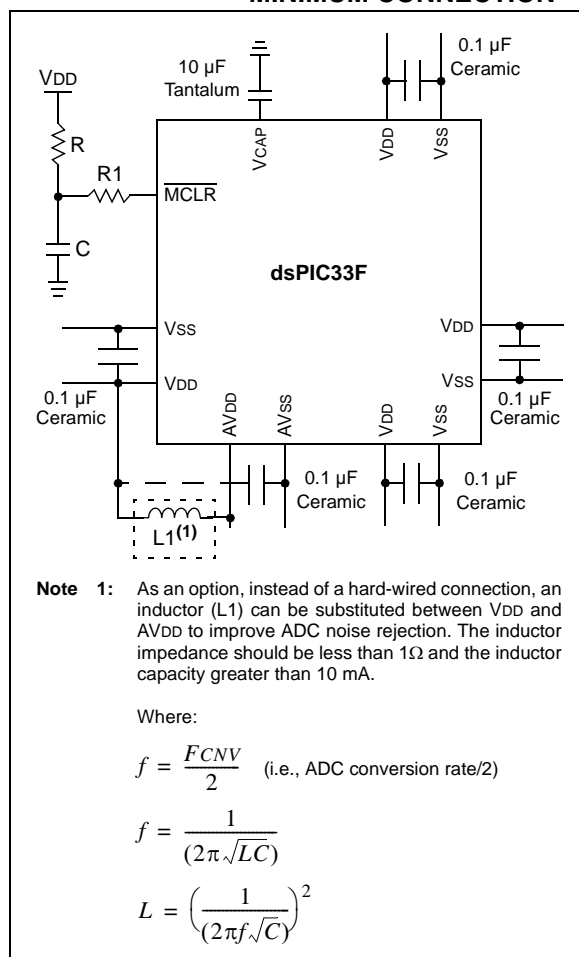
■ = Pins are up to 5V tolerant



Note 1: The RPN pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 Capacitor on Internal Voltage Regulator (VCAP)

A low-ESR (<5 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD, and must have a capacitor between 4.7 µF and 10 µF, 16V connected to ground. The type can be ceramic or tantalum. Refer to **Section 24.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the VCAP. It is recommended that the trace length not exceed one-quarter inch (6 mm). Refer to **Section 21.2 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

- Device Reset
- Device programming and debugging.

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS

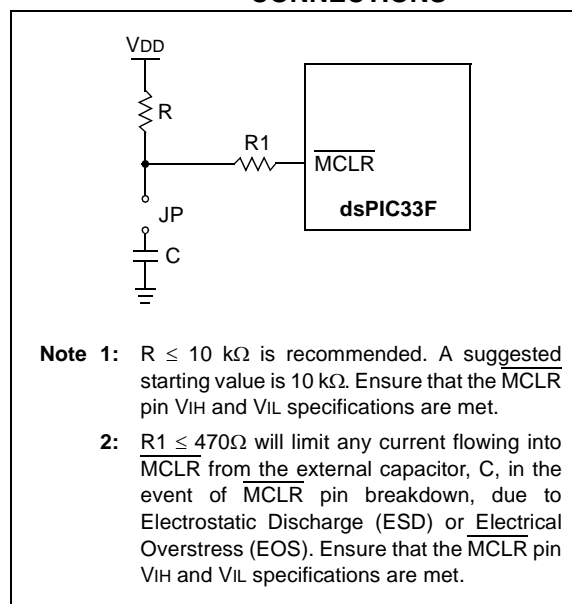
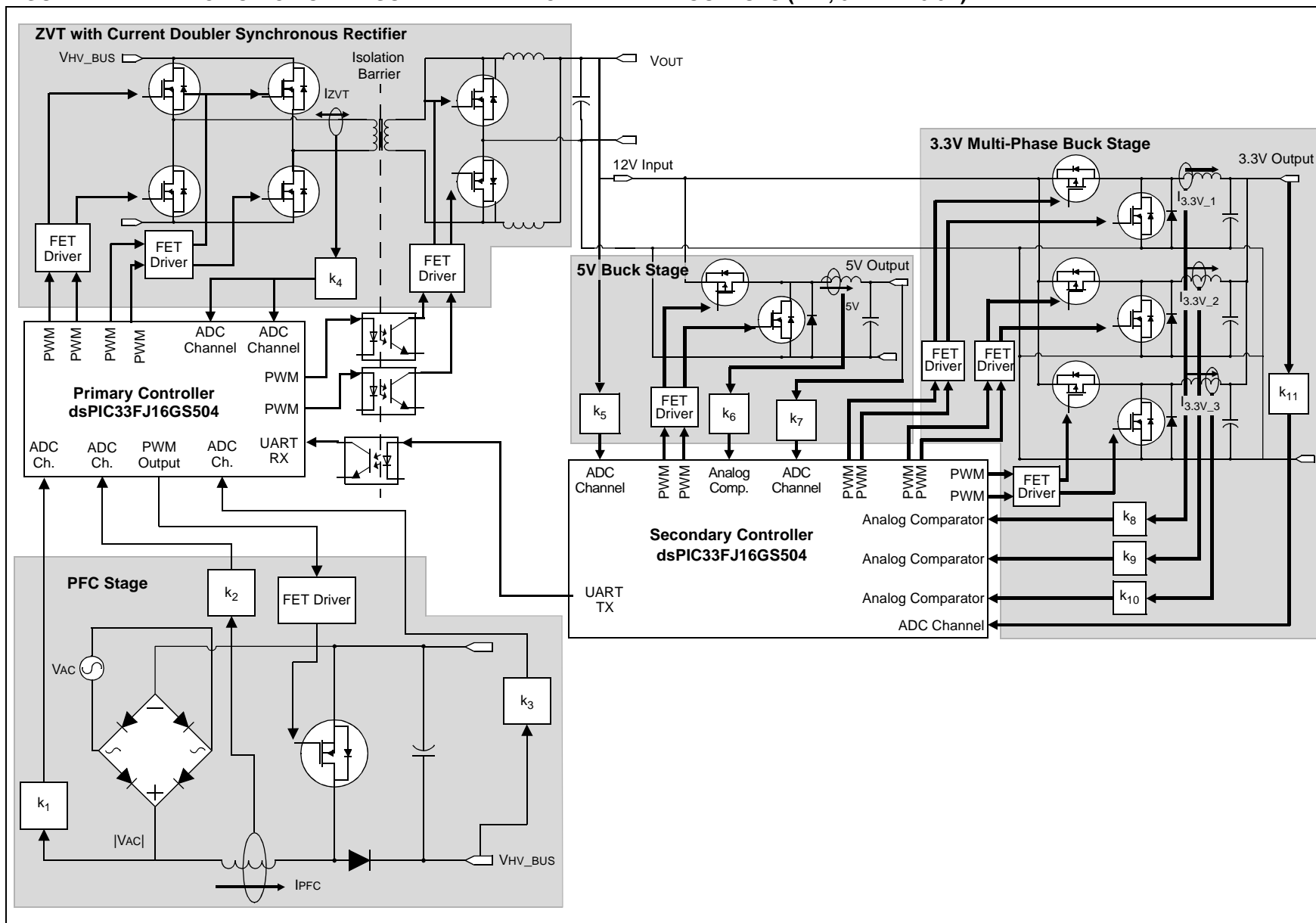


FIGURE 2-11: AC-TO-DC POWER SUPPLY WITH PFC AND THREE OUTPUTS (12V, 5V AND 3.3V)

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate consider each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (see Figure 4-2).

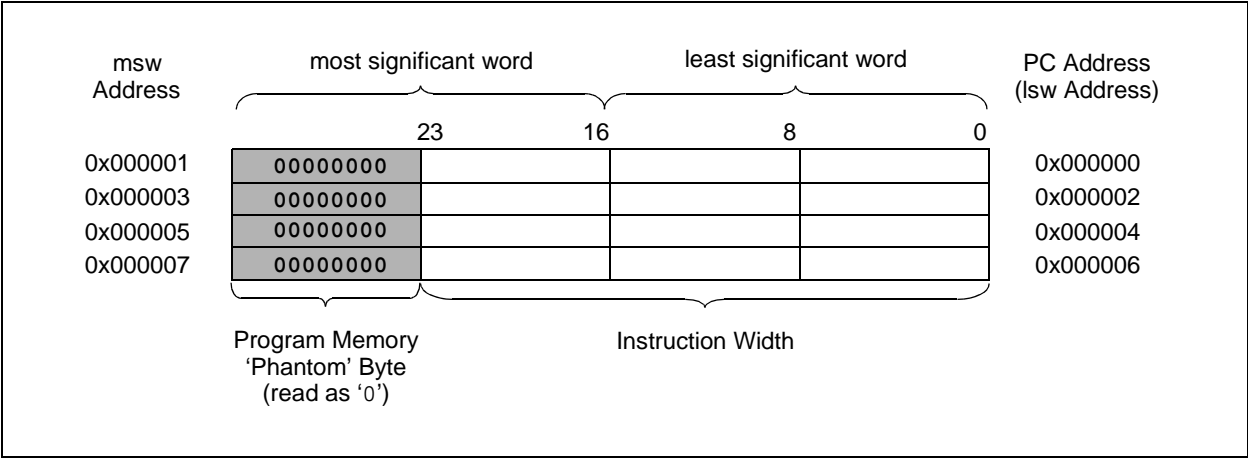
Program memory addresses are always word-aligned on the lower word, and addresses are incremented or decremented by two during the code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices reserve the addresses between 0x00000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at 0x000000, with the actual address for the start of code at 0x000002.

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices also have two interrupt vector tables, located from 0x000004 to 0x0000FF and 0x000100 to 0x0001FF. These vector tables allow each of the device interrupt sources to be handled by separate Interrupt Service Routines (ISRs). A more detailed discussion of the interrupt vector tables is provided in **Section 7.1 “Interrupt Vector Table”**.

FIGURE 4-2: PROGRAM MEMORY ORGANIZATION



dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

FIGURE 4-3: DATA MEMORY MAP FOR dsPIC33FJ06GS101/102 DEVICES WITH 256 BYTES OF RAM

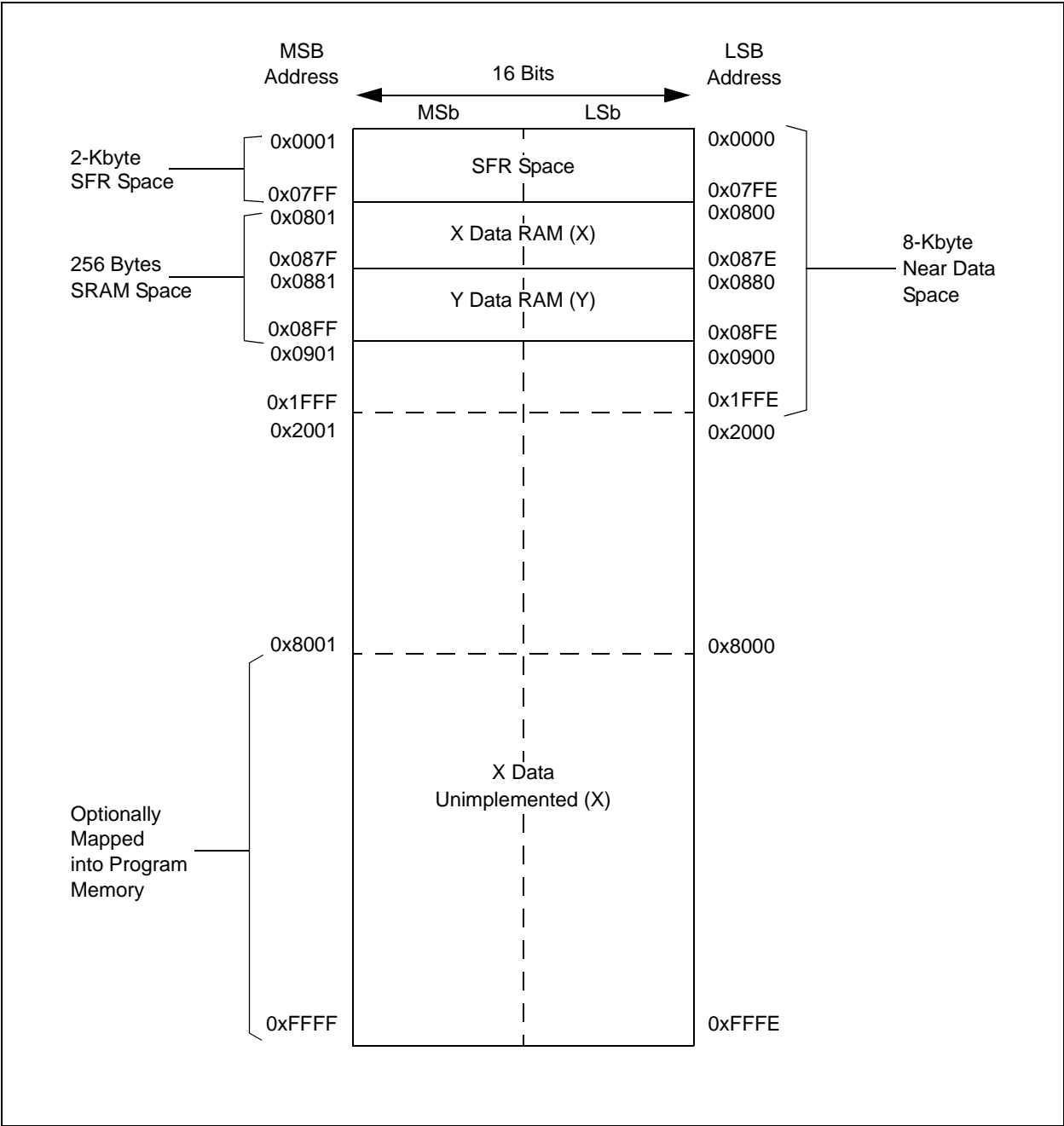


TABLE 4-30: HIGH-SPEED 10-BIT ADC REGISTER MAP FOR dsPIC33FJ16GS504 DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
ADCON	0300	ADON	—	ADSIDL	SLOWCLK	—	GSWTRG	—	FORM	EIE	ORDER	SEQSAMP	ASYNCSAMP	—	ADCS2	ADCS1	ADCS0	0003	
ADPCFG	0302	—	—	—	—	PCFG11	PCFG10	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000	
ADSTAT	0306	—	—	—	—	—	—	—	—	—	P6RDY	P5RDY	P4RDY	P3RDY	P2RDY	P1RDY	P0RDY	0000	
ADBASE	0308	ADBASE<15:1>																—	0000
ADPC0	030A	IRQEN1	PEND1	SWTRG1	TRGSRC14	TRGSRC13	TRGSRC12	TRGSRC11	TRGSRC10	IRQEN0	PEND0	SWTRG0	TRGSRC04	TRGSRC03	TRGSRC02	TRGSRC01	TRGSRC00	0000	
ADPC1	030C	IRQEN3	PEND3	SWTRG3	TRGSRC34	TRGSRC33	TRGSRC32	TRGSRC31	TRGSRC30	IRQEN2	PEND2	SWTRG2	TRGSRC24	TRGSRC23	TRGSRC22	TRGSRC21	TRGSRC20	0000	
ADPC2	030E	IRQEN5	PEND5	SWTRG5	TRGSRC54	TRGSRC53	TRGSRC52	TRGSRC51	TRGSRC50	IRQEN4	PEND4	SWTRG4	TRGSRC44	TRGSRC43	TRGSRC42	TRGSRC41	TRGSRC40	0000	
ADPC3	0310	—	—	—	—	—	—	—	—	IRQEN6	PEND6	SWTRG6	TRGSRC64	TRGSRC63	TRGSRC62	TRGSRC61	TRGSRC60	0000	
ADCBUF0	0320	ADC Data Buffer 0																xxxx	
ADCBUF1	0322	ADC Data Buffer 1																xxxx	
ADCBUF2	0324	ADC Data Buffer 2																xxxx	
ADCBUF3	0326	ADC Data Buffer 3																xxxx	
ADCBUF4	0328	ADC Data Buffer 4																xxxx	
ADCBUF5	032A	ADC Data Buffer 5																xxxx	
ADCBUF6	032C	ADC Data Buffer 6																xxxx	
ADCBUF7	032E	ADC Data Buffer 7																xxxx	
ADCBUF8	0330	ADC Data Buffer 8																xxxx	
ADCBUF9	0332	ADC Data Buffer 9																xxxx	
ADCBUF10	0334	ADC Data Buffer 10																xxxx	
ADCBUF11	0336	ADC Data Buffer 11																xxxx	
ADCBUF12	0338	ADC Data Buffer 12																xxxx	
ADCBUF13	033A	ADC Data Buffer 13																xxxx	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

TABLE 4-48: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn forms the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn forms the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

4.3.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions and the DSP accumulator class of instructions to provide a greater addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the `MOV` instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (register offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-bit Literal
- 16-bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.3.4 MAC INSTRUCTIONS

The dual source operand DSP instructions (`CLR`, `ED`, `EDAC`, `MAC`, `MPY`, `MPY.N`, `MOVSAC` and `MSC`), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The two-source operand prefetch registers must be members of the set {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must, therefore, be valid addresses within X data space for W8 and W9 and Y data space for W10 and W11.

Note: Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the MAC class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.3.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, `BRA` (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the `DISI` instruction uses a 14-bit unsigned literal field. In some instructions, such as `ADD ACC`, the source of an operand or result is implied by the opcode itself. Certain operations, such as `NOP`, do not have any operands.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 7-22: IPC3: INTERRUPT PRIORITY CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	ADIP2	ADIP1	ADIP0	—	U1TXIP2	U1TXIP1	U1TXIP0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **ADIP<2:0>:** ADC1 Conversion Complete Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **U1TXIP<2:0>:** UART1 Transmitter Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 7-33: IPC28: INTERRUPT PRIORITY CONTROL REGISTER 28

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	ADCP5IP2	ADCP5IP1	ADCP5IP0	—	ADCP4IP2	ADCP4IP1	ADCP4IP0
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	ADCP3IP2	ADCP3IP1	ADCP3IP0	—	ADCP2IP2	ADCP2IP1	ADCP2IP0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **ADCP5IP<2:0>:** ADC Pair 5 Conversion Done Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **ADCP4IP<2:0>:** ADC Pair 4 Conversion Done Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **ADCP3IP<2:0>:** ADC Pair 3 Conversion Done Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **ADCP2IP<2:0>:** ADC Pair 2 Conversion Done Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

8.1.3 PLL CONFIGURATION

The primary oscillator and internal FRC oscillator can optionally use an on-chip PLL to obtain higher speeds of operation. The PLL provides significant flexibility in selecting the device operating speed. A block diagram of the PLL is shown in Figure 8-2.

The output of the primary oscillator or FRC, denoted as 'FIN', is divided down by a prescale factor (N1) of 2, 3, ... or 33 before being provided to the PLL's Voltage Controlled Oscillator (VCO). The input to the VCO must be selected in the range of 0.8 MHz to 8 MHz. The prescale factor 'N1' is selected using the PLLPRE<4:0> bits (CLKDIV<4:0>).

The PLL Feedback Divisor, selected using the PLLDIV<8:0> bits (PLLFBD<8:0>), provides a factor, 'M', by which the input to the VCO is multiplied. This factor must be selected such that the resulting VCO output frequency is in the range of 100 MHz to 200 MHz.

The VCO output is further divided by a postscale factor, 'N2'. This factor is selected using the PLLPOST<1:0> bits (CLKDIV<7:6>). 'N2' can be either 2, 4, or 8, and must be selected such that the PLL output frequency (Fosc) is in the range of 12.5 MHz to 80 MHz, which generates device operating speeds of 6.25-40 MIPS.

For a primary oscillator or FRC oscillator, output 'FIN', the PLL output 'Fosc' is given by Equation 8-2.

EQUATION 8-2: Fosc CALCULATION

$$F_{OSC} = F_{IN} * \left(\frac{M}{N1 * N2} \right)$$

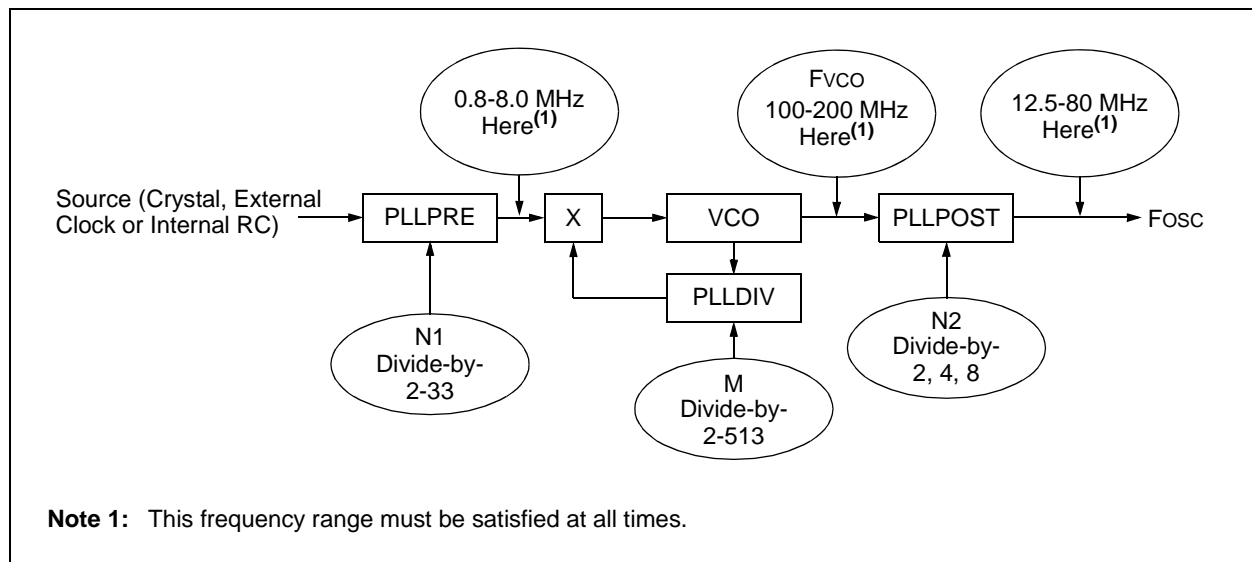
For example, suppose a 10 MHz crystal is being used with the selected oscillator mode of XT with PLL (see Equation 8-3).

- If PLLPRE<4:0> = 0, then N1 = 2. This yields a VCO input of 10/2 = 5 MHz, which is within the acceptable range of 0.8-8 MHz.
- If PLLDIV<8:0> = 0x1E, then M = 32. This yields a VCO output of 5 x 32 = 160 MHz, which is within the 100-200 MHz range needed.
- If PLLPOST<1:0> = 0, then N2 = 2. This provides a Fosc of 160/2 = 80 MHz. The resultant device operating speed is 80/2 = 40 MIPS.

EQUATION 8-3: XT WITH PLL MODE EXAMPLE

$$F_{CY} = \frac{F_{OSC}}{2} = \frac{1}{2} \left(\frac{10000000 * 32}{2 * 2} \right) = 40 \text{ MIPS}$$

FIGURE 8-2: dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 PLL BLOCK DIAGRAM



dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER^(1,2) (CONTINUED)

- bit 3 **CF:** Clock Fail Detect bit (read/clear by application)
 1 = FSCM has detected clock failure
 0 = FSCM has not detected clock failure
- bit 2-1 **Unimplemented:** Read as '0'
- bit 0 **OSWEN:** Oscillator Switch Enable bit
 1 = Request oscillator switch to selection specified by NOSC<2:0> bits
 0 = Oscillator switch is complete

- Note 1:** Writes to this register require an unlock sequence. Refer to “**Oscillator (Part IV)**” (DS70307) in the “*dsPIC33F/PIC24H Family Reference Manual*” (available from the Microchip web site) for details.
- 2:** This register is reset only on a Power-on Reset (POR).
- 3:** Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 8-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN<5:0> ⁽²⁾					
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits⁽²⁾

011111 = Center frequency + 11.6% (8.2268 MHz)

011110 = Center frequency + 11.2% (8.1992 MHz)

•

•

•

000001 = Center frequency + 0.375% (7.3976 MHz)

000000 = Center frequency (7.37 MHz nominal)

111111 = Center frequency – 0.375% (7.2594 MHz)

•

•

•

100001 = Center frequency – 11.6% (6.5132 MHz)

000000 = Center frequency – 12% (6.4856 MHz)

Note 1: This register is reset only on a Power-on Reset (POR).

2: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step-size is an approximation and is neither characterized nor tested.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 10-20: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5⁽¹⁾

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP11R5	RP11R4	RP11R3	RP11R2	RP11R1	RP11R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP10R5	RP10R4	RP10R3	RP10R2	RP10R1	RP10R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP11R<5:0>:** Peripheral Output Function is Assigned to RP11 Output Pin bits
(see Table 10-2 for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP10R<5:0>:** Peripheral Output Function is Assigned to RP10 Output Pin bits
(see Table 10-2 for peripheral function numbers)

Note 1: This register is not implemented in the dsPIC33FJ06GS101 device.

REGISTER 10-21: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6⁽¹⁾

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP13R5	RP13R4	RP13R3	RP13R2	RP13R1	RP13R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP12R5	RP12R4	RP12R3	RP12R2	RP12R1	RP12R0
bit 7							bit 0

Legend:

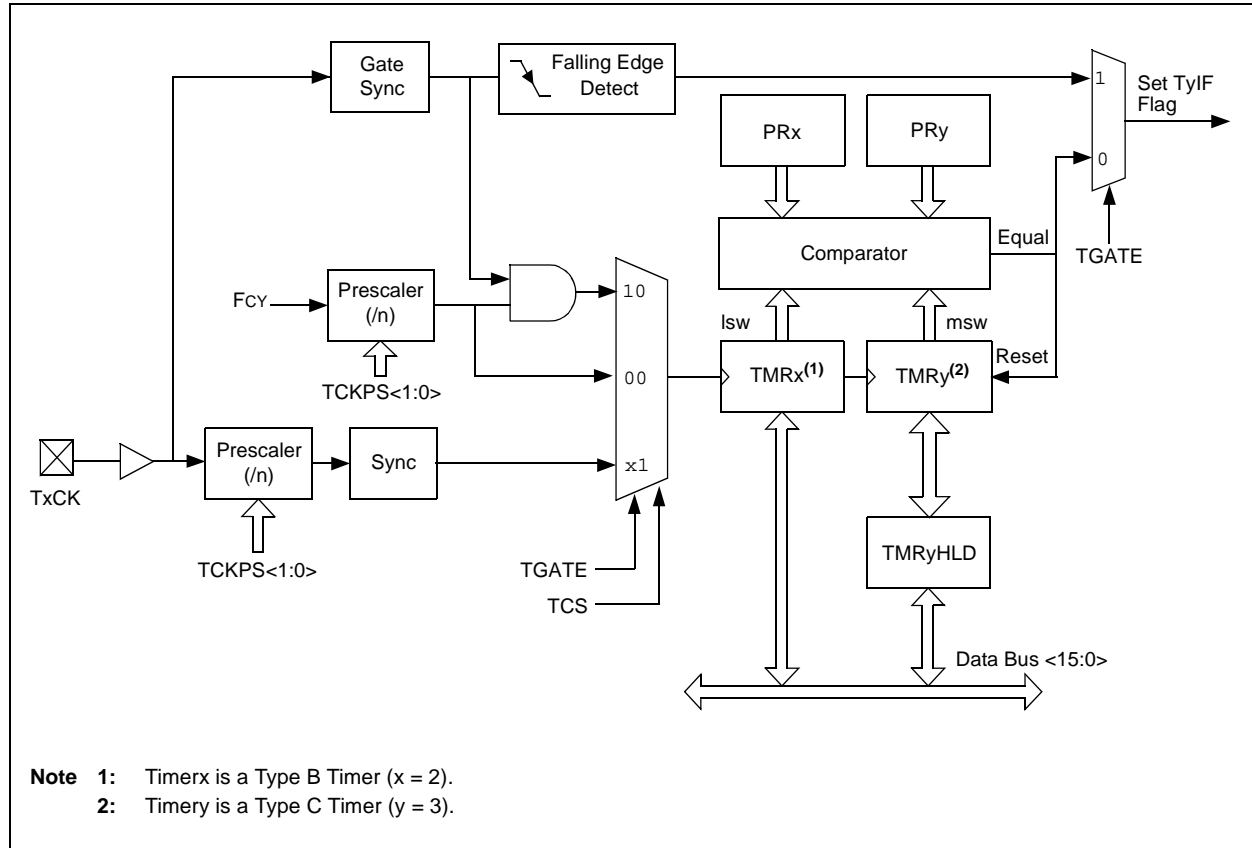
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP13R<5:0>:** Peripheral Output Function is Assigned to RP13 Output Pin bits
(see Table 10-2 for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP12R<5:0>:** Peripheral Output Function is Assigned to RP12 Output Pin bits
(see Table 10-2 for peripheral function numbers)

Note 1: This register is not implemented in the dsPIC33FJ06GS101 device.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

FIGURE 12-3: 32-BIT TIMER BLOCK DIAGRAM



dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 15-13: TRGCONx: PWMx TRIGGER CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—
bit 15				bit 8			

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTM ⁽¹⁾	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **TRGDIV<3:0>**: Trigger # Output Divider bits

1111 = Trigger output for every 16th trigger event
 1110 = Trigger output for every 15th trigger event
 1101 = Trigger output for every 14th trigger event
 1100 = Trigger output for every 13th trigger event
 1011 = Trigger output for every 12th trigger event
 1010 = Trigger output for every 11th trigger event
 1001 = Trigger output for every 10th trigger event
 1000 = Trigger output for every 9th trigger event
 0111 = Trigger output for every 8th trigger event
 0110 = Trigger output for every 7th trigger event
 0101 = Trigger output for every 6th trigger event
 0100 = Trigger output for every 5th trigger event
 0011 = Trigger output for every 4th trigger event
 0010 = Trigger output for every 3rd trigger event
 0001 = Trigger output for every 2nd trigger event
 0000 = Trigger output for every trigger event

bit 11-8 **Unimplemented**: Read as '0'

bit 7 **DTM**: Dual Trigger Mode bit⁽¹⁾

1 = Secondary trigger event is combined with the primary trigger event to create the PWM trigger.
 0 = Secondary trigger event is not combined with the primary trigger event to create the PWM trigger;
 two separate PWM triggers are generated

bit 6 **Unimplemented**: Read as '0'

bit 5-0 **TRGSTRT<5:0>**: Trigger Postscaler Start Enable Select bits

111111 = Wait 63 PWM cycles before generating the first trigger event after the module is enabled
 •
 •
 •
 000010 = Wait 1 PWM cycles before generating the first trigger event after the module is enabled
 000001 = Wait 1 PWM cycle before generating the first trigger event after the module is enabled
 000000 = Wait 0 PWM cycles before generating the first trigger event after the module is enabled

Note 1: The secondary generator cannot generate PWM trigger interrupts.

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REGISTER 17-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 4	P: Stop bit 1 = Indicates that a Stop bit has been detected last 0 = Stop bit was not detected last Hardware is set or clear when Start, Repeated Start or Stop is detected.
bit 3	S: Start bit 1 = Indicates that a Start (or Repeated Start) bit has been detected last 0 = Start bit was not detected last Hardware is set or clear when Start, Repeated Start or Stop is detected.
bit 2	R_W: Read/Write Information bit (when operating as I ² C slave) 1 = Read – indicates data transfer is output from slave 0 = Write – indicates data transfer is input to slave Hardware is set or clear after reception of an I ² C device address byte.
bit 1	RBF: Receive Buffer Full Status bit 1 = Receive is complete, I2CxRCV is full 0 = Receive is not complete, I2CxRCV is empty Hardware is set when I2CxRCV is written with a received byte. Hardware is clear when software reads I2CxRCV.
bit 0	TBF: Transmit Buffer Full Status bit 1 = Transmit is in progress, I2CxTRN is full 0 = Transmit is complete, I2CxTRN is empty Hardware is set when software writes to I2CxTRN. Hardware is clear at completion of data transmission.

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REGISTER 19-8: ADCPC3: ANALOG-TO-DIGITAL CONVERT PAIR CONTROL REGISTER 3⁽¹⁾

bit 4-0 **TRGSRC6<4:0>**: Trigger 6 Source Selection bits
Selects trigger source for conversion of Analog Channels AN13 and AN12.
11111 = Timer2 period match
•
•
•
11011 = Reserved
11010 = PWM Generator 4 current-limit ADC trigger
11001 = PWM Generator 3 current-limit ADC trigger
11000 = PWM Generator 2 current-limit ADC trigger
10111 = PWM Generator 1 current-limit ADC trigger
10110 = Reserved
•
•
•
10010 = Reserved
10001 = PWM Generator 4 secondary trigger is selected
10000 = PWM Generator 3 secondary trigger is selected
01111 = PWM Generator 2 secondary trigger is selected
01110 = PWM Generator 1 secondary trigger is selected
01101 = Reserved
01100 = Timer1 period match
•
•
•
01000 = Reserved
00111 = PWM Generator 4 primary trigger is selected
00110 = PWM Generator 3 primary trigger is selected
00101 = PWM Generator 2 primary trigger is selected
00100 = PWM Generator 1 primary trigger is selected
00011 = PWM Special Event Trigger is selected
00010 = Global software trigger is selected
00001 = Individual software trigger is selected
00000 = No conversion is enabled

- Note 1:** This register is only implemented on the dsPIC33FJ16GS502 and dsPIC33FJ16GS504 devices.
- 2:** The trigger source must be set as global software trigger prior to setting this bit to '1'. If other conversions are in progress, conversion will be performed when the conversion resources are available.

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Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSBs are '0's. If this second word is executed as an instruction (by itself), it will execute as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the Program Counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles with the additional instruction cycle(s) executed as a NOP. Notable exceptions are the BRA

(unconditional/computed branch), indirect CALL/GOTO, all Table Reads and Table Writes and RETURN/RETfie instructions, which are single-word instructions but take two or three cycles. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

Note: For more details on the instruction set, refer to the "16-bit MCU and DSC Programmer's Reference Manual" (DS70157).

TABLE 22-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
<n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator Write-Back Destination Address register $\in \{W13, [W13]+2\}$
bit4	4-bit bit selection field (used in word-addressed instructions) $\in \{0..15\}$
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address $\in \{0x0000..0x1FFF\}$
lit1	1-bit unsigned literal $\in \{0,1\}$
lit4	4-bit unsigned literal $\in \{0..15\}$
lit5	5-bit unsigned literal $\in \{0..31\}$
lit8	8-bit unsigned literal $\in \{0..255\}$
lit10	10-bit unsigned literal $\in \{0..255\}$ for Byte mode, $\{0:1023\}$ for Word mode
lit14	14-bit unsigned literal $\in \{0..16384\}$
lit16	16-bit unsigned literal $\in \{0..65535\}$
lit23	23-bit unsigned literal $\in \{0..8388608\}$; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal $\in \{-512..511\}$
Slit16	16-bit signed literal $\in \{-32768..32767\}$
Slit6	6-bit signed literal $\in \{-16..16\}$
Wb	Base W register $\in \{W0..W15\}$
Wd	Destination W register $\in \{Wd, [Wd], [Wd++] , [Wd--], [++Wd], [--Wd] \}$
Wdo	Destination W register $\in \{Wnd, [Wnd], [Wnd++] , [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] \}$
Wm,Wn	Dividend, Divisor Working register pair (Direct Addressing)

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NOTES:

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