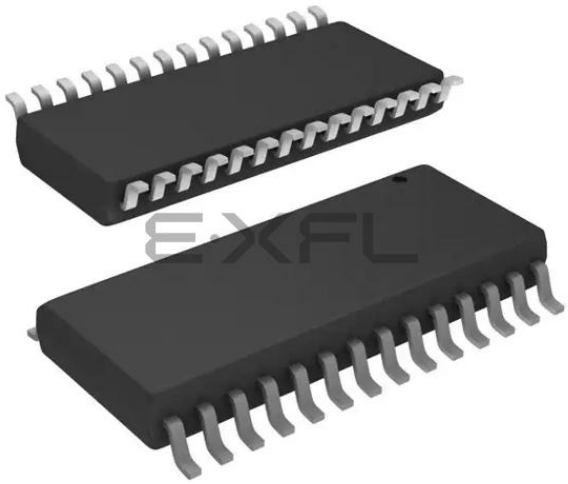
Microchip Technology - DSPIC33FJ16GS402-50I/SO Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	50 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gs402-50i-so

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Program Memory"** (DS70202) in the "*dsPIC33F/PIC24H Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 architecture features separate program and data memory spaces and buses. This architecture also allows the direct access to program memory from the data space during code execution.

4.1 Program Address Space

The program address memory space of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit Program Counter (PC) during program execution, or from table operation or data space remapping, as described in **Section 4.6 "Interfacing Program and Data Memory Spaces"**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

The memory maps for the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices are shown in Figure 4-1.

FIGURE 4-1: PROGRAM MEMORY MAPS FOR dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 DEVICES

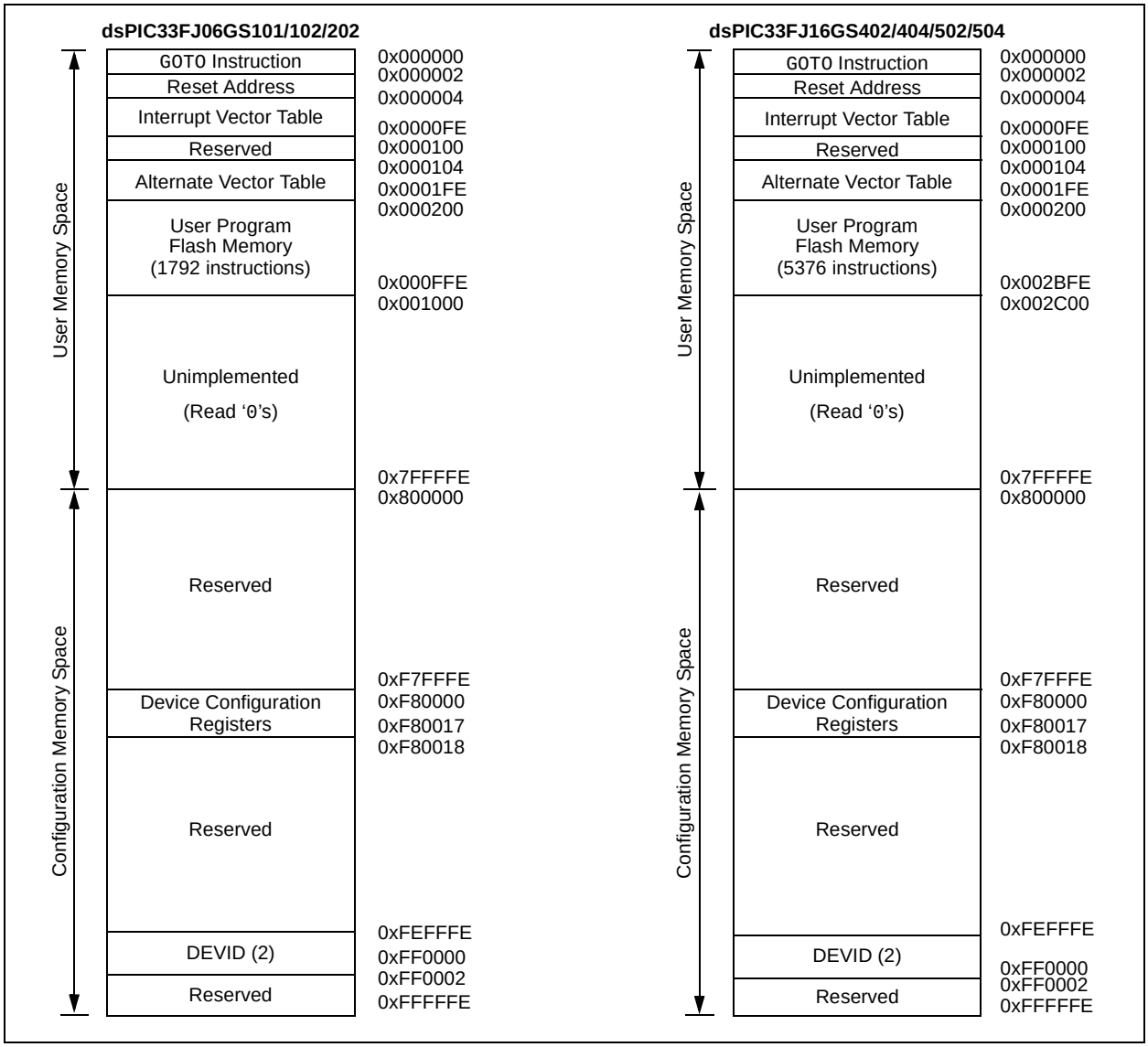


TABLE 4-33: PERIPHERAL PIN SELECT INPUT REGISTER MAP

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	0680	—	—	INT1R5	INT1R4	INT1R3	INT1R2	INT1R1	INT1R0	—	—	—	—	—	—	—	—	3F00
RPINR1	0682	—	—	—	—	—	—	—	—	—	—	INT2R5	INT2R4	INT2R3	INT2R2	INT2R1	INT2R0	003F
RPINR2	0684	—	—	T1CKR5	T1CKR4	T1CKR3	T1CKR2	T1CKR1	T1CKR0	—	—	—	—	—	—	—	—	0000
RPINR3	0686	—	—	T3CKR5	T3CKR4	T3CKR3	T3CKR2	T3CKR1	T3CKR0	—	—	T2CKR5	T2CKR4	T2CKR3	T2CKR2	T2CKR1	T2CKR0	3F3F
RPINR7	068E	—	—	IC2R5	IC2R4	IC2R3	IC2R2	IC2R1	IC2R0	—	—	IC1R5	IC1R4	IC1R3	IC1R2	IC1R1	IC1R0	3F3F
RPINR11	0696	—	—	—	—	—	—	—	—	—	—	OCFAR5	OCFAR4	OCFAR3	OCFAR2	OCFAR1	OCFAR0	3F3F
RPINR18	06A4	—	—	U1CTSR5	U1CTSR4	U1CTSR3	U1CTSR2	U1CTSR1	U1CTSR0	—	—	U1RXR5	U1RXR4	U1RXR3	U1RXR2	U1RXR1	U1RXR0	003F
RPINR20	06A8	—	—	SCK1R5	SCK1R4	SCK1R3	SCK1R2	SCK1R1	SCK1R0	—	—	SDI1R5	SDI1R4	SDI1R3	SDI1R2	SDI1R1	SDI1R0	3F3F
RPINR21	06AA	—	—	—	—	—	—	—	—	—	—	SS1R5	SS1R54	SS1R3	SS1R2	SS1R1	SS1R0	0000
RPINR29	06BA	—	—	FLT1R5	FLT1R4	FLT1R3	FLT1R2	FLT1R1	FLT1R0	—	—	—	—	—	—	—	—	3F00
RPINR30	06BC	—	—	FLT3R5	FLT3R4	FLT3R3	FLT3R2	FLT3R1	FLT3R0	—	—	FLT2R5	FLT2R4	FLT2R3	FLT2R2	FLT2R1	FLT2R0	3F3F
RPINR31	06BE	—	—	FLT5R5	FLT5R4	FLT5R3	FLT5R2	FLT5R1	FLT5R0	—	—	FLT4R5	FLT4R4	FLT4R3	FLT4R2	FLT4R1	FLT4R0	3F3F
RPINR32	06C0	—	—	FLT7R5	FLT7R4	FLT7R3	FLT7R2	FLT7R1	FLT7R0	—	—	FLT6R5	FLT6R4	FLT6R3	FLT6R2	FLT6R1	FLT6R0	3F3F
RPINR33	06C2	—	—	SYNCI1R5	SYNCI1R4	SYNCI1R3	SYNCI1R2	SYNCI1R1	SYNCI1R0	—	—	FLT8R5	FLT8R4	FLT8R3	FLT8R2	FLT8R1	FLT8R0	3F3F
RPINR34	06C4	—	—	—	—	—	—	—	—	—	—	SYNCI2R5	SYNCI2R4	SYNCI2R3	SYNCI2R2	SYNCI2R1	SYNCI2R0	3F3F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-34: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33FJ06GS101

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	06D0	—	—	RP1R5	RP1R4	RP1R3	RP1R2	RP1R1	RP1R0	—	—	RP0R5	RP0R4	RP0R3	RP0R2	RP0R1	RP0R0	0000
RPOR1	06D2	—	—	RP3R5	RP3R4	RP3R3	RP3R2	RP3R1	RP3R0	—	—	RP2R5	RP2R4	RP2R3	RP2R2	RP2R1	RP2R0	0000
RPOR2	06D4	—	—	RP5R5	RP5R4	RP5R3	RP5R2	RP5R1	RP5R0	—	—	RP4R5	RP4R4	RP4R3	RP4R2	RP4R1	RP4R0	0000
RPOR3	06D6	—	—	RP7R5	RP7R4	RP7R3	RP7R2	RP7R1	RP7R0	—	—	RP6R5	RP6R4	RP6R3	RP6R2	RP6R1	RP6R0	0000
RPOR16	06F0	—	—	RP33R5	RP33R4	RP33R3	RP33R2	RP33R1	RP33R0	—	—	RP32R5	RP32R4	RP32R3	RP32R2	RP32R1	RP32R0	0000
RPOR17	06F2	—	—	RP35R5	RP35R4	RP35R3	RP35R2	RP35R1	RP35R0	—	—	RP34R5	RP34R4	RP34R3	RP34R2	RP34R1	RP34R0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4 Modulo Addressing

Modulo Addressing mode is a method used to provide an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either data or program space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into program space) and Y data spaces. Modulo Addressing can operate on any W register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction as there are certain restrictions on the buffer start address (for incrementing buffers), or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

4.4.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

Note:	Y space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

4.4.2 W ADDRESS REGISTER SELECTION

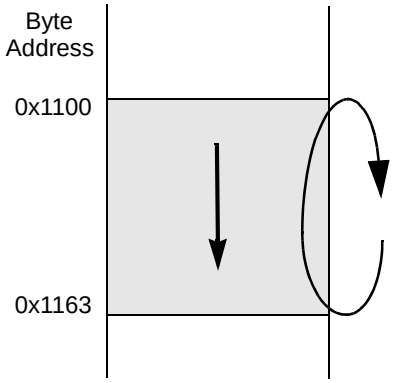
The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that will operate with Modulo Addressing:

- If XWM = 15, X RAGU and X WAGU Modulo Addressing is disabled.
- If YWM = 15, Y AGU Modulo Addressing is disabled.

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X data space when XWM is set to any value other than ‘15’ and the XMODEN bit is set at MODCON<15>.

The Y Address Space Pointer W register (YWM) to which Modulo Addressing is to be applied is stored in MODCON<7:4>. Modulo Addressing is enabled for Y data space when YWM is set to any value other than ‘15’ and the YMODEN bit is set at MODCON<14>.

FIGURE 4-7: MODULO ADDRESSING OPERATION EXAMPLE




```
MOV     #0x1100, W0
MOV     W0, XMODSRT     ;set modulo start address
MOV     #0x1163, W0
MOV     W0, MODEND      ;set modulo end address
MOV     #0x8001, W0
MOV     W0, MODCON      ;enable W1, X AGU for modulo

MOV     #0x0000, W0     ;W0 holds buffer fill value

MOV     #0x1110, W1     ;point W1 to buffer

DO      AGAIN, #0x31    ;fill the 50 buffer locations
MOV     W0, [W1++]      ;fill the next location
AGAIN:  INC W0, W0      ;increment the fill value
```

REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ALTIVT:** Enable Alternate Interrupt Vector Table bit
1 = Use alternate vector table
0 = Use standard (default) vector table

bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active

bit 13-3 **Unimplemented:** Read as ‘0’

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

REGISTER 7-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ADIF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IF	OC2IF	IC2IF	—	T1IF	OC1IF	IC1IF	INT0IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **ADIF:** ADC Group Conversion Complete Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12 **U1TXIF:** UART1 Transmitter Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 11 **U1RXIF:** UART1 Receiver Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 10 **SPI1IF:** SPI1 Event Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 9 **SPI1EIF:** SPI1 Fault Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8 **T3IF:** Timer3 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7 **T2IF:** Timer2 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6 **OC2IF:** Output Compare Channel 2 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **IC2IF:** Input Capture Channel 2 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **T1IF:** Timer1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **OC1IF:** Output Compare Channel 1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 7-31: IPC26: INTERRUPT PRIORITY CONTROL REGISTER 26

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	AC4IP2	AC4IP1	AC4IP0	—	AC3IP2	AC3IP1	AC3IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-4 **AC4IP<2:0>:** Analog Comparator 4 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **AC3IP<2:0>:** Analog Comparator 3 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

TABLE 10-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)

Input Name	Function Name	Register	Configuration Bits
External Interrupt 1	INT1	RPINR0	INT1R<5:0>
External Interrupt 2	INT2	RPINR1	INT2R<5:0>
Timer1 External Clock	T1CK	RPINR2	T1CKR<5:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<5:0>
Timer3 External Clock	T3CK	RPINR3	T3CKR<5:0>
Input Capture 1	IC1	RPINR7	IC1R<5:0>
Input Capture 2	IC2	RPINR7	IC2R<5:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<5:0>
UART1 Receive	U1RX	RPINR18	U1RXR<5:0>
UART1 Clear-to-Send	$\overline{\text{U1CTS}}$	RPINR18	U1CTSR<5:0>
SPI Data Input 1	SDI1	RPINR20	SDI1R<5:0>
SPI Clock Input 1	SCK1	RPINR20	SCK1R<5:0>
SPI Slave Select Input 1	$\overline{\text{SS1}}$	RPINR21	SS1R<5:0>
PWM Fault Input PWM1	FLT1	RPINR29	FLT1R<5:0>
PWM Fault Input PWM2	FLT2	RPINR30	FLT2R<5:0>
PWM Fault Input PWM3	FLT3	RPINR30	FLT3R<5:0>
PWM Fault Input PWM4	FLT4	RPINR31	FLT4R<5:0>
PWM Fault Input PWM5	FLT5	RPINR31	FLT5R<5:0>
PWM Fault Input PWM6	FLT6	RPINR32	FLT6R<5:0>
PWM Fault Input PWM7	FLT7	RPINR32	FLT7R<5:0>
PWM Fault Input PWM8	FLT8	RPINR33	FLT8R<5:0>
External Synchronization signal to PWM Master Time Base	SYNCI1	RPINR33	SYNCI1R<5:0>
External Synchronization signal to PWM Master Time Base	SYNCI2	RPINR34	SYNCI2R<5:0>

REGISTER 16-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
SPIEN	—	SPISIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/C-0	U-0	U-0	U-0	U-0	R-0	R-0
—	SPIROV	—	—	—	—	SPITBF	SPIRBF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **SPIEN:** SPIx Enable bit
1 = Enables module and configures SCKx, SDOx, SDIx and $\overline{SSx}$ as serial port pins
0 = Disables module

bit 14 **Unimplemented:** Read as '0'

bit 13 **SPISIDL:** SPIx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **SPIROV:** SPIx Receive Overflow Flag bit
1 = A new byte/word is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
0 = No overflow has occurred

bit 5-2 **Unimplemented:** Read as '0'

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit
1 = Transmit not yet started, SPIxTXB is full
0 = Transmit started, SPIxTXB is empty. Automatically set in hardware when CPU writes the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit
1 = Receive complete, SPIxRXB is full
0 = Receive is not complete, SPIxRXB is empty. Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when core reads the SPIxBUF location, reading SPIxRXB.

21.0 SPECIAL FEATURES

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F/PIC24H Family Reference Manual"*. Please see the Microchip web site (www.microchip.com) for the latest *"dsPIC33F/PIC24H Family Reference Manual"* sections.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation
- Brown-out Reset (BOR)

21.1 Configuration Bits

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices provide nonvolatile memory implementations for device Configuration bits. Refer to **"Device Configuration"** (DS70194) in the *"dsPIC33F/PIC24H Family Reference Manual"* for more information on this implementation.

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped starting at program memory location 0xF80000.

The individual Configuration bit descriptions for the Configuration registers are shown in Table 21-2.

Note that address, 0xF80000, is beyond the user program memory space. It belongs to the configuration memory space (0x800000-0xFFFFFF), which can only be accessed using Table Reads and Table Writes.

The device Configuration register map is shown in Table 21-1.

TABLE 21-1: DEVICE CONFIGURATION REGISTER MAP

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xF80000	FBS	—	—	—	—	BSS2	BSS1	BSS0	BWRP
0xF80002	Reserved	—	—	—	—	—	—	—	—
0xF80004	FGS	—	—	—	—	—	GSS1	GSS0	GWRP
0xF80006	FOSCSEL	IESO	—	—	—		FNOSC2	FNOSC1	FNOSC0
0xF80008	FOSC	FCKSM1	FCKSM0	IOL1WAY	—	—	OSCIOFNC	POSCMD1	POSCMD0
0xF8000A	FWDT	FWDTEN	WINDIS	—	WDTPRE	WDTPOST3	WDTPOST2	WDTPOST1	WDTPOST0
0xF8000C	FPOR	—	—	—	—	Reserved(2)	FPWRT2	FPWRT1	FPWRT0
0xF8000E	FICD	Reserved(1)		JTAGEN	—	—	—	ICS1	ICS0
0xF80010	FUID0	User Unit ID Byte 0							
0xF80012	FUID1	User Unit ID Byte 1							

Legend: — = unimplemented bit, read as '0'.

Note 1: These bits are reserved for use by development tools and must be programmed to '1'.

2: This bit reads the current programmed value.

21.2 On-Chip Voltage Regulator

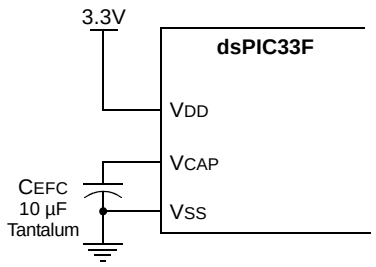
The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices power their core digital logic at a nominal 2.5V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. When the regulator is enabled, a low-ESR (less than 5 ohms) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 21-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 24-13 located in **Section 24.1 "DC Characteristics"**.

Note:	It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

On a POR, it takes approximately 20 μs for the on-chip voltage regulator to generate an output voltage. During this time, designated as TSTARTUP, code execution is disabled. TSTARTUP is applied every time the device resumes operation after any power-down.

FIGURE 21-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR(1,2,3)



Note 1: These are typical operating voltages. Refer to Table 24-13 located in **Section 24.1 "DC Characteristics"** for the full operating ranges of VDD.

2: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

3: Typical VCAP pin voltage = 2.5V when VDD ≥ VDDMIN.

21.3 BOR: Brown-out Reset

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines, or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM = 100 is applied. The total delay in this case is TFSCM.

The BOR Status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
29	DIV	DIV.S Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF Wm,Wn	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO #lit14,Expr	Do code to PC + Expr, lit14 + 1 times	2	2	None
		DO Wn,Expr	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED Wm*Wm,Acc,Wx,Wy,Wxd	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB, SA,SB,SAB
33	EDAC	EDAC Wm*Wm,Acc,Wx,Wy,Wxd	Euclidean Distance	1	1	OA,OB,OAB, SA,SB,SAB
34	EXCH	EXCH Wns,Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL Ws,Wnd	Find Bit Change from Left (MSb) Side	1	1	C
36	FF1L	FF1L Ws,Wnd	Find First One from Left (MSb) Side	1	1	C
37	FF1R	FF1R Ws,Wnd	Find First One from Right (LSb) Side	1	1	C
38	GOTO	GOTO Expr	Go to Address	2	2	None
		GOTO Wn	Go to Indirect	1	2	None
39	INC	INC f	f = f + 1	1	1	C,DC,N,OV,Z
		INC f,WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
40	INC2	INC2 f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2 f,WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2 Ws,Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
41	IOR	IOR f	f = f .IOR. WREG	1	1	N,Z
		IOR f,WREG	WREG = f .IOR. WREG	1	1	N,Z
		IOR #lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N,Z
42	LAC	LAC Wso,#Slit4,Acc	Load Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
43	LNK	LNK #lit14	Link Frame Pointer	1	1	None
44	LSR	LSR f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR f,WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR Ws,Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR Wb,Wns,Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
45	MAC	MAC Wm*Wn,Acc,Wx,Wxd,Wy,Wyd, AWB	Multiply and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB
		MAC Wm*Wm,Acc,Wx,Wxd,Wy,Wyd	Square and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB
46	MOV	MOV f,Wn	Move f to Wn	1	1	None
		MOV f	Move f to f	1	1	N,Z
		MOV f,WREG	Move f to WREG	1	1	None
		MOV #lit16,Wn	Move 16-bit Literal to Wn	1	1	None
		MOV.b #lit8,Wn	Move 8-bit Literal to Wn	1	1	None
		MOV Wn,f	Move Wn to f	1	1	None
		MOV Wso,Wdo	Move Ws to Wd	1	1	None
		MOV WREG,f	Move WREG to f	1	1	None
		MOV.D Wns,Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D Ws,Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
47	MOVSAC	MOVSAC Acc,Wx,Wxd,Wy,Wyd,AWB	Prefetch and Store Accumulator	1	1	None

TABLE 24-11: ELECTRICAL CHARACTERISTICS: BOR

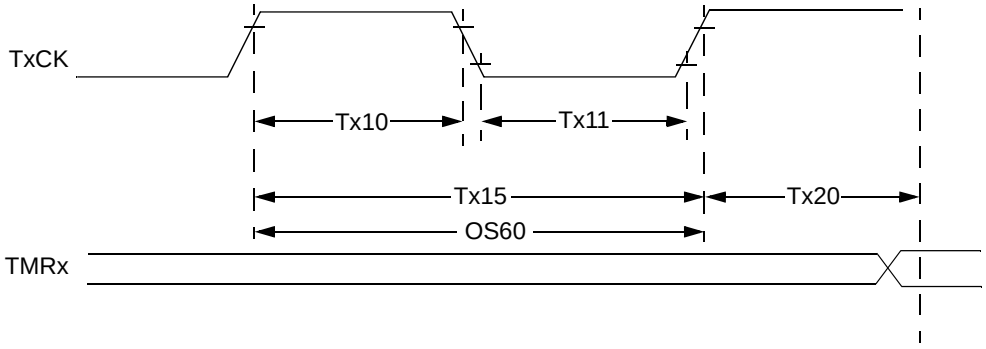
DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min(1)**	**Typ**	**Max**	**Units**	**Conditions**
BO10	VBOR	BOR Event on VDD Transition High-to-Low BOR Event is Tied to VDD Core Voltage Decrease	2.55	—	2.79	V	See **Note 2**

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: The device will operate as normal until the VDDMIN threshold is reached.

3: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested but not characterized. All device analog modules such as the ADC, etc., will function but with degraded performance below VDDMIN.

FIGURE 24-5: TIMER1, 2 AND 3 EXTERNAL CLOCK TIMING CHARACTERISTICS



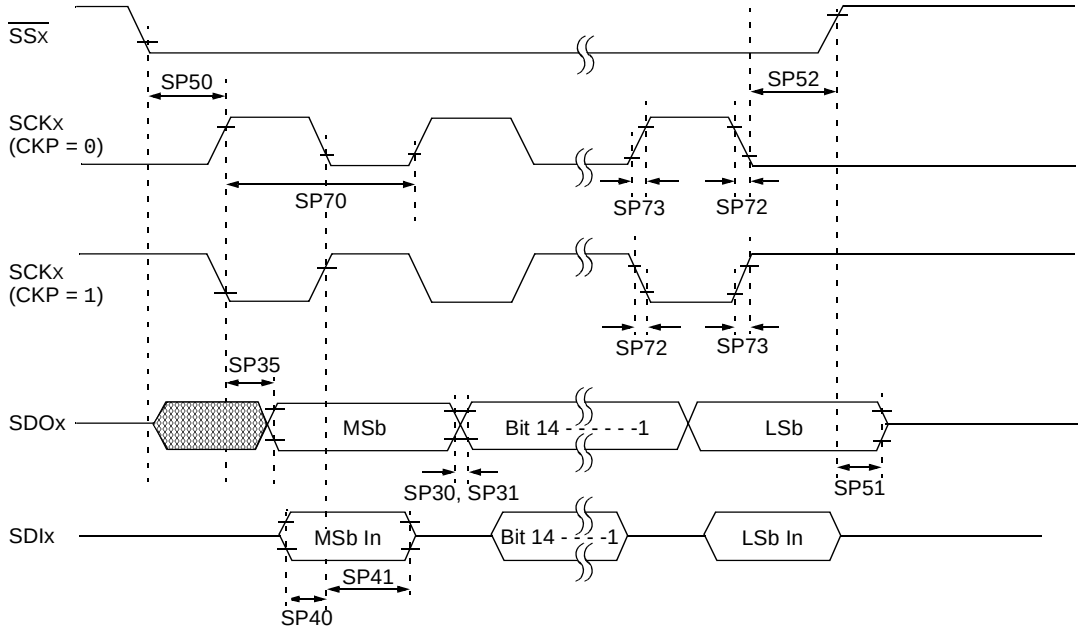
Note: Refer to Figure 24-1 for load conditions.

TABLE 24-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS(1)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TA10	TTXH	T1CK High Time	Synchronous, no prescaler	TCY + 20	—	—	ns	Must also meet Parameter TA15, N = Prescale value (1, 8, 64, 256)
			Synchronous, with prescaler	(TCY + 20)/N	—	—	ns	
			Asynchronous	20	—	—	ns	
TA11	TTXL	T1CK Low Time	Synchronous, no prescaler	TCY + 20	—	—	ns	Must also meet Parameter TA15, N = Prescale value (1, 8, 64, 256)
			Synchronous, with prescaler	(TCY + 20)/N	—	—	ns	
			Asynchronous	20	—	—	ns	
TA15	TTXP	T1CK Input Period	Synchronous, no prescaler	2 TCY + 40	—	—	ns	
			Synchronous, with prescaler	Greater of: 40 ns or (2 TCY + 40)/N	—	—	—	N = Prescale value (1, 8, 64, 256)
			Asynchronous	40	—	—	ns	
OS60	FT1	T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON<1>))		DC	—	50	kHz	
TA20	TCKEXTMRL	Delay from External T1CK Clock Edge to Timer Increment		0.75 TCY + 40	—	1.75 TCY + 40	—	

Note 1: Timer1 is a Type A timer.

FIGURE 24-18: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 24-1 for load conditions.

TABLE 25-6: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
HD130	EP	Cell Endurance	10,000	—	—	E/W	-40°C to +150°C(2)
HD134	TRETD	Characteristic Retention	20	—	—	Year	1000 E/W cycles or less and no other specifications are violated

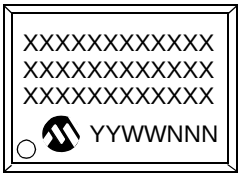
Note 1: These parameters are assured by design, but are not characterized or tested in manufacturing.

2: Programming of the Flash memory is not allowed above +125°C.

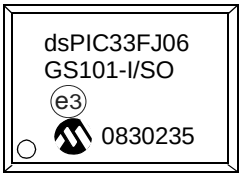
28.0 PACKAGING INFORMATION

28.1 Package Marking Information

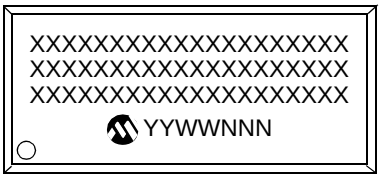
18-Lead SOIC (.300”)



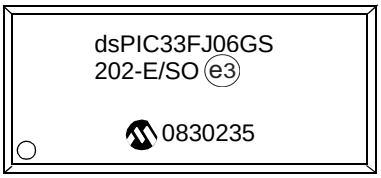
Example



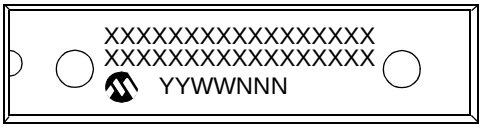
28-Lead SOIC



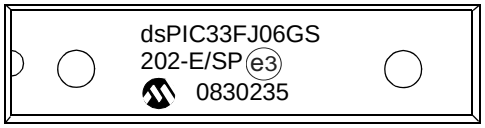
Example



28-Lead SPDIP



Example



28-Lead QFN-S

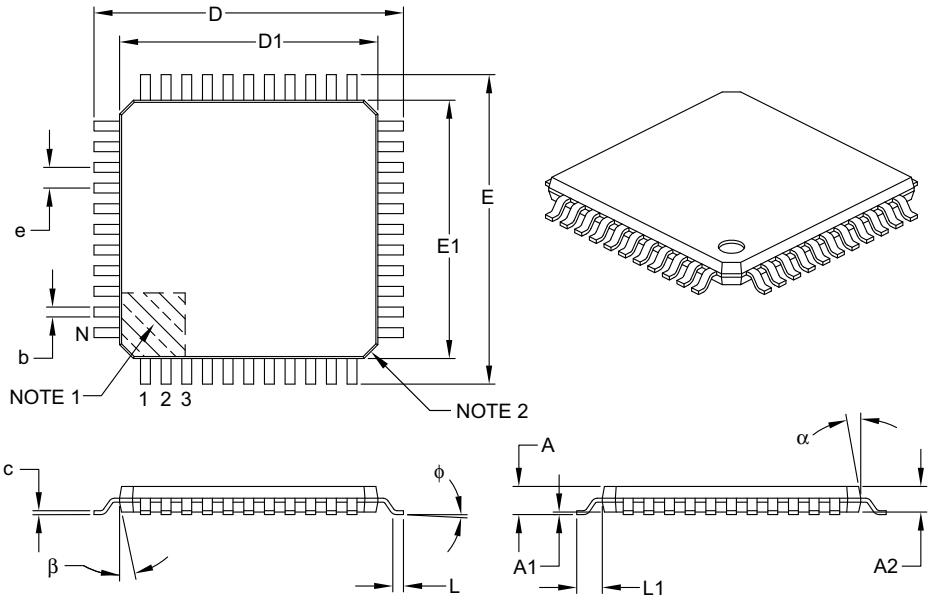
Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: If the full Microchip part number cannot be marked on one line, it is carried over to the next line, thus limiting the number of available characters for customer-specific information.

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 7.0 "Oscillator Configuration"	Removed the first sentence of the third clock source item (External Clock) in **Section 7.1.1 "System Clock sources"** Updated the default bit values for DOZE and FRCDIV in the Clock Divisor Register (see Register 7-2).
Section 8.0 "Power-Saving Features"	Added the following six registers: • **"PMD1: Peripheral Module Disable Control Register 1"** • **"PMD2: Peripheral Module Disable Control Register 2"** • **"PMD3: Peripheral Module Disable Control Register 3"** • **"PMD4: Peripheral Module Disable Control Register 4"** • **"PMD6: Peripheral Module Disable Control Register 6"** • **"PMD7: Peripheral Module Disable Control Register 7"**
Section 9.0 "I/O Ports"	Added paragraph and Table 9-1 to **Section 9.1.1 "Open-Drain Configuration"**, which provides details on I/O pins and their functionality. Removed 9.1.2 "5V Tolerance". Updated MUX range and removed virtual pin details in Figure 9-2. Updated PWM Input Name descriptions in Table 9-1. Added **Section 9.4.2.3 "Virtual Pins"**. Updated bit values in all Peripheral Pin Select Input Registers (see Register 9-1 through Register 9-14). Updated bit name information for Peripheral Pin Select Output Registers RPOR16 and RPOR17 (see Register 9-30 and Register 9-31). Added the following two registers: • **"RPOR16: Peripheral Pin Select Output Register 16"** • **"RPOR17: Peripheral Pin Select Output Register 17"** Removed the following sections: • 9.4.2 "Available Peripherals" • 9.4.3.2 "Virtual Input Pins" • 9.4.3.4 "Peripheral Mapping" • 9.4.5 "Considerations for Peripheral Pin Selection" (and all subsections)
Section 14.0 "High-Speed PWM"	Added Note 1 (remappable pin reference) to Figure 14-1. Added Note 2 (Duty Cycle resolution) to PWM Master Duty Cycle Register (Register 14-5), PWM Generator Duty Cycle Register (Register 14-7), and PWM Secondary Duty Cycle Register (Register 14-8). Added Note 2 and Note 3 and updated bit information for CLSRC and FLTSRC in the PWM Fault Current-Limit Control Register (Register 14-15).
Section 15.0 "Serial Peripheral Interface (SPI)"	Removed the following sections, which are now available in the related section of the dsPIC33F/PIC24H Family Reference Manual: • 15.1 "Interrupts" • 15.2 "Receive Operations" • 15.3 "Transmit Operations" • 15.4 "SPI Setup" (retained Figure 15-1: SPI Module Block Diagram)

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 16.0 “Inter-Integrated Circuit (I^2C™)”	Removed the following sections, which are now available in the related section of the dsPIC33F/PIC24H Family Reference Manual: • 16.3 “I^2C Interrupts” • 16.4 “Baud Rate Generator” (retained Figure 16-1: I^2C Block Diagram) • 16.5 “I^2C Module Addresses • 16.6 “Slave Address Masking” • 16.7 “IPMI Support” • 16.8 “General Call Address Support” • 16.9 “Automatic Clock Stretch” • 16.10 “Software Controlled Clock Stretching (STREN = 1)” • 16.11 “Slope Control” • 16.12 “Clock Arbitration” • 16.13 “Multi-Master Communication, Bus Collision, and Bus Arbitration
Section 17.0 “Universal Asynchronous Receiver Transmitter (UART)”	Removed the following sections, which are now available in the related section of the dsPIC33F/PIC24H Family Reference Manual: • 17.1 “UART Baud Rate Generator” • 17.2 “Transmitting in 8-bit Data Mode • 17.3 “Transmitting in 9-bit Data Mode • 17.4 “Break and Sync Transmit Sequence” • 17.5 “Receiving in 8-bit or 9-bit Data Mode” • 17.6 “Flow Control Using $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins” • 17.7 “Infrared Support” Removed IrDA references and Note 1, and updated the bit and bit value descriptions for UTXINV (UxSTA<14>) in the UARTx Status and Control Register (see Register 17-2).
Section 18.0 “High-Speed 10-bit Analog-to-Digital Converter (ADC)”	Updated bit value information for Analog-to-Digital Control Register (see Register 18-1). Updated TRGSRC6 bit value for Timer1 period match in the Analog-to-Digital Convert Pair Control Register 3 (see Register 18-8).

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 23.0 "Electrical Characteristics"	Updated Typ values for Thermal Packaging Characteristics (Table 23-3). Removed Typ value for DC Temperature and Voltage Specifications Parameter DC12 (Table 23-4). Updated all Typ values and conditions for DC Characteristics: Operating Current (I_{DD}), updated last sentence in Note 2 (Table 23-5). Updated all Typ values for DC Characteristics: Idle Current (I_{IDLE}) (see Table 23-6). Updated all Typ values for DC Characteristics: Power Down Current (I_{PD}) (see Table 23-7). Updated all Typ values for DC Characteristics: Doze Current (I_{DOZE}) (see Table 23-8). Added Note 4 (reference to new table containing digital-only and analog pin information, as well as Current Sink/Source capabilities) in the I/O Pin Input Specifications (Table 23-9). Updated Max value for BOR electrical characteristics Parameter BO10 (see Table 23-11). Swapped Min and Typ values for Program Memory Parameters D136 and D137 (Table 23-12). Updated Typ values for Internal RC Accuracy Parameter F20 and added Extended temperature range to table heading (see Table 23-19). Removed all values for Reset, Watchdog Timer, Oscillator Start-up Timer, and Power-up Timer Parameter SY20 and updated conditions, which now refers to **Section 20.4 "Watchdog Timer (WDT)"** and LPRC Parameter F21a (see Table 23-22). Added specifications to High-Speed PWM Module Timing Requirements for Tap Delay (Table 23-29). Updated Min and Max values for 10-bit High-Speed Analog-to-Digital Module Parameters AD01 and AD11 (see Table 23-36). Updated Max value and unit of measure for DAC AC Specification (see Table 23-40).