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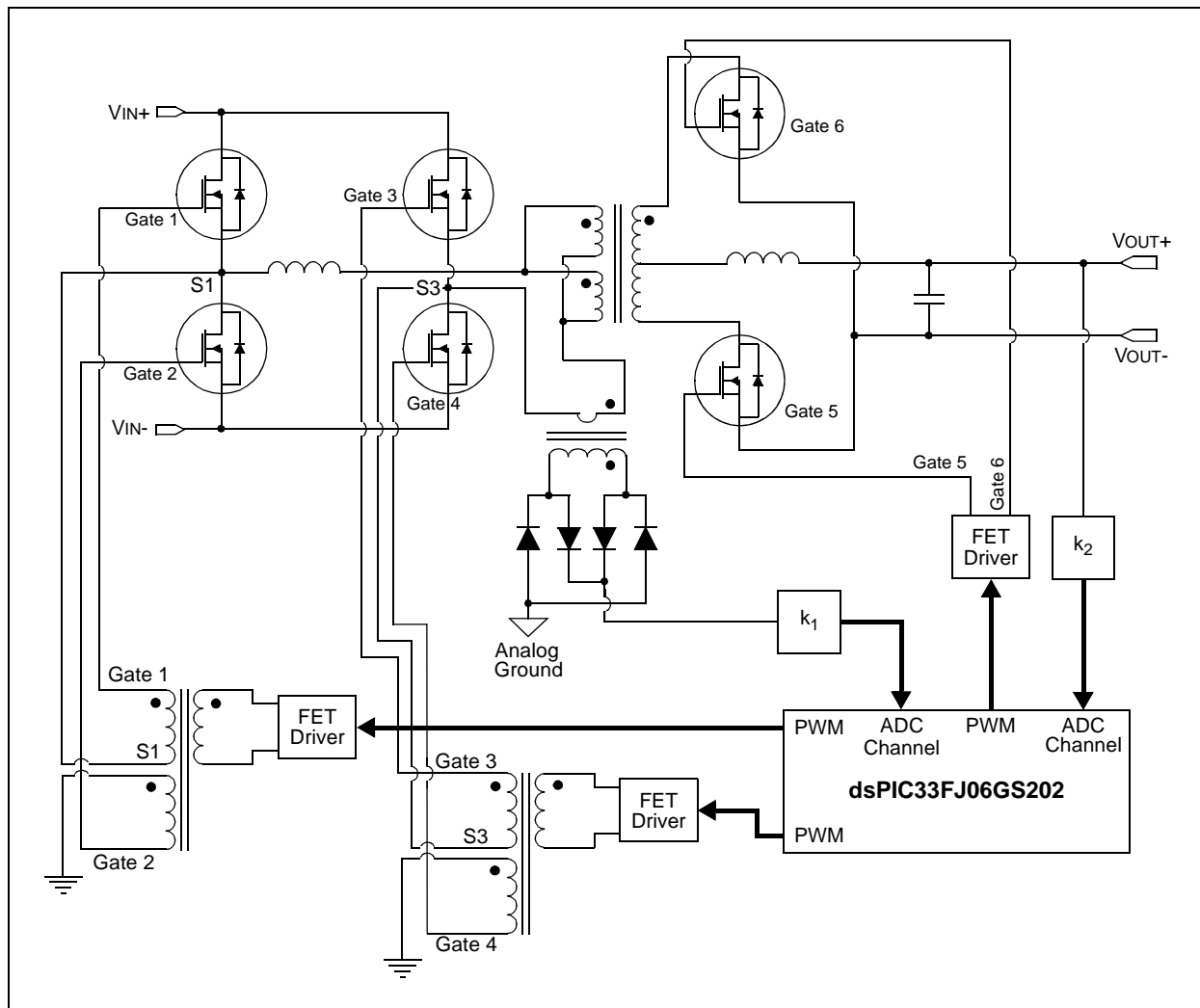
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gs402-e-mm

FIGURE 2-10: PHASE-SHIFTED FULL-BRIDGE CONVERTER



dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

FIGURE 3-3: DSP ENGINE BLOCK DIAGRAM

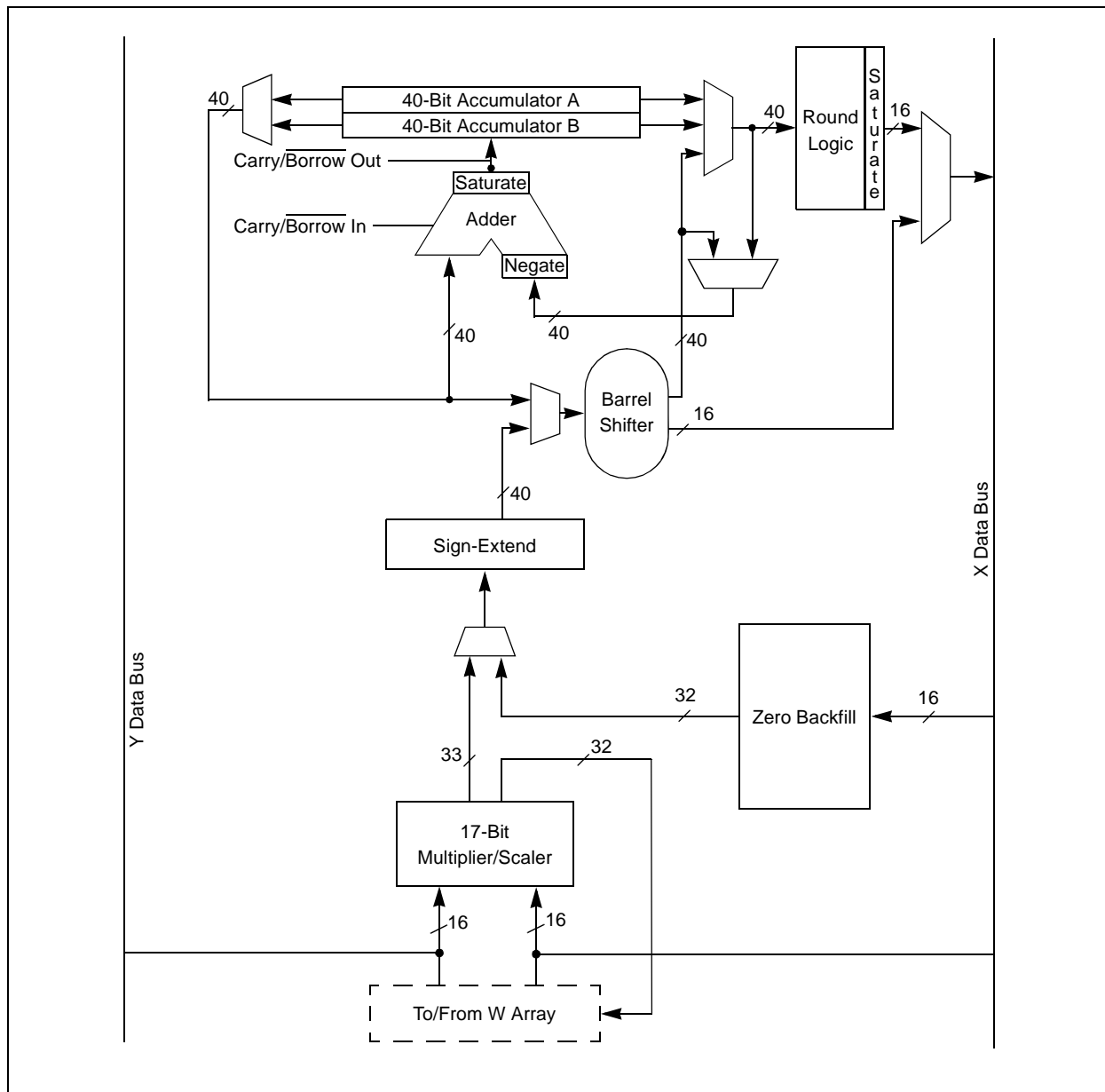


TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33FJ06GS102 DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFail	—	0000
INTCON2	0082	ALTVT	DISI	—	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	—	ADIF	U1TXIF	U1RXIF	SP1IF	SP1EIF	—	T2IF	—	—	—	T1IF	OC1IF	—	INT0IF	0000
IFS1	0086	—	—	INT2IF	—	—	—	—	—	—	—	—	INT1IF	CNIF	—	MI2C1IF	SI2C1IF	0000
IFS3	008A	—	—	—	—	—	—	PSEMIF	—	—	—	—	—	—	—	—	—	0000
IFS4	008C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIF	—	0000
IFS5	008E	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	0090	ADCP1IF	ADCP0IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS7	0092	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP2IF	0000
IEC0	0094	—	—	ADIE	U1TXIE	U1RXIE	SP1IE	SP1EIE	—	T2IE	—	—	—	T1IE	OC1IE	—	INT0IE	0000
IEC1	0096	—	—	INT2IE	—	—	—	—	—	—	—	—	INT1IE	CNIE	—	MI2C1IE	SI2C1IE	0000
IEC3	009A	—	—	—	—	—	—	PSEMIE	—	—	—	—	—	—	—	—	—	0000
IEC4	009C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIE	—	0000
IEC5	009E	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	00A0	ADCP1IE	ADCP0IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC7	00A2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP2IE	0000
IPC0	00A4	—	T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0	—	—	—	—	—	INT0IP2	INT0IP1	INT0IP0	4404
IPC1	00A6	—	T2IP2	T2IP1	T2IP0	—	—	—	—	—	—	—	—	—	—	—	—	4000
IPC2	00A8	—	U1RXIP2	U1RXIP2	U1RXIP0	—	SP1IP2	SP1IP1	SP1IP0	—	SP1EIP2	SP1EIP1	SP1EIP0	—	—	—	—	4440
IPC3	00AA	—	—	—	—	—	—	—	—	—	ADIP2	ADIP1	ADIP0	—	U1TXIP2	U1TXIP1	U1TXIP0	0044
IPC4	00AC	—	CNIP2	CNIP1	CNIP0	—	—	—	—	—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0	4044
IPC5	00AE	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0	0004
IPC7	00B2	—	—	—	—	—	—	—	—	—	INT2IP2	INT2IP1	INT2IP0	—	—	—	—	0040
IPC14	00C0	—	—	—	—	—	—	—	—	—	PSEMIP2	PSEMIP1	PSEMIP0	—	—	—	—	0040
IPC16	00C4	—	—	—	—	—	—	—	—	—	U1EIP2	U1EIP1	U1EIP0	—	—	—	—	0040
IPC23	00D2	—	PWM2IP2	PWM2IP1	PWM2IP0	—	PWM1IP2	PWM1IP1	PWM1IP0	—	—	—	—	—	—	—	—	4400
IPC27	00DA	—	ADCP1IP2	ADCP1IP1	ADCP1IP0	—	ADCP0IP2	ADCP0IP1	ADCP0IP0	—	—	—	—	—	—	—	—	4400
IPC28	00DC	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP2IP2	ADCP2IP1	ADCP2IP0	0004
INTTREG	00E0	—	—	—	—	ILR3	ILR2	ILR1	ILR0	—	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

6.2 Power-on Reset (POR)

A Power-on Reset (POR) circuit ensures the device is reset from power-on. The POR circuit is active until VDD crosses the VPOR threshold and the delay, TPOR, has elapsed. The delay, TPOR, ensures the internal device bias circuits become stable.

The device supply voltage characteristics must meet the specified starting voltage and rise rate requirements to generate the POR. Refer to **Section 24.0 “Electrical Characteristics”** for details.

The POR status (POR) bit in the Reset Control (RCON<0>) register is set to indicate the Power-on Reset.

6.2.1 Brown-out Reset (BOR) and Power-up Timer (PWRT)

The on-chip regulator has a Brown-out Reset (BOR) circuit that resets the device when the VDD is too low ($VDD < V_{BOR}$) for proper device operation. The BOR circuit keeps the device in Reset until VDD crosses the

VBOR threshold and the delay, TBOR, has elapsed. The delay, TBOR, ensures the voltage regulator output becomes stable.

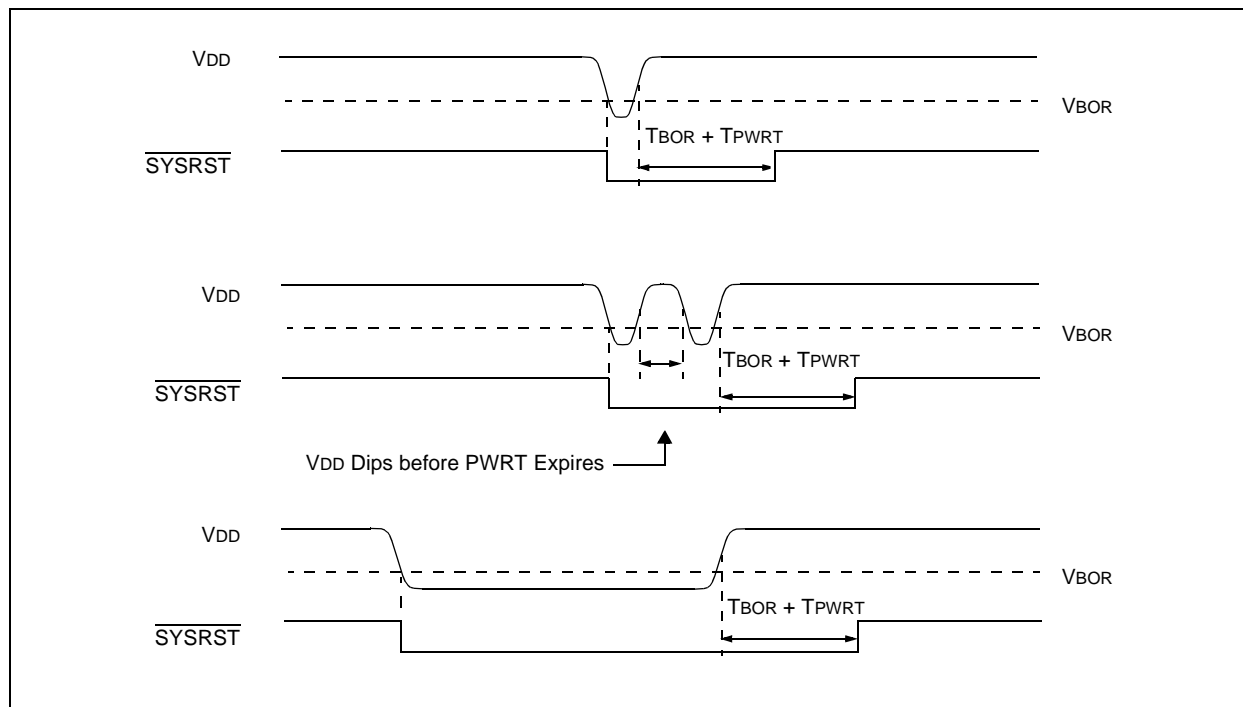
The BOR status (BOR) bit in the Reset Control (RCON<1>) register is set to indicate the Brown-out Reset.

The device will not run at full speed after a BOR as the VDD should rise to acceptable levels for full-speed operation. The PWRT provides power-up time delay (TPWRT) to ensure that the system power supplies have stabilized at the appropriate levels for full-speed operation before the SYSRST is released.

The Power-up Timer Delay (TPWRT) is programmed by the Power-on Reset Timer Value Select (FPWRT<2:0>) bits in the FPOR Configuration (FPOR<2:0>) register, which provides eight settings (from 0 ms to 128 ms). Refer to **Section 21.0 “Special Features”** for further details.

Figure 6-3 shows the typical brown-out scenarios. The Reset delay (TBOR + TPWRT) is initiated each time VDD rises above the VBOR trip point.

FIGURE 6-3: BROWN-OUT SITUATIONS



dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 7-14: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	PSEMIE	—
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9 **PSEMIE:** PWM Special Event Match Interrupt Enable bit

1 = Interrupt request enabled

0 = Interrupt request not enabled

bit 8-0 **Unimplemented:** Read as '0'

REGISTER 7-15: IEC4: INTERRUPT ENABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	U1EIE	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-2 **Unimplemented:** Read as '0'

bit 1 **U1EIE:** UART1 Error Interrupt Enable bit

1 = Interrupt request enabled

0 = Interrupt request not enabled

bit 0 **Unimplemented:** Read as '0'

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 7-17: IEC6: INTERRUPT ENABLE CONTROL REGISTER 6

R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
ADCP1IE	ADCP0IE	—	—	—	—	AC4IE	AC3IE
bit 15						bit 8	

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
AC2IE	—	—	—	—	—	PWM4IE	PWM3IE
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ADCP1IE:** ADC Pair 1 Conversion Done Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

bit 14 **ADCP0IE:** ADC Pair 0 Conversion Done Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

bit 13-10 **Unimplemented:** Read as '0'

bit 9 **AC4IE:** Analog Comparator 4 Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

bit 8 **AC3IE:** Analog Comparator 3 Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

bit 7 **AC2IE:** Analog Comparator 2 Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

bit 6-2 **Unimplemented:** Read as '0'

bit 1 **PWM4IE:** PWM4 Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

bit 0 **PWM3IE:** PWM3 Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 7-21: IPC2: INTERRUPT PRIORITY CONTROL REGISTER 2

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI1EIP2	SPI1EIP1	SPI1EIP0	—	T3IP2	T3IP1	T3IP0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **Unimplemented:** Read as '0'
- bit 14-12 **U1RXIP<2:0>:** UART1 Receiver Interrupt Priority bits
 111 = Interrupt is Priority 7 (highest priority interrupt)
 •
 •
 •
 001 = Interrupt is Priority 1
 000 = Interrupt source is disabled
- bit 11 **Unimplemented:** Read as '0'
- bit 10-8 **SPI1IP<2:0>:** SPI1 Event Interrupt Priority bits
 111 = Interrupt is Priority 7 (highest priority interrupt)
 •
 •
 •
 001 = Interrupt is Priority 1
 000 = Interrupt source is disabled
- bit 7 **Unimplemented:** Read as '0'
- bit 6-4 **SPI1EIP<2:0>:** SPI1 Error Interrupt Priority bits
 111 = Interrupt is Priority 7 (highest priority interrupt)
 •
 •
 •
 001 = Interrupt is Priority 1
 000 = Interrupt source is disabled
- bit 3 **Unimplemented:** Read as '0'
- bit 2-0 **T3IP<2:0>:** Timer3 Interrupt Priority bits
 111 = Interrupt is Priority 7 (highest priority interrupt)
 •
 •
 •
 001 = Interrupt is Priority 1
 000 = Interrupt source is disabled

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 7-24: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-3

Unimplemented: Read as '0'

bit 2-0

INT1IP<2:0>: External Interrupt 1 Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

REGISTER 7-25: IPC7: INTERRUPT PRIORITY CONTROL REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	INT2IP2	INT2IP1	INT2IP0	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7

Unimplemented: Read as '0'

bit 6-4

INT2IP<2:0>: External Interrupt 2 Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3-0

Unimplemented: Read as '0'

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 9-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	—	—	—	—	CMPMD	—	—
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **CMPMD:** Analog Comparator Module Disable bit

1 = Analog comparator module is disabled

0 = Analog comparator module is enabled

bit 9-0 **Unimplemented:** Read as '0'

REGISTER 9-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
—	—	—	—	REFOMD	—	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **REFOMD:** Reference Clock Generator Module Disable bit

1 = Reference clock generator module is disabled

0 = Reference clock generator module is enabled

bit 2-0 **Unimplemented:** Read as '0'

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

10.0 I/O PORTS

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “I/O Ports” (DS70193) in the “dsPIC33F/PIC24H Family Reference Manual”, which is available on Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

All of the device pins (except VDD, VSS, MCLR and OSC1/CLKI) are shared among the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

10.1 Parallel I/O (PIO) Ports

Generally a parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port

has ownership of the output data and control signals of the I/O pin. The logic also prevents “loop through”, in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 10-1 shows how ports are shared with other peripherals and the associated I/O pin to which they are connected.

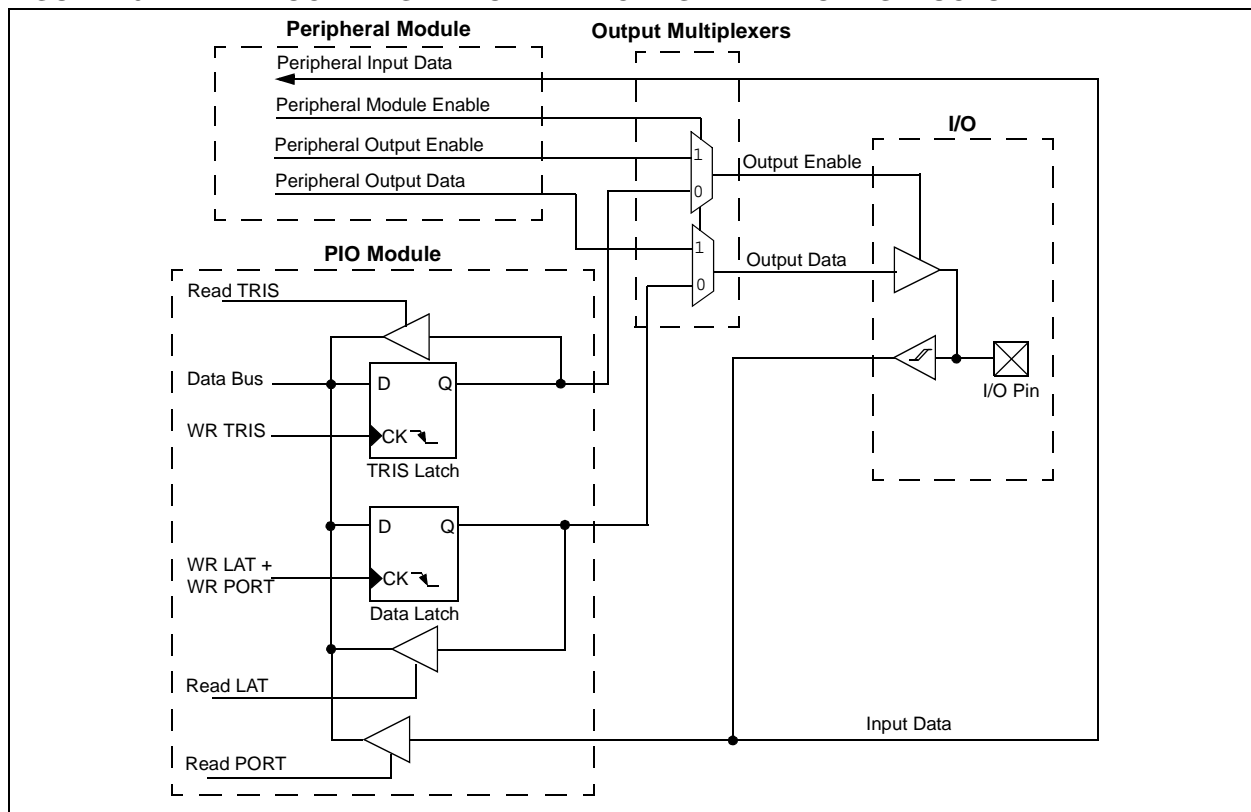
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have three registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is ‘1’, then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers and the port pin will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

FIGURE 10-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 16-3: SPIxCON2: SPIx CONTROL REGISTER 2

R/W-0		R/W-0		R/W-0		U-0		U-0		U-0		U-0		U-0			
FRMEN		SPIFSD		FRMPOL		—		—		—		—		—			
bit 15														bit 8			
U-0				U-0		U-0		U-0		U-0		U-0		R/W-0		U-0	
—				—		—		—		—		—		FRMDLY		—	
bit 7														bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **FRMEN:** Framed SPIx Support bit
1 = Framed SPIx support is enabled (\overline{SSx} pin used as frame sync pulse input/output)
0 = Framed SPIx support is disabled
- bit 14 **SPIFSD:** SPIx Frame Sync Pulse Direction Control bit
1 = Frame sync pulse input (slave)
0 = Frame sync pulse output (master)
- bit 13 **FRMPOL:** Frame Sync Pulse Polarity bit
1 = Frame sync pulse is active-high
0 = Frame sync pulse is active-low
- bit 12-2 **Unimplemented:** Read as '0'
- bit 1 **FRMDLY:** Frame Sync Pulse Edge Select bit
1 = Frame sync pulse coincides with first bit clock
0 = Frame sync pulse precedes first bit clock
- bit 0 **Unimplemented:** This bit must not be set to '1' by the user application

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

NOTES:

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 19-1: ADON: ANALOG-TO-DIGITAL CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0
ADON	—	ADSIDL	SLOWCLK ⁽¹⁾	—	GSWTRG	—	FORM ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-1	R/W-1
EIE ⁽¹⁾	ORDER ^(1,2)	SEQSAMP ^(1,2)	ASYNCAMP ⁽¹⁾	—	ADCS2 ⁽¹⁾	ADCS1 ⁽¹⁾	ADCS0 ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **ADON:** Analog-to-Digital Operating Mode bit
 1 = Analog-to-Digital Converter (ADC) module is operating
 0 = ADC Converter is off
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **ADSIDL:** ADC Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12 **SLOWCLK:** Enable The Slow Clock Divider bit⁽¹⁾
 1 = ADC is clocked by the auxiliary PLL (ACLK)
 0 = ADC is clock by the primary PLL (Fvco)
- bit 11 **Unimplemented:** Read as '0'
- bit 10 **GSWTRG:** Global Software Trigger bit
 When this bit is set by the user, it will trigger conversions if selected by the TRGSRC<4:0> bits in the ADCPCx registers. This bit must be cleared by the user prior to initiating another global trigger (i.e., this bit is not auto-clearing).
- bit 9 **Unimplemented:** Read as '0'
- bit 8 **FORM:** Data Output Format bit⁽¹⁾
 1 = Fractional (DOUT = dddd dddd dd00 0000)
 0 = Integer (DOUT = 0000 00dd dddd dddd)
- bit 7 **EIE:** Early Interrupt Enable bit⁽¹⁾
 1 = Interrupt is generated after first conversion is completed
 0 = Interrupt is generated after second conversion is completed
- bit 6 **ORDER:** Conversion Order bit^(1,2)
 1 = Odd numbered analog input is converted first, followed by conversion of even numbered input
 0 = Even numbered analog input is converted first, followed by conversion of odd numbered input
- bit 5 **SEQSAMP:** Sequential Sample Enable bit^(1,2)
 1 = Shared Sample-and-Hold (S&H) circuit is sampled at the start of the second conversion if ORDER = 0. If ORDER = 1, then the shared S&H is sampled at the start of the first conversion.
 0 = Shared S&H is sampled at the same time the dedicated S&H is sampled if the shared S&H is not currently busy with an existing conversion process. If the shared S&H is busy at the time the dedicated S&H is sampled, then the shared S&H will sample at the start of the new conversion cycle.

Note 1: These control bits can only be changed while ADC is disabled (ADON = 0).

2: These bits are only available on devices with one SAR.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 19-6: ADCPC1: ANALOG-TO-DIGITAL CONVERT PAIR CONTROL REGISTER 1 (CONTINUED)

bit 12-8	<p>TRGSRC3<4:0>: Trigger 3 Source Selection bits⁽¹⁾ Selects trigger source for conversion of Analog Channels AN7 and AN6. 11111 = Timer2 period match</p> <ul style="list-style-type: none">•••11011 = Reserved11010 = PWM Generator 4 current-limit ADC trigger11001 = PWM Generator 3 current-limit ADC trigger11000 = PWM Generator 2 current-limit ADC trigger10111 = PWM Generator 1 current-limit ADC trigger10110 = Reserved•••10010 = Reserved10001 = PWM Generator 4 secondary trigger is selected10000 = PWM Generator 3 secondary trigger is selected01111 = PWM Generator 2 secondary trigger is selected01110 = PWM Generator 1 secondary trigger is selected01101 = Reserved01100 = Timer1 period match•••01000 = Reserved00111 = PWM Generator 4 primary trigger is selected00110 = PWM Generator 3 primary trigger is selected00101 = PWM Generator 2 primary trigger is selected00100 = PWM Generator 1 primary trigger is selected00011 = PWM Special Event Trigger is selected00010 = Global software trigger is selected00001 = Individual software trigger is selected00000 = No conversion is enabled
bit 7	<p>IRQEN2: Interrupt Request Enable 2 bit⁽²⁾ 1 = Enables IRQ generation when requested conversion of Channels AN5 and AN4 is completed 0 = IRQ is not generated</p>
bit 6	<p>PEND2: Pending Conversion Status 2 bit⁽²⁾ 1 = Conversion of Channels AN5 and AN4 is pending; set when selected trigger is asserted 0 = Conversion is complete</p>
bit 5	<p>SWTRG2: Software Trigger 2 bit⁽²⁾ 1 = Starts conversion of AN5 and AN4 (if selected by the TRGSRCx bits)⁽³⁾ This bit is automatically cleared by hardware when the PEND2 bit is set. 0 = Conversion has not started</p>

Note 1: These bits are available in the dsPIC33FJ16GS402/404, dsPIC33FJ16GS504, dsPIC33FJ16GS502 and dsPIC33FJ06GS101 devices only.

2: These bits are available in the dsPIC33FJ16GS502, dsPIC33FJ16GS504, dsPIC33FJ06GS102, dsPIC33FJ06GS202 and dsPIC33FJ16GS402/404 devices only.

3: The trigger source must be set as a global software trigger prior to setting this bit to '1'. If other conversions are in progress, then the conversion will be performed when the conversion resources are available.

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21.0 SPECIAL FEATURES

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “dsPIC33F/PIC24H Family Reference Manual”. Please see the Microchip web site (www.microchip.com) for the latest “dsPIC33F/PIC24H Family Reference Manual” sections.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation
- Brown-out Reset (BOR)

21.1 Configuration Bits

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices provide nonvolatile memory implementations for device Configuration bits. Refer to “**Device Configuration**” (DS70194) in the “dsPIC33F/PIC24H Family Reference Manual” for more information on this implementation.

The Configuration bits can be programmed (read as ‘0’), or left unprogrammed (read as ‘1’), to select various device configurations. These bits are mapped starting at program memory location 0xF80000.

The individual Configuration bit descriptions for the Configuration registers are shown in Table 21-2.

Note that address, 0xF80000, is beyond the user program memory space. It belongs to the configuration memory space (0x800000-0xFFFFF), which can only be accessed using Table Reads and Table Writes.

The device Configuration register map is shown in Table 21-1.

TABLE 21-1: DEVICE CONFIGURATION REGISTER MAP

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xF80000	FBS	—	—	—	—	BSS2	BSS1	BSS0	BWRP
0xF80002	Reserved	—	—	—	—	—	—	—	—
0xF80004	FGS	—	—	—	—	—	GSS1	GSS0	GWRP
0xF80006	FOSCSEL	IESO	—	—	—	—	FNOSC2	FNOSC1	FNOSC0
0xF80008	FOSC	FCKSM1	FCKSM0	IOL1WAY	—	—	OSCIOFNC	POSCMD1	POSCMD0
0xF8000A	FWDT	FWDTEN	WINDIS	—	WDTPRE	WDTPOST3	WDTPOST2	WDTPOST1	WDTPOST0
0xF8000C	FPOR	—	—	—	—	Reserved ⁽²⁾	FPWRT2	FPWRT1	FPWRT0
0xF8000E	FICD	Reserved ⁽¹⁾		JTAGEN	—	—	—	ICS1	ICS0
0xF80010	FUID0	User Unit ID Byte 0							
0xF80012	FUID1	User Unit ID Byte 1							

Legend: — = unimplemented bit, read as ‘0’.

Note 1: These bits are reserved for use by development tools and must be programmed to ‘1’.

2: This bit reads the current programmed value.

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24.1 DC Characteristics

TABLE 24-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)	Temp Range (in °C)	Max MIPS
			dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04
—	3.0-3.6V ⁽¹⁾	-40°C to +85°C	40
—	3.0-3.6V ⁽¹⁾	-40°C to +125°C	40

Note 1: Overall functional device operation at $V_{BORMIN} < V_{DD} < V_{DDMIN}$ is tested but not characterized. All device analog modules such as the ADC, etc., will function but with degraded performance below V_{DDMIN} . Refer to Parameter BO10 in Table 24-11 for BOR values.

TABLE 24-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal chip power dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$ I/O Pin Power Dissipation: $I/O = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	$(T_J - T_A)/\theta_{JA}$			W

TABLE 24-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit	Notes
Package Thermal Resistance, 44-Pin QFN	θ_{JA}	28	—	°C/W	1
Package Thermal Resistance, 44-Pin TFQP	θ_{JA}	39	—	°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θ_{JA}	42	—	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θ_{JA}	47	—	°C/W	1
Package Thermal Resistance, 28-Pin QFN-S	θ_{JA}	34	—	°C/W	1
Package Thermal Resistance, 18-Pin SOIC	θ_{JA}	57	—	°C/W	1
Package Thermal Resistance, 44-Pin VTLA	θ_{JA}	25	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

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FIGURE 24-5: TIMER1, 2 AND 3 EXTERNAL CLOCK TIMING CHARACTERISTICS

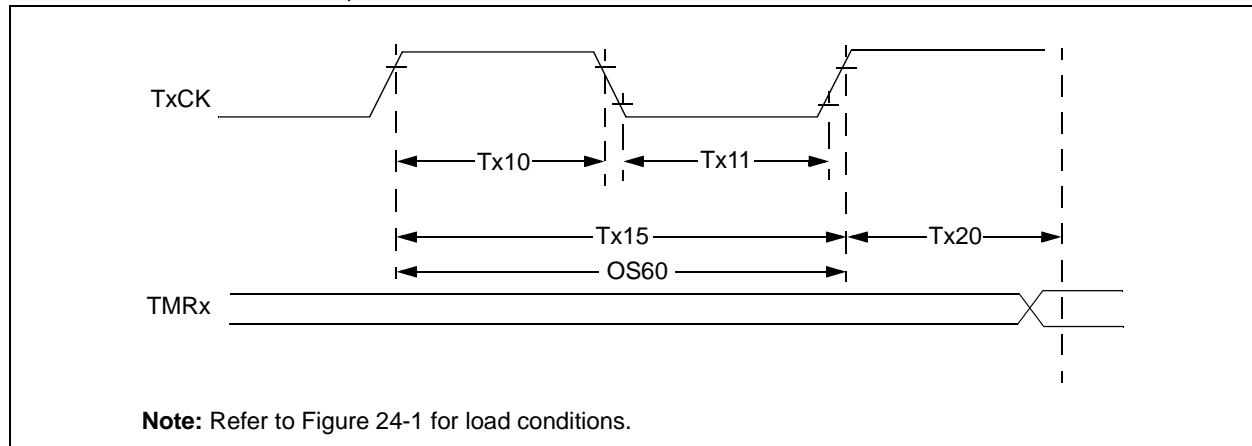


TABLE 24-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS⁽¹⁾

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended					
Param No.	Symbol	Characteristic		Min.	Typ.	Max.	Units	Conditions
TA10	T _{TXH}	T1CK High Time	Synchronous, no prescaler	T _{CY} + 20	—	—	ns	Must also meet Parameter TA15, N = Prescale value (1, 8, 64, 256)
			Synchronous, with prescaler	(T _{CY} + 20)/N	—	—	ns	
			Asynchronous	20	—	—	ns	
TA11	T _{TXL}	T1CK Low Time	Synchronous, no prescaler	T _{CY} + 20	—	—	ns	Must also meet Parameter TA15, N = Prescale value (1, 8, 64, 256)
			Synchronous, with prescaler	(T _{CY} + 20)/N	—	—	ns	
			Asynchronous	20	—	—	ns	
TA15	T _{TXP}	T1CK Input Period	Synchronous, no prescaler	2 T _{CY} + 40	—	—	ns	N = Prescale value (1, 8, 64, 256)
			Synchronous, with prescaler	Greater of: 40 ns or (2 T _{CY} + 40)/N	—	—	—	
			Asynchronous	40	—	—	ns	
OS60	F _{T1}	T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON<1>))		DC	—	50	kHz	
TA20	T _{CKEXTMRL}	Delay from External T1CK Clock Edge to Timer Increment		0.75 T _{CY} + 40	—	1.75 T _{CY} + 40	—	

Note 1: Timer1 is a Type A timer.

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TABLE 24-24: TIMER2 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic		Min.	Typ.	Max.	Units	Conditions
TB10	TtxH	T2CK High Time	Synchronous	Greater of: 20 ns or (Tcy + 20)/N	—	—	ns	Must also meet Parameter TB15, N = Prescale value (1, 8, 64, 256)
TB11	TtxL	T2CK Low Time	Synchronous	Greater of: 20 ns or (Tcy + 20)/N	—	—	ns	Must also meet Parameter TB15, N = Prescale value (1, 8, 64, 256)
TB15	TtxP	T2CK Input Period	Synchronous	Greater of: 40 ns or (2 Tcy + 40)/N	—	—	ns	N = Prescale value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from External T2CK Clock Edge to Timer Increment		0.75 Tcy + 40	—	1.75 Tcy + 40	ns	

TABLE 24-25: TIMER3 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
TC10	TtxH	T3CK High Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC11	TtxL	T3CK Low Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC15	TtxP	T3CK Input Period	Synchronous, with prescaler	2 Tcy + 40	—	—	ns	
TC20	TCKEXTMRL	Delay from External T3CK Clock Edge to Timer Increment		0.75 Tcy + 40	—	1.75 Tcy + 40	—	

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TABLE 24-35: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
SP70	TscP	Maximum SCKx Input Frequency	—	—	11	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx \uparrow or SCKx Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx} \uparrow$ to SDOx Output High-Impedance ⁽⁴⁾	10	—	50	ns	
SP52	Tsch2ssH, TscL2ssH	\overline{SSx} after SCKx Edge	1.5 Tcy + 40	—	—	ns	See Note 4
SP60	TssL2doV	SDOx Data Output Valid after \overline{SSx} Edge	—	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the Master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

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Revision C and D (March 2009)

This revision includes minor typographical and formatting changes throughout the data sheet text.

Global changes include:

- Changed all instances of OSC1 to OSC1 and OSC0 to OSC2
- Changed all instances of PGCx/EMUCx and PGDx/EMUDx (where x = 1, 2, or 3) to PGECx and PGEDx
- Changed all instances of VDDCORE and VDDCORE/VCAP to VCAP/VDDCORE

Other major changes are referenced by their respective section in the following table.

TABLE A-2: MAJOR SECTION UPDATES

Section Name	Update Description
“High-Performance, 16-bit Digital Signal Controllers”	Added “Application Examples” to list of features Updated all pin diagrams to denote the pin voltage tolerance (see “Pin Diagrams”). Added Note 2 to the 28-Pin QFN-S and 44-Pin QFN pin diagrams, which references pin connections to VSS.
Section 1.0 “Device Overview”	Added ACMP1-ACMP4 pin names and Peripheral Pin Select capability column to Pinout I/O Descriptions (see Table 1-1).
Section 2.0 “Guidelines for Getting Started with 16-bit Digital Signal Controllers”	Added new section to the data sheet that provides guidelines on getting started with 16-bit Digital Signal Controllers.
Section 3.0 “CPU”	Updated CPU Core Block Diagram with a connection from the DSP Engine to the Y Data Bus (see Figure 3-1). Vertically extended the X and Y Data Bus lines in the DSP Engine Block Diagram (see Figure 3-3).
Section 4.0 “Memory Organization”	Updated Reset value for ADCON in Table 4-25. Removed reference to dsPIC33FJ06GS102 devices in the PMD Register Map and updated bit definitions for PMD1 and PMD6, and removed PMD7 (see Table 4-43). Added a new PMD Register Map, which references dsPIC33FJ06GS102 devices (see Table 4-44). Updated RAM stack address and SPLIM values in the third paragraph of Section 4.2.6 “Software Stack” Removed Section 4.2.7 “Data Ram Protection Feature” .
Section 5.0 “Flash Program Memory”	Updated Section 5.3 “Programming Operations” with programming time formula.