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#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gs402-e-sp

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## 3.0 CPU

- Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "CPU" (DS70204) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for DSP. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented varies from device to device. A singlecycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/ X04 devices have sixteen, 16-bit Working registers in the programmer's model. Each of the Working registers can serve as a data, address or address offset register. The sixteenth Working register (W15) operates as a software Stack Pointer (SP) for interrupts and calls.

There are two classes of instruction in the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/ X04 devices: MCU and DSP. These two instruction classes are seamlessly integrated into a single CPU. The instruction set includes many addressing modes and is designed for optimum C compiler efficiency. For most instructions, the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 is capable of executing a data (or program data) memory read, a Working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.

A block diagram of the CPU is shown in Figure 3-1, and the programmer's model is shown in Figure 3-2.

## 3.1 Data Addressing Overview

The data space can be addressed as 32K words or 64 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear data space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device-specific.

Overhead-free circular buffers (Modulo Addressing mode) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. Furthermore, the X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page (PSVPAG) register. The program-to-data space mapping feature allows any instruction access program space as if it were data space.

## 3.2 DSP Engine Overview

The DSP engine features a high-speed, 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bidirectional barrel shifter. The barrel shifter is capable of shifting a 40-bit value up to 16 bits, right or left, in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal realtime performance. The MAC instruction and other associated instructions can concurrently fetch two data operands from memory while multiplying two W registers and accumulating and optionally saturating the result in the same cycle. This instruction functionality requires that the RAM data space be split for these instructions and linear for all others. Data space partitioning is achieved in a transparent and flexible manner through dedicating certain Working registers to each address space.



### TABLE 4-14: INPUT CAPTURE REGISTER MAP FOR dsPIC33FJ16GSX02 AND dsPIC33FJ16GSX04

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IC1BUF	0140							Inpu	t Capture	1 Register								xxxx
IC1CON	0142	—	—	ICSIDL	_	_	—	_	_	ICTMR	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC2BUF	0144							Inpu	t Capture 2	2 Register								xxxx
IC2CON	0146	_	_	ICSIDL	—		_	—		ICTMR	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

### TABLE 4-15: OUTPUT COMPARE REGISTER MAP FOR dsPIC33FJ06GS101 AND dsPIC33FJ06GSX02

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1RS	0180		Output Compare 1 Secondary Register												xxxx			
OC1R	0182							Outpu	ut Compare	1 Register								xxxx
OC1CON	0184	—	_	OCSIDL	_	_	—	—	_	—	_	_	OCFLT	OCTSEL	OCM2	OCM1	OCM0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

#### TABLE 4-16: OUTPUT COMPARE REGISTER MAP FOR dsPIC33FJ16GSX02 AND dsPIC33FJ06GSX04

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1RS	0180							Output Co	mpare 1 Se	condary Re	egister							xxxx
OC1R	0182		Output Compare 1 Register xxx											xxxx				
OC1CON	0184	_	_	OCSIDL	_	_	_	_	_	_	_	_	OCFLT	OCTSEL	OCM2	OCM1	OCM0	0000
OC2RS	0186							Output Co	mpare 2 Se	condary Re	egister							xxxx
OC2R	0188		Output Compare 2 Register xxxx										xxxxx					
OC2CON	018A	_	-	OCSIDL	_	_	_	_	_	_		_	OCFLT	OCTSEL	OCM2	OCM1	OCM0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

### TABLE 4-17: HIGH-SPEED PWM REGISTER MAP

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTCON	0400	PTEN	_	PTSIDL	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	-	SYNCSRC1	SYNCSRC0	SEVTPS3	SEVTPS2	SEVTPS1	SEVTPS0	0000
PTCON2	0402	_	_	_	_	_	_	_	_	_	_	_	_	_	PCLKDIV2	PCLKDIV1	PCLKDIV0	0000
PTPER	0404									PTPER<15	:0>							FFF8
SEVTCMP	0406		SEVTCMP<15:3> 0000										0000					
MDC	040A		MDC<15:0> 0000															

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Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

#### 4.4.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. Address boundaries check for addresses equal to:

- The upper boundary addresses for incrementing buffers
- The lower boundary addresses for decrementing buffers

The address boundaries check for addresses less than or greater than the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes can, therefore, jump beyond boundaries and still be adjusted correctly.

Note: The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (such as [W7 + W2]) is used, Modulo Addressing correction is performed but the contents of the register remain unchanged.

## 4.5 Bit-Reversed Addressing

Bit-Reversed Addressing mode is intended to simplify data re-ordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

# 4.5.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing mode is enabled in any of these situations:

- BWM bits (W register selection) in the MODCON register are any value other than 15 (the stack cannot be accessed using Bit-Reversed Addressing)
- The BREN bit is set in the XBREV register
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment

If the length of a bit-reversed buffer is  $M = 2^N$  bytes, the last 'N' bits of the data buffer start address must be zeros.

XB<14:0> is the Bit-Reversed Address modifier, or 'pivot point,' which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

Note:	All bit-reversed EA calculations assume
	word-sized data (LSb of every EA is
	always clear). The XB value is scaled
	accordingly to generate compatible (byte)
	addresses.

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It will not function for any other addressing mode or for byte-sized data, and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XB), and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

Note:	Modulo	Address	sing a	ind B	it-Reversed
	Addressi	ng sho	ould n	not b	e enabled
	together.	If an a	oplicatio	on atte	empts to do
	so, Bit-R	leversed	Addres	ssing	will assume
	priority w	hen activ	ve for th	ne X W	AGU and X
	WAGU;	Modulo	Addres	ssing	will be dis-
	abled. H	lowever,	Modul	o Add	ressing wil
	continue	to function	on in th	e X R/	AGU.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV<15>) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.



### TABLE 4-49: BIT-REVERSED ADDRESS SEQUENCE (16-ENTRY)

		Norma	al Addres	SS			Bit-Rev	ersed Ac	ldress
A3	A2	A1	A0	Decimal	A3	A2	A1	A0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15

## 11.0 **TIMER1**

- Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70205) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer, which can serve as a time counter for the Real-Time Clock (RTC), or operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be operated from the low-power 32 kHz crystal oscillator available on the device
- Can be operated in Asynchronous Counter mode from an external clock source
- Optionally, the external clock input (T1CK) can be synchronized to the internal device clock and the clock synchronization is performed after the prescaler

The unique features of Timer1 allow it to be used for Real-Time Clock (RTC) applications. A block diagram of Timer1 is shown in Figure 11-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FcY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

The timer control bit settings for different operating modes are given in the Table 11-1.

<b>FABLE 11-1</b> :	TIMER MODE SETTINGS
---------------------	---------------------

Mode	TCS	TGATE	TSYNC
Timer	0	0	х
Gated Timer	0	1	х
Synchronous Counter	1	x	1
Asynchronous Counter	1	x	0

#### FIGURE 11-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



### REGISTER 15-4: SEVTCMP: PWM SPECIAL EVENT COMPARE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SEVTC	MP <15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	SE	EVTCMP <7:3>	•		—	—	—
bit 7							bit 0
Legend:							
R = Readable b	oit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-3 SEVTCMP<12:0>: Special Event Compare Count Value bits

bit 2-0 Unimplemented: Read as '0'

## **REGISTER 15-5:** MDC: PWM MASTER DUTY CYCLE REGISTER<sup>(1,2)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			MDC	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			MD	C<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 MDC<15:0>: Master PWM Duty Cycle Value bits

**Note 1:** The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0009, while the maximum pulse width generated corresponds to a value of Period – 0x0008.

2: As the duty cycle gets closer to 0% or 100% of the PWM period (0 ns-40 ns, depending on the mode of operation), the PWM duty cycle resolution will degrade from 1 LSB to 3 LSBs.

	REGISTER 15-10:	SPHASEX: PWMx SECONDARY PHASE-SHIFT REGISTER <sup>(1,2)</sup>
--	-----------------	---

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
SPHASEx<15:8>										
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	SPHASEx<7:0>									
bit 7							bit 0			
Legend:										
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'										
-n = Value at P	OR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown							

bit 15-0 SPHASEx<15:0>: Secondary Phase Offset for PWMxL Output Pin bits (used in Independent PWM mode only)

- **Note 1:** If PWMCONx<ITB> = 0, the following applies based on the mode of operation:
  - Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10); SPHASEx<15:0> = Not used
  - True Independent Output mode (IOCONx<PMOD> = 11); PHASEx<15:0> = Phase-shift value for PWMxL only
  - **2:** If PWMCONx<ITB> = 1, the following applies based on the mode of operation:
    - Complementary, Redundant and Push-Pull Output mode (IOCONx<PMOD> = 00, 01, or 10); SPHASEx<15:0> = Not used
    - True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11); PHASEx<15:0> = Independent Time Base period value for PWMxL only

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			PWMCA	\P<15:8> <sup>(1,2)</sup>			
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	U-0	U-0	U-0
	PW	/MCAP<7:3> <sup>(1,2</sup>	2)		—	—	—
bit 7							bit 0
Legend:							
R = Readable bit	= Readable bit W = Writable bit U = Unimplemented bit, read as '0'						
-n = Value at POR		'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown
L							

## REGISTER 15-19: PWMCAPx: PRIMARY PWMx TIME BASE CAPTURE REGISTER

bit 15-3 **PWMCAP<15:3>:** Captured PWM Time Base Value bits<sup>(1,2)</sup> The value in this register represents the captured PWM time base value when a leading edge is detected on the current-limit input.

bit 2-0 Unimplemented: Read as '0'

**Note 1:** The capture feature is only available on the primary output (PWMxH).

2: This feature is active only after LEB processing on the current-limit input signal is complete.

## 19.4 ADC Control Registers

The ADC module uses the following control and status registers:

- ADCON: Analog-to-Digital Control Register
- ADSTAT: Analog-to-Digital Status Register
- ADBASE: Analog-to-Digital Base Register(1,2)
- ADPCFG: Analog-to-Digital Port Configuration Register
- ADCPC0: Analog-to-Digital Convert Pair Control Register 0
- ADCPC1: Analog-to-Digital Convert Pair Control Register 1
- ADCPC2: Analog-to-Digital Convert Pair Control Register 2(1)
- ADCPC3: Analog-to-Digital Convert Pair Control Register 3(1)

The ADCON register controls the operation of the ADC module. The ADSTAT register displays the status of the conversion processes. The ADPCFG registers configure the port pins as analog inputs or as digital I/O. The ADCPCx registers control the triggering of the ADC conversions. See Register 19-1 through Register 19-8 for detailed bit configurations.

Note: A unique feature of the ADC module is its ability to sample inputs in an asynchronous manner. Individual Sample-and-Hold circuits can be triggered independently of each other.

## **REGISTER 19-3:** ADBASE: ANALOG-TO-DIGITAL BASE REGISTER<sup>(1,2)</sup>

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown				nown			
R = Readable I	bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
Legend:							
bit 7							bit 0
		/	ADBASE<7:1	>			—
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
bit 15							bit 8
			ADBAS	SE<15:8>			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

#### bit 15-1 ADBASE<15:1>: Analog-to-Digital Base bits

This register contains the base address of the user's ADC Interrupt Service Routine jump table. This register, when read, contains the sum of the ADBASE register contents and the encoded value of the PxRDY status bits.

The encoder logic provides the bit number of the highest priority PxRDY bits, where P0RDY is the highest priority and P6RDY is the lowest priority.

#### bit 0 Unimplemented: Read as '0'

- Note 1: The encoding results are shifted left two bits, so bits 1-0 of the result are always zero.
  - **2:** As an alternative to using the ADBASE register, the ADCP0-6 ADC Pair Conversion Complete interrupts can be used to invoke A to D conversion completion routines for individual ADC input pairs.

#### **REGISTER 19-4:** ADPCFG: ANALOG-TO-DIGITAL PORT CONFIGURATION REGISTER

11.0	11.0	11.0	11.0	DAMA	DAMA	DAMA	D/11/0
0-0	U-0	0-0	0-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—		PCFG<	:11:8> <sup>(1)</sup>	
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PCFG	<7:0> <sup>(1)</sup>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 Unimplemented: Read as '0'

bit 11-0 PCFG<11:0>: Analog-to-Digital Port Configuration Control bits<sup>(1)</sup>

1 = Port pin in Digital mode; port read input is enabled, Analog-to-Digital input multiplexer is connected to AVss

0 = Port pin in Analog mode; port read input is disabled, Analog-to-Digital samples the pin voltage

**Note 1:** Not all PCFGx bits are available on all devices. See Figure 19-1 through Figure 19-6 for the available analog pins (PCFGx = ANx, where x = 0-11).

Bit Field	Register	RTSP Effect	Description
BWRP	FBS	Immediate	Boot Segment Program Flash Write Protection bit
			1 = Boot segment can be written
			0 = Boot segment is write-protected
BSS<2:0>	FBS	Immediate	Boot Segment Program Flash Code Protection Size bits
			x11 = No boot program Flash segment
			Boot Space is 256 Instruction Words (except interrupt vectors):
			110 = Standard security; boot program Flash segment ends at
			010 = High security; boot program Flash segment ends at
			0x0003FE
			Boot Space is 768 Instruction Words (except interrupt vectors):
			101 = Standard security; boot program Flash segment ends at
			0x0007FE
			0x0007FE
			Boot Space is 1792 Instruction Words (except interrupt vectors):
			100 = Standard security; boot program Flash segment ends at
			0x000FFE
			000 = High security; boot program Flash segment ends at 0x000FFF
GSS<1:0>	FGS	Immediate	General Segment Code-Protect bits
	1.00	initiodiato	11 = User program memory is not code-protected
			10 = Standard security
			0x = High security
GWRP	FGS	Immediate	General Segment Write-Protect bit
			1 = User program memory is not write-protected
	FORCEL	Immodiate	0 = Osel program memory is white-protected
1230	FUSCSEL	Inneulate	1 - Start-up device with EPC, then automatically switch to the
			user-selected oscillator source when ready
			0 = Start-up device with user-selected oscillator source
FNOSC<2:0>	FOSCSEL	If clock switch	Initial Oscillator Source Selection bits
		is enabled,	111 = Internal Fast RC (FRC) Oscillator with Postscaler
		RISP effect	110 = Internal Fast RC (FRC) Oscillator with Divide-by-16
		device Reset;	101 = LPRC Oscillator 100 = Reserved
		otherwise,	011 = Primary (XT, HS, EC) Oscillator with PLL
		Immediate	010 = Primary (XT, HS, EC) Oscillator
			001 = Internal Fast RC (FRC) Oscillator with PLL
ECKSM-1.0	EOSC	Immodiato	Clock Switching Mode hite
	F030	mmediate	$1_{\rm X} = $ Clock switching is disabled. Fail-Safe Clock Monitor is disabled.
			01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
			00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	FOSC	Immediate	Peripheral Pin Select Configuration bit
			1 = Allows only one reconfiguration
	5000		0 = Allows multiple reconfigurations
OSCIOENC	FOSC	Immediate	USU2 Pin Function bit (except in X I and HS modes)
	1		

### TABLE 21-2: dsPIC33F CONFIGURATION BITS DESCRIPTION

## 21.2 On-Chip Voltage Regulator

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices power their core digital logic at a nominal 2.5V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. When the regulator is enabled, a low-ESR (less than 5 ohms) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 21-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 24-13 located in **Section 24.1 "DC Characteristics"**.

Note:	It is important for the low-ESR capacitor to
	be placed as close as possible to the VCAP
	pin.

On a POR, it takes approximately 20  $\mu$ s for the on-chip voltage regulator to generate an output voltage. During this time, designated as TSTARTUP, code execution is disabled. TSTARTUP is applied every time the device resumes operation after any power-down.

#### FIGURE 21-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR<sup>(1,2,3)</sup>



### 21.3 BOR: Brown-out Reset

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines, or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM = 100 is applied. The total delay in this case is TFSCM.

The BOR Status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

### FIGURE 24-8: OCx/PWMx MODULE TIMING CHARACTERISTICS



### TABLE 24-28: SIMPLE OCx/PWMx MODE TIMING REQUIREMENTS

AC CHAF	RACTERIS	Standard (unless of Operating	I Operatin otherwise g temperat	g Condition stated) cure -40°0 -40°0	ons: 3.0V C ≤ TA ≤ +8 C ≤ TA ≤ +1	<b>to 3.6V</b> 35°C for Industrial 125°C for Extended	
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min Typ Max Units Conditions				
OC15	Tfd	Fault Input to PWMx I/O Change	—	_	Tcy + 20	ns	
OC20	TFLT	Fault Input Pulse Width	TCY + 20	_		ns	

**Note 1:** These parameters are characterized but not tested in manufacturing.

# TABLE 24-36:SPIX SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING<br/>REQUIREMENTS

AC CHARACTERISTICS			Standard Op (unless othe Operating ter	erating rwise sta nperatur	Conditio ated) e -40° -40°	ONS: 3.0 C ≤ TA ≤ C ≤ TA ≤	<b>/ to 3.6V</b> +85°C for Industrial +125°C for Extended
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Min Typ <sup>(2)</sup>		Units	Conditions
SP70	TscP	Maximum SCKx Input Frequency	_		15	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	_			ns	See Parameter DO32 and <b>Note 4</b>
SP73	TscR	SCKx Input Rise Time	—	_	_	ns	See Parameter DO31 and <b>Note 4</b>
SP30	TdoF	SDOx Data Output Fall Time	—	—	_	ns	See Parameter DO32 and <b>Note 4</b>
SP31	TdoR	SDOx Data Output Rise Time	—	—	_	ns	See Parameter DO31 and <b>Note 4</b>
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30		_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30		_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx $\uparrow$ or SCKx Input	120	Ι	_	ns	
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance	10	—	50	ns	See Note 4
SP52	TscH2ssH TscL2ssH	SSx after SCKx Edge	1.5 TCY + 40	—	_	ns	See Note 4

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the Master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

# TABLE 24-37:SPIX SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING<br/>REQUIREMENTS

AC CHARACTERISTICS			Standard Op (unless othe Operating ter	erating rwise sta mperatur	Conditio ated) e -40° -40°	<b>DNS: 3.0</b> C ≤ TA ≤ C ≤ TA ≤	<b>V to 3.6V</b> +85°C for Industrial +125°C for Extended
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Min Typ <sup>(2)</sup>		Units	Conditions
SP70	TscP	Maximum SCKx Input Frequency	_		11	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	_			ns	See Parameter DO32 and <b>Note 4</b>
SP73	TscR	SCKx Input Rise Time	_		_	ns	See Parameter DO31 and <b>Note 4</b>
SP30	TdoF	SDOx Data Output Fall Time	_		—	ns	See Parameter DO32 and <b>Note 4</b>
SP31	TdoR	SDOx Data Output Rise Time	_		_	ns	See Parameter DO31 and <b>Note 4</b>
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_	_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx $\uparrow$ or SCKx Input	120	Ι	_	ns	
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance	10	—	50	ns	See Note 4
SP52	TscH2ssH TscL2ssH	SSx after SCKx Edge	1.5 TCY + 40	—	_	ns	See Note 4

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the Master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



## RECOMMENDED LAND PATTERN

	N		S	
Dimension	MIN	NOM	MAX	
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	С		9.40	
Contact Pad Width (X28)	Х			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

Section Name	Update Description
Section 7.0 "Oscillator Configuration"	Removed the first sentence of the third clock source item (External Clock) in Section 7.1.1 "System Clock sources"
	Updated the default bit values for DOZE and FRCDIV in the Clock Divisor Register (see Register 7-2).
Section 8.0 "Power-Saving	Added the following six registers:
Features"	"PMD1: Peripheral Module Disable Control Register 1"
	"PMD2: Peripheral Module Disable Control Register 2"
	"PMD3: Peripheral Module Disable Control Register 3"
	"PMD4: Peripheral Module Disable Control Register 4"
	"PMD6: Peripheral Module Disable Control Register 6"
	• "PMD7: Peripheral Module Disable Control Register 7"
Section 9.0 "I/O Ports"	Added paragraph and Table 9-1 to <b>Section 9.1.1 "Open-Drain</b> <b>Configuration"</b> , which provides details on I/O pins and their functionality.
	Removed 9.1.2 "5V Tolerance".
	Updated MUX range and removed virtual pin details in Figure 9-2.
	Updated PWM Input Name descriptions in Table 9-1.
	Added Section 9.4.2.3 "Virtual Pins".
	Updated bit values in all Peripheral Pin Select Input Registers (see Register 9-1 through Register 9-14).
	Updated bit name information for Peripheral Pin Select Output Registers RPOR16 and RPOR17 (see Register 9-30 and Register 9-31).
	Added the following two registers:
	"RPOR16: Peripheral Pin Select Output Register 16"     "BBOD17: Berinkeral Bin Select Output Register 17"
	• RPORT/: Peripheral Pill Select Output Register 17
	Removed the following sections:
	9.4.2 "Available Peripherals"
	9.4.3.2 "Virtual Input Pins"
	• 9.4.3.4 "Peripheral Mapping"
	• 9.4.5 "Considerations for Peripheral Pin Selection" (and all subsections)
Section 14.0 "High-Speed PWM"	Added Note 1 (remappable pin reference) to Figure 14-1.
	Added Note 2 (Duty Cycle resolution) to PWM Master Duty Cycle Register
	(Register 14-5), PWM Generator Duty Cycle Register (Register 14-7), and PWM Secondary Duty Cycle Register (Register 14-8).
	Added Note 2 and Note 3 and updated bit information for CLSRC and FLTSRC in the PWM Fault Current-Limit Control Register (Register 14-15).
Section 15.0 "Serial Peripheral Interface (SPI)"	Removed the following sections, which are now available in the related section of the dsPIC33F/PIC24H Family Reference Manual:
	• 15.1 "Interrupts"
	15.2 "Receive Operations"
	15.3 "Transmit Operations"
	• 15.4 "SPI Setup" (retained Figure 15-1: SPI Module Block Diagram)

## TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)