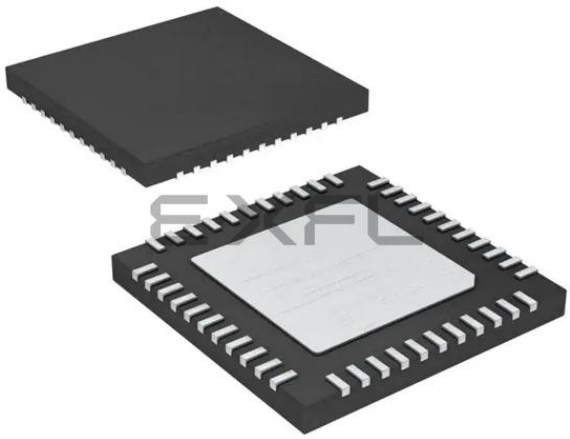
Microchip Technology - DSPIC33FJ16GS404-50I/ML Datasheet



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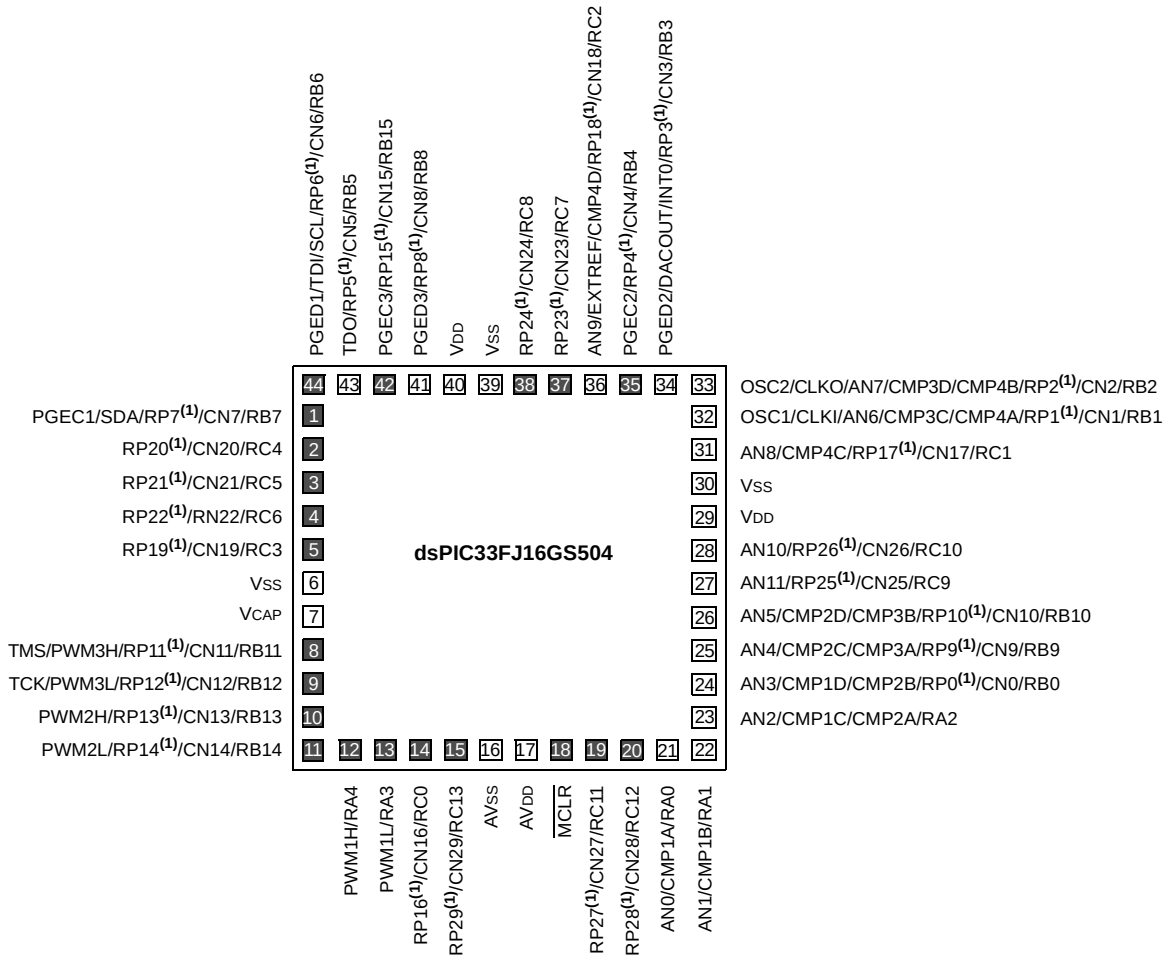
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	50 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gs404-50i-ml

Pin Diagrams (Continued)

44-Pin VTLA(2)

■ = Pins are up to 5V tolerant



Note 1: The RPn pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.

2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 1 **RND:** Rounding Mode Select bit
1 = Biased (conventional) rounding is enabled
0 = Unbiased (convergent) rounding is enabled

bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit
1 = Integer mode is enabled for DSP multiply ops
0 = Fractional mode is enabled for DSP multiply ops

Note 1: This bit will always read as '0'.
2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

FIGURE 4-4: DATA MEMORY MAP FOR dsPIC33FJ06GS202 DEVICE WITH 1-KBYTE RAM

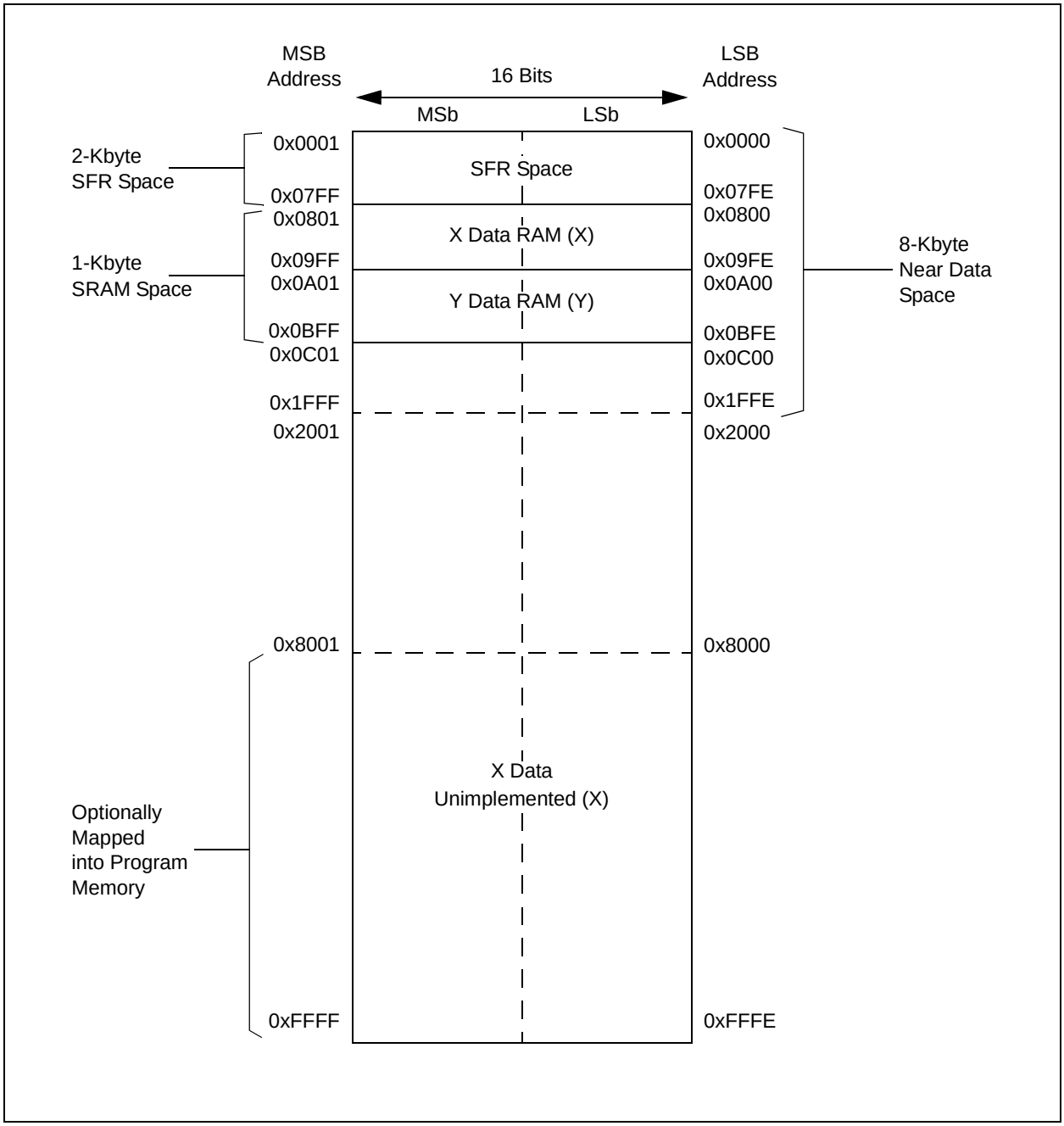
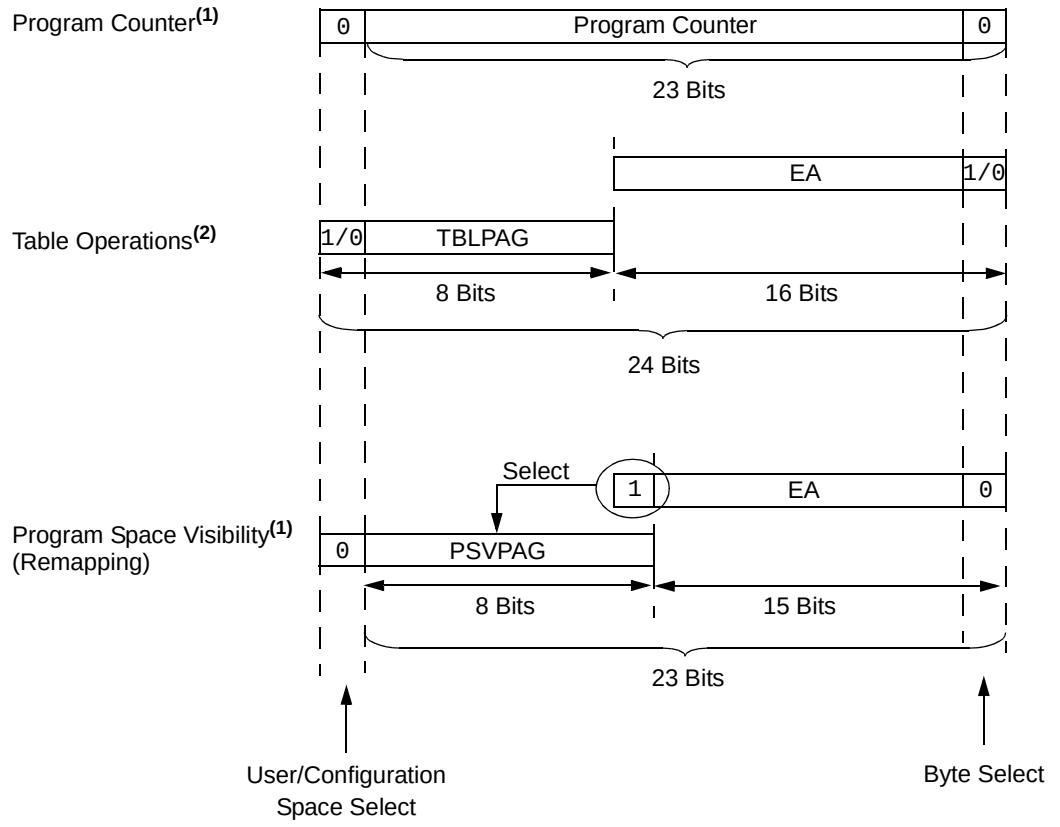


FIGURE 4-9: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



Note 1: The Least Significant bit (LSb) of program space addresses is always fixed as '0' to maintain word alignment of data in the program and data spaces.

2: Table operations are not required to be word-aligned. Table Read operations are permitted in the configuration memory space.

7.0 INTERRUPT CONTROLLER

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Interrupts (Part IV)"** (DS70300) in the "*dsPIC33F/PIC24H Family Reference Manual*", which is available on the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 CPU. It has the following features:

- Up to eight processor exceptions and software traps
- Seven user-selectable priority levels
- Interrupt Vector Table (IVT) with up to 118 vectors
- A unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Alternate Interrupt Vector Table (AIVT) for debug support
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The Interrupt Vector Table (IVT) is shown in Figure 7-1. The IVT resides in program memory, starting at location 000004h. The IVT contains 126 vectors, consisting of eight nonmaskable trap vectors, plus up to 118 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit-wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 will take priority over interrupts at any other vector address.

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices implement up to 35 unique interrupts and 4 non-maskable traps. These are summarized in Table 7-1.

7.1.1 ALTERNATE INTERRUPT VECTOR TABLE

The Alternate Interrupt Vector Table (AIVT) is located after the IVT, as shown in Figure 7-1. Access to the AIVT is provided by the ALTIVT control bit (INTCON2<15>). If the ALTIVT bit is set, all interrupt and exception processes use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors.

The AIVT supports debugging by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time. If the AIVT is not needed, the AIVT should be programmed with the same addresses used in the IVT.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices clear their registers in response to a Reset, which forces the PC to zero. The Digital Signal Controller then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT and AIVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

REGISTER 7-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0 (CONTINUED)

bit 1 **IC1IF:** Input Capture Channel 1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **INT0IF:** External Interrupt 0 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 7-34: IPC29: INTERRUPT PRIORITY CONTROL REGISTER 29

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	ADCP6IP2	ADCP6IP1	ADCP6IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **ADCP6IP<2:0>:** ADC Pair 6 Conversion Done Interrupt 1 Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 7-35: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	ILR3	ILR2	ILR1	ILR0
bit 15							bit 8

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-8 **ILR<3:0>:** New CPU Interrupt Priority Level bits
1111 = CPU Interrupt Priority Level is 15
•
•
•
0001 = CPU Interrupt Priority Level is 1
0000 = CPU Interrupt Priority Level is 0

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **VECNUM<6:0>:** Vector Number of Pending Interrupt bits
0111111 = Interrupt vector pending is Number 135
•
•
•
0000001 = Interrupt vector pending is Number 9
0000000 = Interrupt vector pending is Number 8

REGISTER 9-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	—	—	—	—	CMPMD	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10 **CMPMD**: Analog Comparator Module Disable bit
1 = Analog comparator module is disabled
0 = Analog comparator module is enabled

bit 9-0 **Unimplemented:** Read as ‘0’

REGISTER 9-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
—	—	—	—	REFOMD	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3 **REFOMD**: Reference Clock Generator Module Disable bit
1 = Reference clock generator module is disabled
0 = Reference clock generator module is enabled

bit 2-0 **Unimplemented:** Read as ‘0’

10.2 Open-Drain Configuration

In addition to the PORTx, LATx and TRISx registers for data control, some digital-only port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (for example, 5V) on any desired 5V tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

Refer to **"Pin Diagrams"** for the available pins and their functionality.

10.3 Configuring Analog Port Pins

The ADPCFG and TRISx registers control the operation of the Analog-to-Digital (A/D) port pins. The port pins that are to function as analog inputs must have their corresponding TRISx bit set (input). If the TRISx bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The ADPCFG register has a default value of 0x0000; therefore, all pins that share ANx functions are analog (not digital) by default.

When the PORTx register is read, all pins configured as analog input channels will read as cleared (a low level).

Pins configured as digital inputs will not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

10.4 I/O Port Write/Read Timing

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a NOP. An example is shown in Example 10-1.

10.5 Input Change Notification

The Input Change Notification (ICN) function of the I/O ports allows the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Depending on the device pin count, up to 30 external signals (CNx pin) can be selected (enabled) for generating an interrupt request on a Change-of-State.

Four control registers are associated with the CN module. The CNEN1 and CNEN2 registers contain the interrupt enable control bits for each of the CN input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CN pin also has a weak pull-up connected to it. The pull-ups act as a current source connected to the pin, and eliminate the need for external resistors when the push button or keypad devices are connected. The pull-ups are enabled separately using the CNPU1 and CNPU2 registers, which contain the control bits for each of the CN pins. Setting any of the control bits enables the weak pull-ups for the corresponding pins.

Note:	Pull-ups on Change Notification pins should always be disabled when the port pin is configured as a digital output.

EQUATION 10-1: PORT WRITE/READ EXAMPLE

```
MOV   0xFF00, W0          ; Configure PORTB<15:8> as inputs
MOV   W0, TRISBB          ; and PORTB<7:0> as outputs
NOP                       ; Delay 1 cycle
BTSS  PORTB, #13          ; Next Instruction
```

NOTES:

FIGURE 19-4: ADC BLOCK DIAGRAM FOR dsPIC33FJ16GS402/404 DEVICES WITH ONE SAR

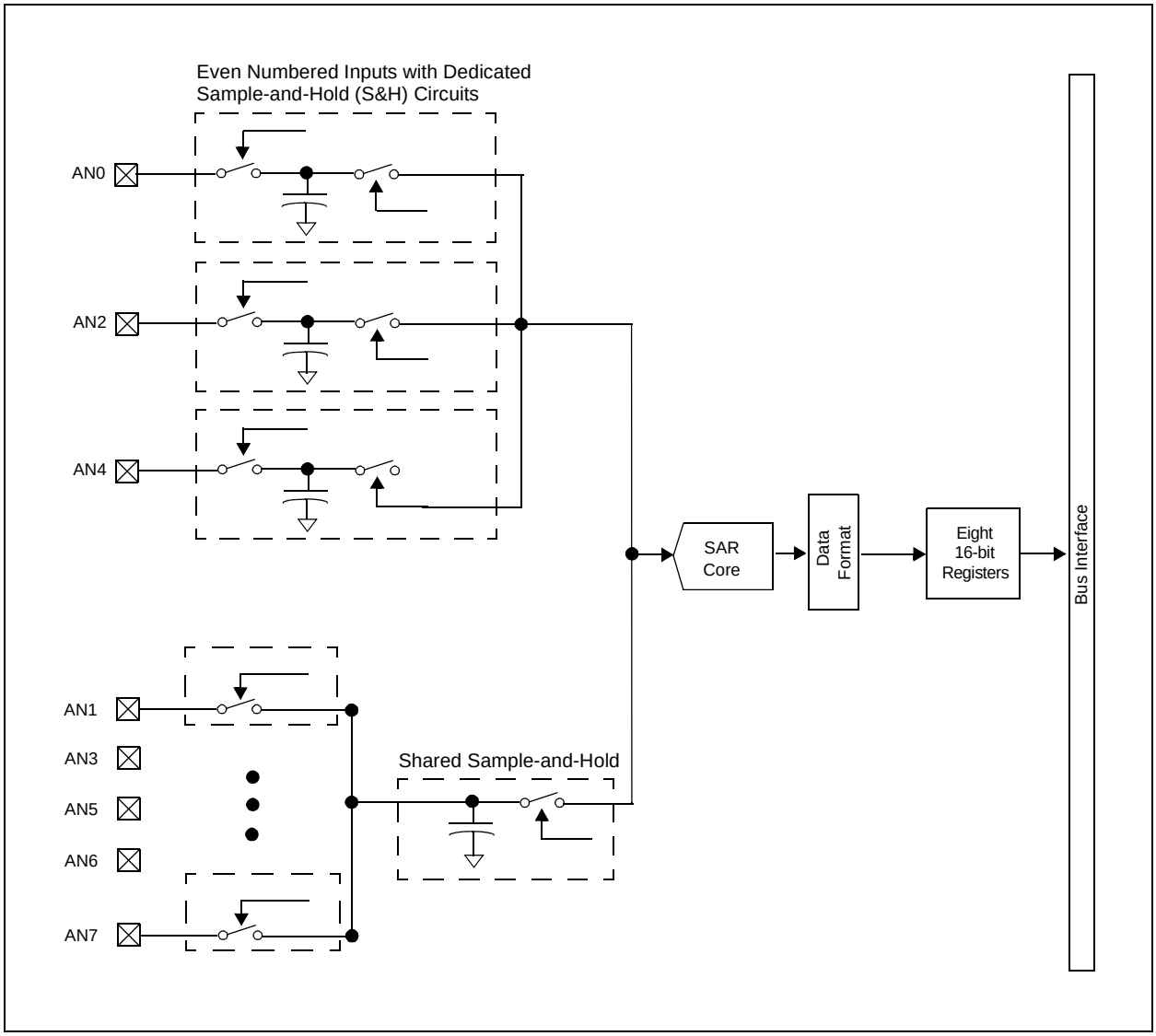
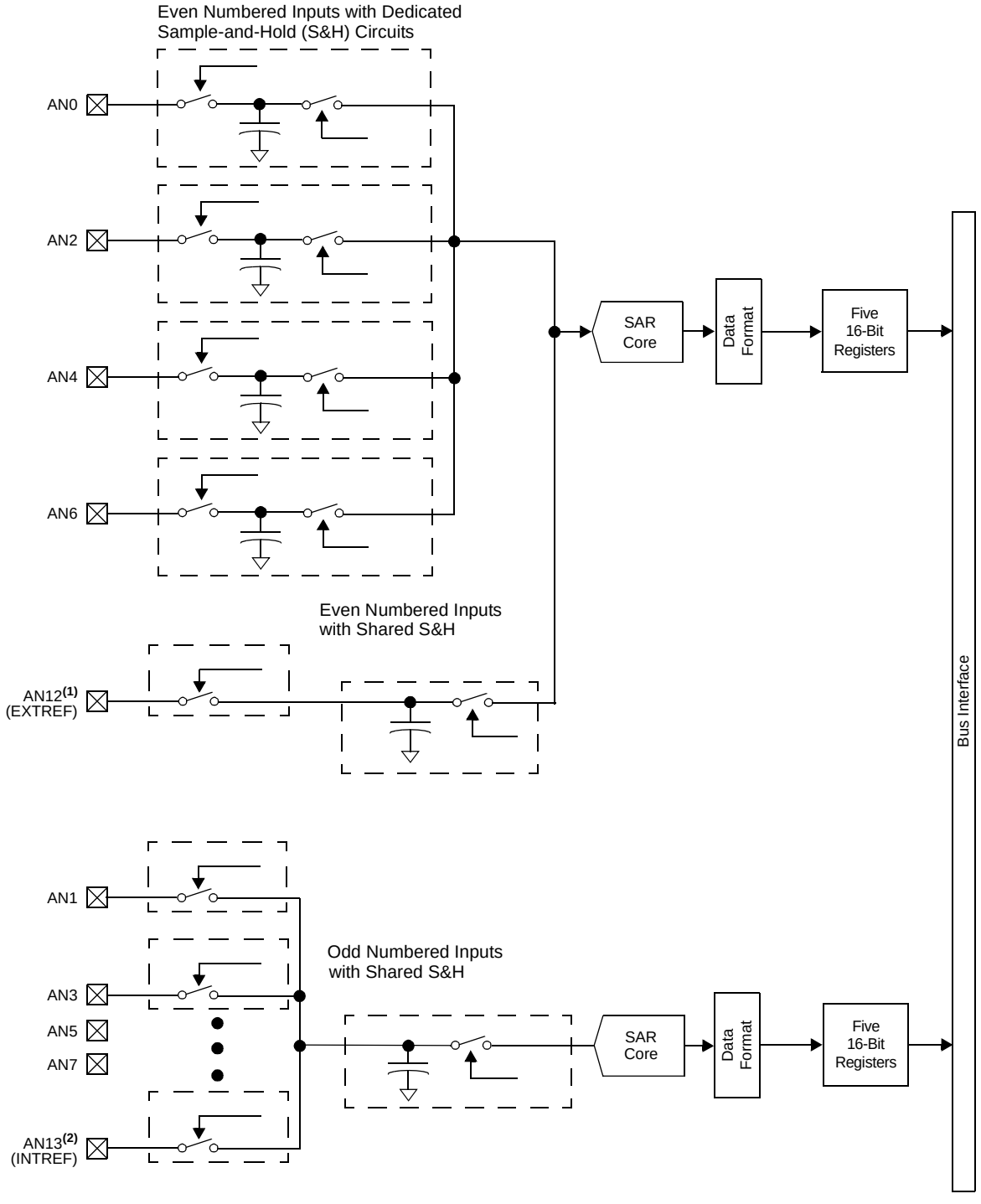


FIGURE 19-5: ADC BLOCK DIAGRAM FOR dsPIC33FJ16GS502 DEVICES WITH TWO SARS



Note 1: AN12 (EXTREF) is an internal analog input. To measure the voltage at AN12 (EXTREF), an analog comparator must be enabled and EXTREF must be selected as the comparator reference.

2: AN13 (INTREF) is an internal analog input and is not available on a pin.

REGISTER 19-5: ADCPC0: ANALOG-TO-DIGITAL CONVERT PAIR CONTROL REGISTER 0 (CONTINUED)

bit 4-0 **TRGSRC0<4:0>:** Trigger 0 Source Selection bits

Selects trigger source for conversion of Analog Channels AN1 and AN0.

11111 = Timer2 period match
•
•
•
11011 = Reserved
11010 = PWM Generator 4 current-limit ADC trigger
11001 = PWM Generator 3 current-limit ADC trigger
11000 = PWM Generator 2 current-limit ADC trigger
10111 = PWM Generator 1 current-limit ADC trigger
10110 = Reserved
•
•
•
10010 = Reserved
10001 = PWM Generator 4 secondary trigger is selected
10000 = PWM Generator 3 secondary trigger is selected
01111 = PWM Generator 2 secondary trigger is selected
01110 = PWM Generator 1 secondary trigger is selected
01101 = Reserved
01100 = Timer1 period match
•
•
•
01000 = Reserved
00111 = PWM Generator 4 primary trigger is selected
00110 = PWM Generator 3 primary trigger is selected
00101 = PWM Generator 2 primary trigger is selected
00100 = PWM Generator 1 primary trigger is selected
00011 = PWM Special Event Trigger is selected
00010 = Global software trigger is selected
00001 = Individual software trigger is selected
00000 = No conversion is enabled

Note 1: The trigger source must be set as a global software trigger prior to setting this bit to '1'. If other conversions are in progress, then the conversion will be performed when the conversion resources are available.

REGISTER 19-7: ADCPC2: ANALOG-TO-DIGITAL CONVERT PAIR CONTROL REGISTER 2(1) (CONTINUED)

bit 12-8 **TRGSRC5<4:0>:** Trigger 5 Source Selection bits

Selects trigger source for conversion of Analog Channels AN11 and AN10.
11111 = Timer2 period match
•
•
•
11011 = Reserved
11010 = PWM Generator 4 current-limit ADC trigger
11001 = PWM Generator 3 current-limit ADC trigger
11000 = PWM Generator 2 current-limit ADC trigger
10111 = PWM Generator 1 current-limit ADC trigger
10110 = Reserved
•
•
•
10010 = Reserved
10001 = PWM Generator 4 secondary trigger is selected
10000 = PWM Generator 3 secondary trigger is selected
01111 = PWM Generator 2 secondary trigger is selected
01110 = PWM Generator 1 secondary trigger is selected
01101 = Reserved
01100 = Timer1 period match
•
•
•
01000 = Reserved
00111 = PWM Generator 4 primary trigger is selected
00110 = PWM Generator 3 primary trigger is selected
00101 = PWM Generator 2 primary trigger is selected
00100 = PWM Generator 1 primary trigger is selected
00011 = PWM Special Event Trigger is selected
00010 = Global software trigger is selected
00001 = Individual software trigger is selected
00000 = No conversion is enabled

bit 7 **IRQEN4:** Interrupt Request Enable 4 bit

1 = Enables IRQ generation when requested conversion of Channels AN9 and AN8 is completed
0 = IRQ is not generated

bit 6 **PEND4:** Pending Conversion Status 4 bit

1 = Conversion of Channels AN9 and AN8 is pending; set when selected trigger is asserted
0 = Conversion is complete

bit 5 **SWTRG4:** Software Trigger 4 bit

1 = Starts conversion of AN9 and AN8 (if selected by the TRGSRCx bits)(2)
This bit is automatically cleared by hardware when the PEND4 bit is set.
0 = Conversion has not started

Note 1: This register is only implemented in the dsPIC33FJ16GS504 devices.

2: The trigger source must be set as a global software trigger prior to setting this bit to '1'. If other conversions are in progress, then the conversion will be performed when the conversion resources are available.

21.8 Code Protection and CodeGuard™ Security

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices offer the intermediate implementation of CodeGuard™ Security. CodeGuard Security enables multiple parties to securely share resources (memory, interrupts and peripherals) on a single chip. This feature helps protect individual Intellectual Property (IP) in collaborative system designs.

When coupled with software encryption libraries, CodeGuard™ Security can be used to securely update Flash even when multiple IPs reside on a single chip.

The code protection features are controlled by the Configuration registers: FBS and FGS.

Secure segment and RAM protection is not implemented in dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices.

Note:	Refer to **"CodeGuard™ Security"** (DS70199) for further information on CodeGuard Security usage, configuration and operation.

TABLE 21-3: CODE FLASH SECURITY SEGMENT SIZES FOR 6-Kbyte DEVICES

Configuration Bits	
BSS<2:0> = x11 **0K**	VS = 256 IW GS = 1792 IW 000000h 0001FEh 000200h 0003FEh 000400h 0007FEh 000800h 000FFEh 001000h 002BFEh
BSS<2:0> = x10 **256**	VS = 256 IW BS = 256 IW GS = 1536 IW 000000h 0001FEh 000200h 0003FEh 000400h 0007FEh 000800h 000FFEh 001000h 002BFEh
BSS<2:0> = x01 **768**	VS = 256 IW BS = 768 IW GS = 1024 IW 000000h 0001FEh 000200h 0003FEh 000400h 0007FEh 000800h 000FFEh 001000h 002BFEh
BSS<2:0> = x00 **1792**	VS = 256 IW BS = 1792 IW 000000h 0001FEh 000200h 0003FEh 000400h 0007FEh 000800h 000FFEh 001000h 002BFEh

TABLE 21-4: CODE FLASH SECURITY SEGMENT SIZES FOR 16-Kbyte DEVICES

Configuration Bits	
BSS<2:0> = x11 **0K**	VS = 256 IW GS = 5376 IW 000000h 0001FEh 000200h 0003FEh 000400h 0007FEh 000800h 000FFEh 001000h 002BFEh
BSS<2:0> = x10 **256**	VS = 256 IW BS = 256 IW GS = 5120 IW 000000h 0001FEh 000200h 0003FEh 000400h 0007FEh 000800h 000FFEh 001000h 002BFEh
BSS<2:0> = x01 **768**	VS = 256 IW BS = 768 IW GS = 4608 IW 000000h 0001FEh 000200h 0003FEh 000400h 0007FEh 000800h 000FFEh 001000h 002BFEh
BSS<2:0> = x00 **1792**	VS = 256 IW BS = 1792 IW GS = 3584 IW 000000h 0001FEh 000200h 0003FEh 000400h 0007FEh 000800h 000FFEh 001000h 002BFEh

TABLE 24-6: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
Idle Current (I_{IDLE}): Core Off Clock On Base Current(2)						
DC40d	48	—	mA	-40°C	3.3V	10 MIPS
DC40a	48	—	mA	+25°C		
DC40b	48	—	mA	+85°C		
DC40c	48	—	mA	+125°C		
DC41d	60	—	mA	-40°C	3.3V	16 MIPS(3)
DC41a	60	—	mA	+25°C		
DC41b	60	—	mA	+85°C		
DC41c	60	—	mA	+125°C		
DC42d	68	—	mA	-40°C	3.3V	20 MIPS(3)
DC42a	68	—	mA	+25°C		
DC42b	68	—	mA	+85°C		
DC42c	68	—	mA	+125°C		
DC43d	77	—	mA	-40°C	3.3V	30 MIPS(3)
DC43a	77	—	mA	+25°C		
DC43b	77	—	mA	+85°C		
DC43c	77	—	mA	+125°C		
DC44d	86	—	mA	-40°C	3.3V	40 MIPS
DC44a	86	—	mA	+25°C		
DC44b	86	—	mA	+85°C		
DC44c	86	—	mA	+125°C		

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

2: Base Idle current (I_{IDLE}) is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- JTAG is disabled

3: These parameters are characterized but not tested in manufacturing.

FIGURE 24-21: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

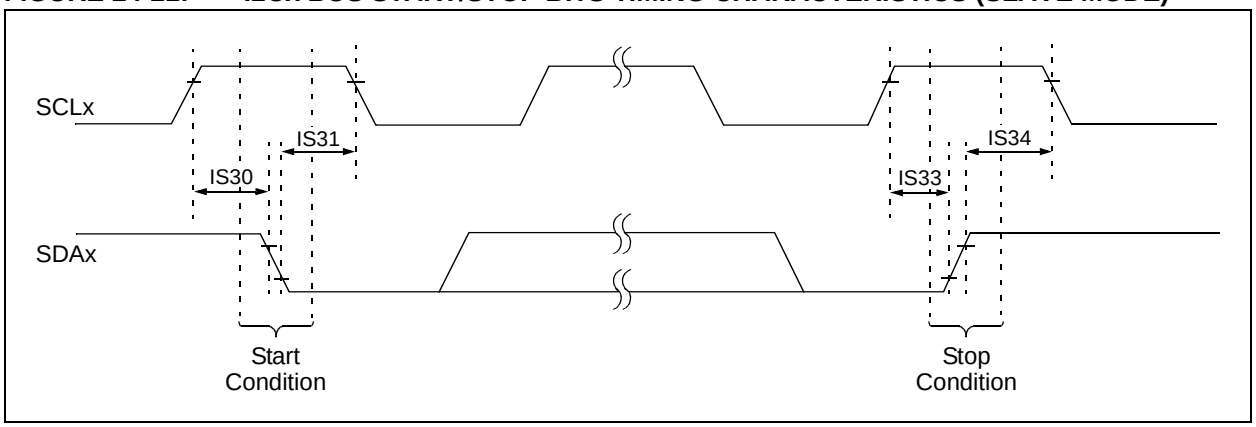


FIGURE 24-22: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)

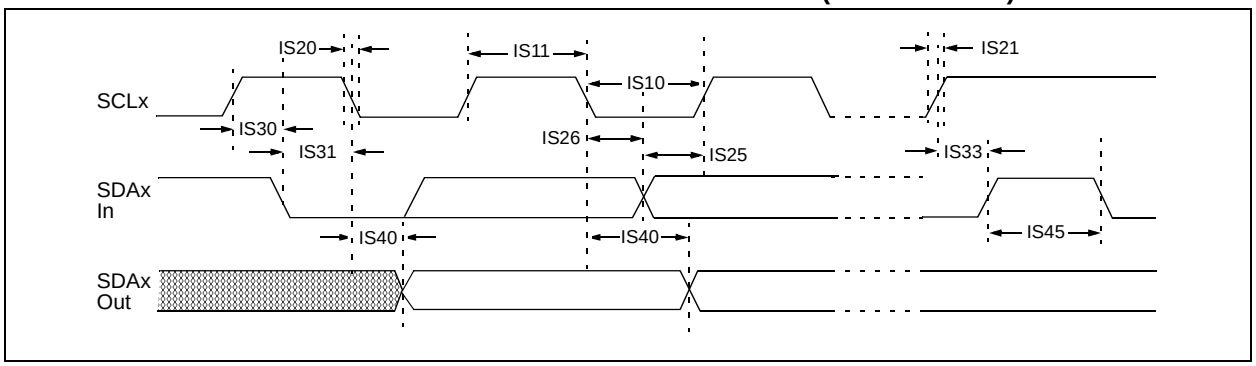


TABLE A-3: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 19.0 "High-Speed 10-bit Analog-to-Digital Converter (ADC)"	Updated Note 1 in the ADCPC0 register (see Register 19-5). Updated Note 3 in the ADCPC1 register (see Register 19-6). Updated Note 2 in the ADCPC2 and ADCPC3 registers (see Register 19-7 and Register 19-8).
Section 21.0 "Special Features"	Updated the second paragraph and removed the fourth paragraph in **Section 21.1 "Configuration Bits"**. Updated the Device Configuration Register Map (see Table 21-1).
Section 24.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings for high temperature and added Note 4. Updated Idle Current (I_{IDLE}) Typical values in Table 24-6. Updated the Typ and Max values for Parameter DI50 in the I/O Pin Input Specifications table (see Table 24-9). Updated the Typ and Max values for Parameters DO10 and DO27 and the Min and Typ values for Parameter DO20 in the I/O Pin Output Specifications (see Table 24-10). Added parameter numbers to the Auxiliary PLL Clock Timing Specifications (see Table 24-18). Added parameters numbers and updated the Internal RC Accuracy Min, Typ, and Max values (see Table 24-19 and Table 24-20). Added parameter numbers, Note 2, updated the Min and Typ parameter values for MP31 and MP32, and removed the conditions for MP10 and MP11 in the High-Speed PWM Module Timing Requirements (see Table 24-29). Updated the SPIx Module Slave Mode (CKE = 1) Timing Characteristics (see Table 24-14). Added Parameter IM51 to the I2Cx Bus Data Timing Requirements (Master Mode) (see Table 24-34). Updated the Max value for Parameter AD33 in the 10-bit High-Speed Analog-to-Digital Module Specifications (see Table 24-36). Updated the titles and added parameter numbers to the Comparator and DAC Module Specifications (see Table 24-38 and Table 24-39) and the DAC Output Buffer Specifications (see Table 24-40).

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