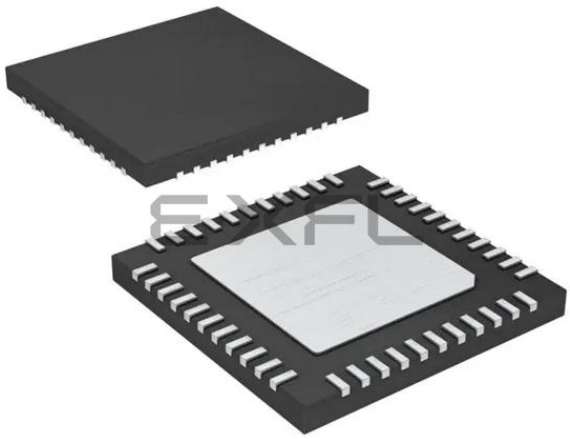
Microchip Technology - DSPIC33FJ16GS404-E/ML Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gs404-e-ml

dsPIC33FJ06GS101/X02 AND dsPIC33FJ16GSX02/X04 PRODUCT FAMILIES

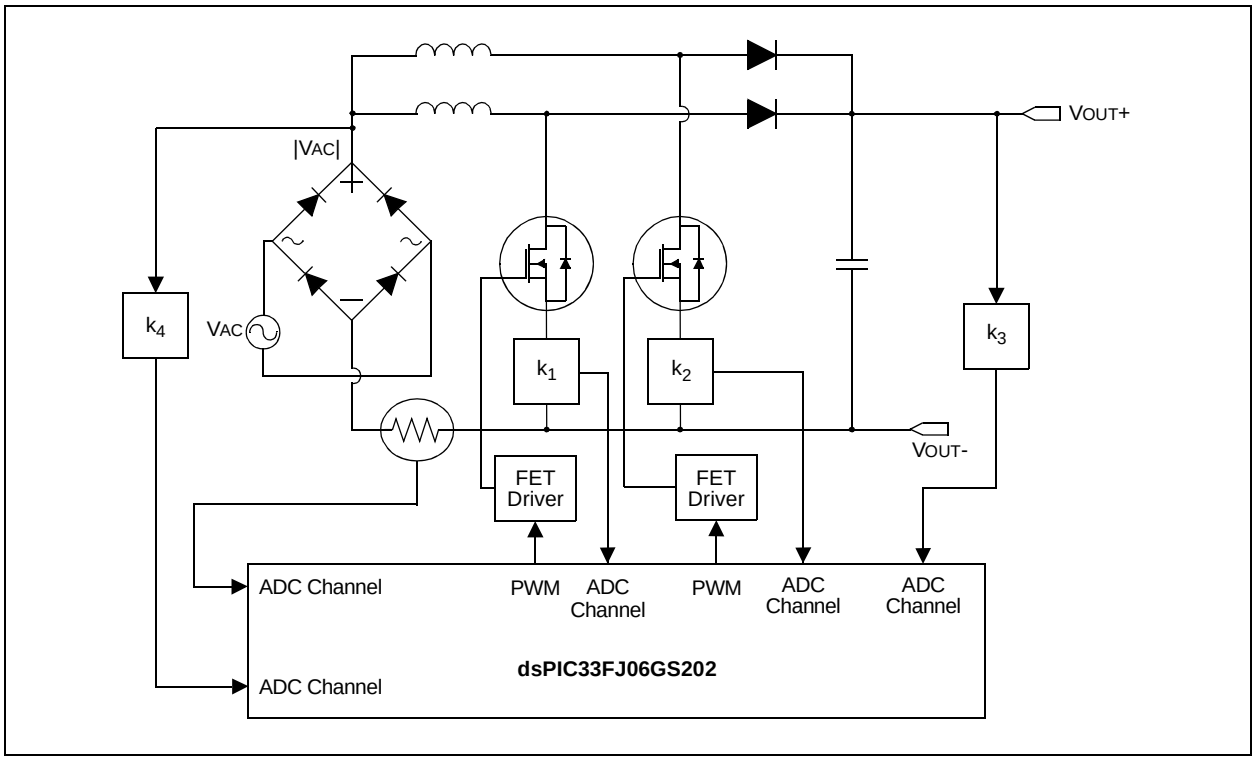
The device names, pin counts, memory sizes and peripheral availability of each device are listed below. The following pages show their pinout diagrams.

TABLE 1: dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 CONTROLLER FAMILIES

Device	Pins	Program Flash Memory (Kbytes)	RAM (Bytes)	Remappable Peripherals									DAC Output	I^2C™	ADC			I/O Pins	Packages
				Remappable Pins	16-Bit Timer	Input Capture	Output Compare	UART	SPI	PWM(2)	Analog Comparator	External Interrupts(3)			SARs	Sample-and-Hold (S&H) Circuit	Analog-to-Digital Inputs		
dsPIC33FJ06GS101	18	6	256	8	2	0	1	1	1	2x2(1)	0	3	0	1	1	3	6	13	SOIC
dsPIC33FJ06GS102	28	6	256	16	2	0	1	1	1	2x2	0	3	0	1	1	3	6	21	SPDIP, SOIC, QFN-S
dsPIC33FJ06GS202	28	6	1K	16	2	1	1	1	1	2x2	2	3	1	1	1	3	6	21	SPDIP, SOIC, QFN-S
dsPIC33FJ16GS402	28	16	2K	16	3	2	2	1	1	3x2	0	3	0	1	1	4	8	21	SPDIP, SOIC, QFN-S
dsPIC33FJ16GS404	44	16	2K	30	3	2	2	1	1	3x2	0	3	0	1	1	4	8	35	QFN, TQFP, VTLA
dsPIC33FJ16GS502	28	16	2K	16	3	2	2	1	1	4x2(1)	4	3	1	1	2	6	8	21	SPDIP, SOIC, QFN-S, UQFN
dsPIC33FJ16GS504	44	16	2K	30	3	2	2	1	1	4x2(1)	4	3	1	1	2	6	12	35	QFN, TQFP, VTLA

Note 1: The PWM4H:PWM4L pins are remappable.
2: The PWM Fault pins and PWM synchronization pins are remappable.
3: Only two out of three interrupts are remappable.

FIGURE 2-9: INTERLEAVED PFC



4.2.5 X AND Y DATA SPACES

The core has two data spaces, X and Y. These data spaces can be considered either separate (for some DSP instructions), or as one unified linear address range (for MCU instructions). The data spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X data space is used by all instructions and supports all addressing modes. X data space has separate read and write data buses. The X read data bus is the read data path for all instructions that view data space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y data space is used in concert with the X data space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY.N and MSC) to provide two concurrent data read paths.

Both the X and Y data spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X data space.

All data memory writes, including in DSP instructions, view data space as combined X and Y address space. The boundary between the X and Y data spaces is device-dependent and is not user-programmable.

All Effective Addresses are 16 bits wide and point to bytes within the data space. Therefore, the data space address range is 64 Kbytes, or 32K words, though the implemented memory locations vary by device.

REGISTER 7-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	INT2IF	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT1IF	CNIF	AC1IF	MI2C1IF	SI2C1IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **INT2IF:** External Interrupt 2 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12-5 **Unimplemented:** Read as ‘0’

bit 4 **INT1IF:** External Interrupt 1 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **CNIF:** Input Change Notification Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **AC1IF:** Analog Comparator 1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **MI2C1IF:** I2C1 Master Events Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **SI2C1IF:** I2C1 Slave Events Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 7-9: IFS5: INTERRUPT FLAG STATUS REGISTER 5

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
PWM2IF	PWM1IF	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PWM2IF:** PWM2 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 14 **PWM1IF:** PWM1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13-0 **Unimplemented:** Read as ‘0’

REGISTER 7-12: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ADIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IE	OC2IE	IC2IE	—	T1IE	OC1IE	IC1IE	INT0IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **ADIE:** ADC1 Conversion Complete Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 12 **U1TXIE:** UART1 Transmitter Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 11 **U1RXIE:** UART1 Receiver Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 10 **SPI1IE:** SPI1 Event Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 9 **SPI1EIE:** SPI1 Event Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 8 **T3IE:** Timer3 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 7 **T2IE:** Timer2 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 6 **OC2IE:** Output Compare Channel 2 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 5 **IC2IE:** Input Capture Channel 2 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **T1IE:** Timer1 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 2 **OC1IE:** Output Compare Channel 1 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

REGISTER 7-35: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	ILR3	ILR2	ILR1	ILR0
bit 15							bit 8

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

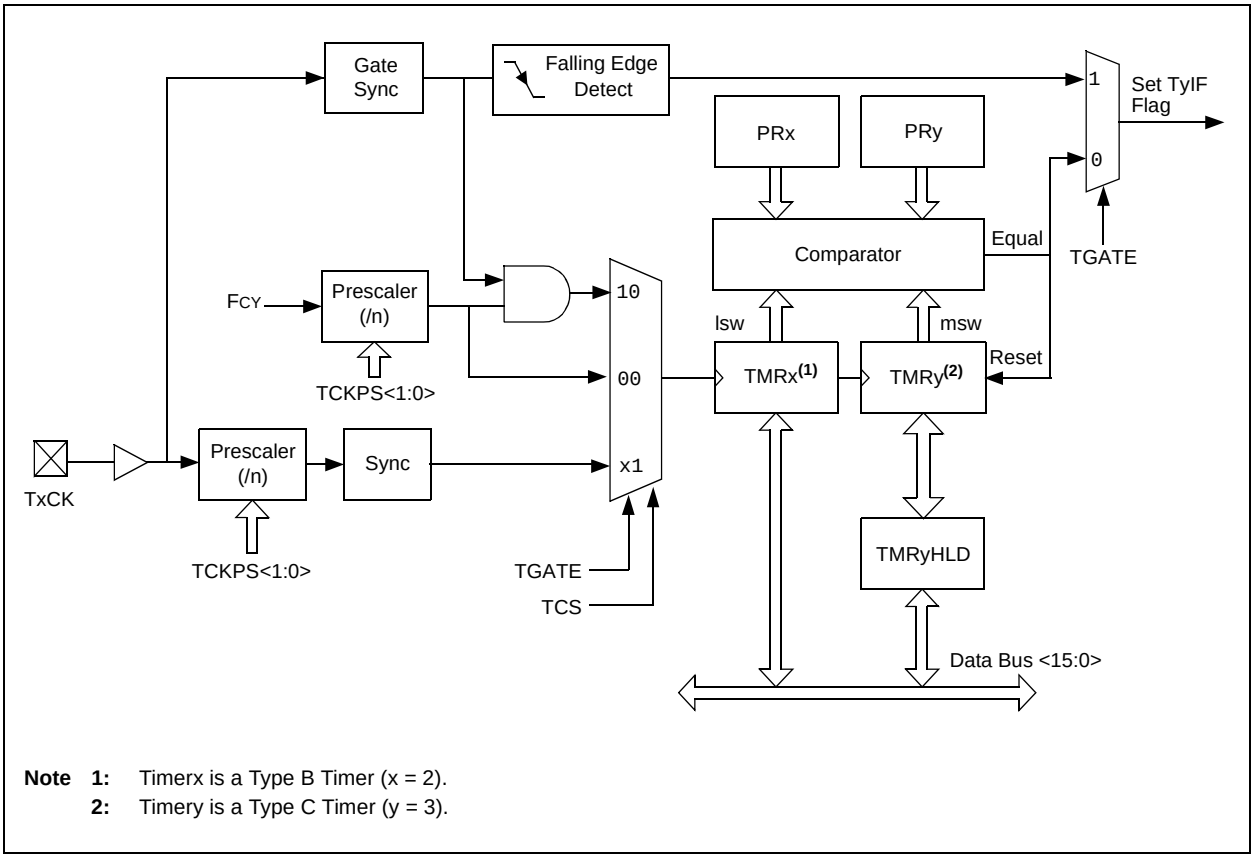
bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-8 **ILR<3:0>:** New CPU Interrupt Priority Level bits
1111 = CPU Interrupt Priority Level is 15
•
•
•
0001 = CPU Interrupt Priority Level is 1
0000 = CPU Interrupt Priority Level is 0

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **VECNUM<6:0>:** Vector Number of Pending Interrupt bits
0111111 = Interrupt vector pending is Number 135
•
•
•
0000001 = Interrupt vector pending is Number 9
0000000 = Interrupt vector pending is Number 8

FIGURE 12-3: 32-BIT TIMER BLOCK DIAGRAM



Note 1: Timerx is a Type B Timer (x = 2).
2: Timery is a Type C Timer (y = 3).

19.4 ADC Control Registers

The ADC module uses the following control and status registers:

- ADCON: Analog-to-Digital Control Register
- ADSTAT: Analog-to-Digital Status Register
- ADBASE: Analog-to-Digital Base Register(1,2)
- ADPCFG: Analog-to-Digital Port Configuration Register
- ADCPC0: Analog-to-Digital Convert Pair Control Register 0
- ADCPC1: Analog-to-Digital Convert Pair Control Register 1
- ADCPC2: Analog-to-Digital Convert Pair Control Register 2(1)
- ADCPC3: Analog-to-Digital Convert Pair Control Register 3(1)

The ADCON register controls the operation of the ADC module. The ADSTAT register displays the status of the conversion processes. The ADPCFG registers configure the port pins as analog inputs or as digital I/O. The ADCPCx registers control the triggering of the ADC conversions. See Register 19-1 through Register 19-8 for detailed bit configurations.

Note:	A unique feature of the ADC module is its ability to sample inputs in an asynchronous manner. Individual Sample-and-Hold circuits can be triggered independently of each other.

REGISTER 19-1: ADCON: ANALOG-TO-DIGITAL CONTROL REGISTER (CONTINUED)

bit 4 **ASYNCSAMP:** Asynchronous Dedicated S&H Sampling Enable bit(1)

1 = The dedicated S&H is constantly sampling and then terminates sampling as soon as the trigger pulse is detected

0 = The dedicated S&H starts sampling when the trigger event is detected and completes the sampling process in two ADC clock cycles

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **ADCS<2:0>:** Analog-to-Digital Conversion Clock Divider Select bits(1)

111 = FADC/8
110 = FADC/7
101 = FADC/6
100 = FADC/5
011 = FADC/4 (default)
010 = FADC/3
001 = FADC/2
000 = FADC/1

Note 1: These control bits can only be changed while ADC is disabled (ADON = 0).

2: These bits are only available on devices with one SAR.

REGISTER 19-6: ADCPC1: ANALOG-TO-DIGITAL CONVERT PAIR CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN3(1)	PEND3(1)	SWTRG3(1)	TRGSRC34(1)	TRGSRC33(1)	TRGSRC32(1)	TRGSRC31(1)	TRGSRC30(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN2(2)	PEND2(2)	SWTRG2(2)	TRGSRC24(2)	TRGSRC23(2)	TRGSRC22(2)	TRGSRC21(2)	TRGSRC20(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **IRQEN3:** Interrupt Request Enable 3 bit(1)
1 = Enables IRQ generation when requested conversion of Channels AN7 and AN6 is completed
0 = IRQ is not generated

bit 14 **PEND3:** Pending Conversion Status 3 bit(1)
1 = Conversion of Channels AN7 and AN6 is pending; set when selected trigger is asserted
0 = Conversion is complete

bit 13 **SWTRG3:** Software Trigger 3 bit(1)
1 = Starts conversion of AN7 and AN6 (if selected by the TRGSRCx bits)(3)
This bit is automatically cleared by hardware when the PEND3 bit is set.
0 = Conversion has not started

Note 1: These bits are available in the dsPIC33FJ16GS402/404, dsPIC33FJ16GS504, dsPIC33FJ16GS502 and dsPIC33FJ06GS101 devices only.

2: These bits are available in the dsPIC33FJ16GS502, dsPIC33FJ16GS504, dsPIC33FJ06GS102, dsPIC33FJ06GS202 and dsPIC33FJ16GS402/404 devices only.

3: The trigger source must be set as a global software trigger prior to setting this bit to ‘1’. If other conversions are in progress, then the conversion will be performed when the conversion resources are available.

REGISTER 20-2: CMPDACx: COMPARATOR DAC x CONTROL REGISTER

r-0	r-0	r-0	r-0	r-0	r-0	R/W-0	R/W-0
r	r	r	r	r	r	CMREF<9:8>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMREF<7:0>							
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Reserved:** Read as '0'

bit 9-0 **CMREF<9:0>:** Comparator Reference Voltage Select bits

1111111111 = (CMREF<9:0> * INTREF/1024) or (CMREF<9:0> * (AV_{DD}/2)/1024) volts depending on the RANGE bit or (CMREF<9:0> * EXTREF/1024) if EXTREF is set

•
•
•

0000000000 = 0.0 volts

24.2 AC Characteristics and Timing Parameters

This section defines dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 AC characteristics and timing parameters.

TABLE 24-14: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended Operating voltage VDD range as described in Table 24-1.

FIGURE 24-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

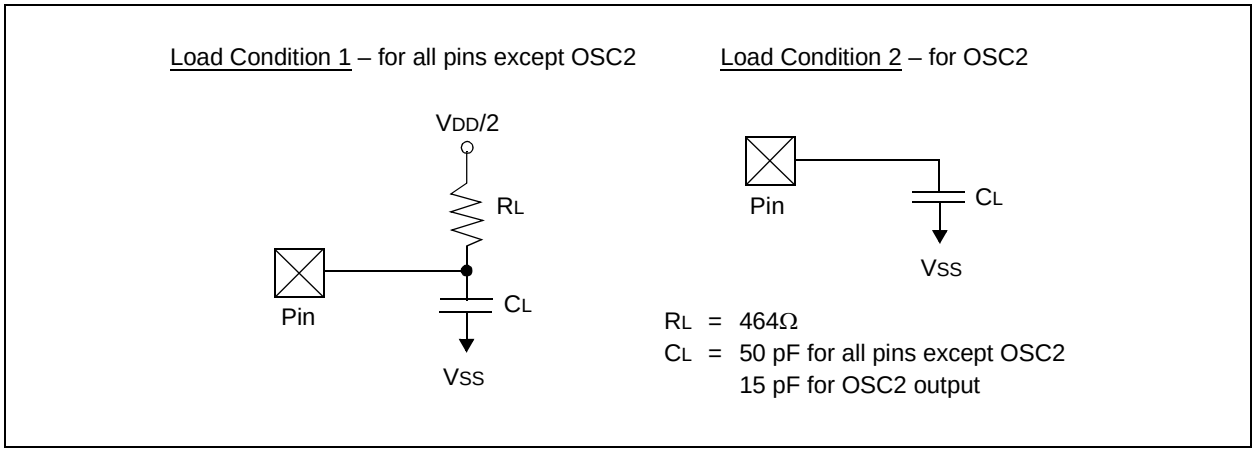


TABLE 24-15: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
DO50	COSCO	OSC2 Pin	—	—	15	pF	In XT and HS modes when external clock is used to drive OSC1
DO56	CIO	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C™ mode

TABLE 24-40: 10-BIT HIGH-SPEED ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 2): 3.0V and 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	—	—	—	—	AVDD is internally connected to VDD; see Parameter DC10 in Table 24-4
AD02	AVSS	Module VSS Supply	—	—	—	—	AVSS is internally connected to VSS
Analog Input							
AD10	VINH-VINL	Full-Scale Input Span	VSS	—	VDD	V	
AD11	VIN	Absolute Input Voltage	AVSS	—	AVDD	V	
AD12	IAD	Operating Current	—	8	—	mA	
AD13	—	Leakage Current	—	±0.6	—	μA	VINL = AVSS = 0V, AVDD = 3.3V, Source Impedance = 100Ω
AD17	RIN	Recommended Impedance Of Analog Voltage Source	—	—	100	Ω	
DC Accuracy @ 1.5 Msps							
AD20A	Nr	Resolution	10 Data Bits				
AD21A	INL	Integral Nonlinearity	-0.5	-0.3/+0.5	+1.2	LSb	
AD22A	DNL	Differential Nonlinearity	-0.9	±0.6	+0.9	LSb	
AD23A	GERR	Gain Error	13	15	22	LSb	
AD24A	EOFF	Offset Error	6	7	8	LSb	
AD25A	—	Monotonicity(1)	—	—	—	—	Guaranteed
DC Accuracy @ 1.7 Msps							
AD20B	Nr	Resolution	10 Data Bits				
AD21B	INL	Integral Nonlinearity	-0.5	-0.4/+1.1	+1.8	LSb	
AD22B	DNL	Differential Nonlinearity	-1.0	±1.0	+1.5	LSb	
AD23B	GERR	Gain Error	13	15	22	LSb	
AD24B	EOFF	Offset Error	6	7	8	LSb	
AD25B	—	Monotonicity(1)	—	—	—	—	Guaranteed
DC Accuracy @ 2.0 Msps							
AD20C	Nr	Resolution	10 Data Bits				
AD21C	INL	Integral Nonlinearity	-0.8	-0.5/+1.8	+2.8	LSb	
AD22C	DNL	Differential Nonlinearity	-1.0	-1.0/+1.8	+2.8	LSb	
AD23C	GERR	Gain Error	14	16	23	LSb	
AD24C	EOFF	Offset Error	6	7	8	LSb	
AD25C	—	Monotonicity(1)	—	—	—	—	Guaranteed
Dynamic Performance							
AD30	THD	Total Harmonic Distortion	—	-73	—	dB	
AD31	SINAD	Signal to Noise and Distortion	—	58	—	dB	
AD32	SFDR	Spurious Free Dynamic Range	—	-73	—	dB	
AD33	FNYQ	Input Signal Bandwidth	—	—	1	MHz	
AD34	ENOB	Effective Number of Bits	—	9.4	—	bits	

Note 1: The Analog-to-Digital conversion result never decreases with an increase in input voltage, and has no missing codes.

2: Module is functional at VBOR < VDD < VDDMIN, but with degraded performance. Module functionality is tested but not characterized.

TABLE 24-44: DAC OUTPUT BUFFER DC SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 3.0V to 3.6V Operating temperature: -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
DA10	RLOAD	Resistive Output Load Impedance	3K	—	—	Ω	
DA11	CLOAD	Output Load Capacitance	—	20	35	pF	
DA12	IOUT	Output Current Drive Strength	-1740	±1400	+1770	μA	Sink and source
DA13	VRANGE	Full Output Drive Strength Voltage Range	AVSS + 250 mV	—	AVDD – 900 mV	V	
DA14	VLRANGE	Output Drive Voltage Range at Reduced Current Drive of 50 μA	AVSS + 50 mV	—	AVDD – 500 mV	V	
DA15	IDD	Current Consumed when Module is Enabled, High-Power Mode	369	626	948	μA	Module will always consume this current even if no load is connected to the output
DA16	ROUTON	Output Impedance when Module is Enabled	—	1200	—	Ω	

Note 1: Module is functional at VBOR < VDD < VDDMIN, but with degraded performance. Module functionality is tested but not characterized.

TABLE 25-5: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DO10	VOL	**Output Low Voltage** I/O Pins: 4x Sink Driver Pins – RA0-RA2, RB0-RB2, RB5-RB10, RB15, RC1, RC2, RC9, RC10	—	—	0.4	V	IOL ≤ 3.6 mA, VDD = 3.3V See **Note 1**
		Output Low Voltage I/O Pins: 8x Sink Driver Pins – RC0, RC3-RC8, RC11-RC13	—	—	0.4	V	IOL ≤ 6 mA, VDD = 3.3V See **Note 1**
		Output Low Voltage I/O Pins: 16x Sink Driver Pins – RA3, RA4, RB3, RB4, RB11-RB14	—	—	0.4	V	IOL ≤ 12 mA, VDD = 3.3V See **Note 1**
DO20	VOH	**Output High Voltage** I/O Pins: 4x Source Driver Pins – RA0-RA2, RB0-RB2, RB5-RB10, RB15, RC1, RC2, RC9, RC10	2.4	—	—	V	IOL ≥ -4 mA, VDD = 3.3V See **Note 1**
		Output High Voltage I/O Pins: 8x Source Driver Pins – RC0, RC3-RC8, RC11-RC13	2.4	—	—	V	IOL ≥ -8 mA, VDD = 3.3V See **Note 1**
		Output High Voltage I/O Pins: 16x Source Driver Pins – RA3, RA4, RB3, RB4, RB11-RB14	2.4	—	—	V	IOL ≥ -16 mA, VDD = 3.3V See **Note 1**
DO20A	VOH1	**Output High Voltage** I/O Pins: 4x Source Driver Pins – RA0-RA2, RB0-RB2, RB5-RB10, RB15, RC1, RC2, RC9, RC10	1.5	—	—	V	IOH ≥ -3.9 mA, VDD = 3.3V See **Note 1**
			2.0	—	—		IOH ≥ -3.7 mA, VDD = 3.3V See **Note 1**
			3.0	—	—		IOH ≥ -2 mA, VDD = 3.3V See **Note 1**
		Output High Voltage I/O Pins: 8x Source Driver Pins – RC0, RC3-RC8, RC11-RC13	1.5	—	—	V	IOH ≥ -7.5 mA, VDD = 3.3V See **Note 1**
			2.0	—	—		IOH ≥ -6.8 mA, VDD = 3.3V See **Note 1**
			3.0	—	—		IOH ≥ -3 mA, VDD = 3.3V See **Note 1**
		Output High Voltage I/O Pins: 16x Source Driver Pins – RA3, RA4, RB3, RB4, RB11-RB14	1.5	—	—	V	IOH ≥ -15 mA, VDD = 3.3V See **Note 1**
			2.0	—	—		IOH ≥ -14 mA, VDD = 3.3V See **Note 1**
			3.0	—	—		IOH ≥ -7 mA, VDD = 3.3V See **Note 1**

Note 1: Parameters are characterized, but not tested.

TABLE 26-3: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

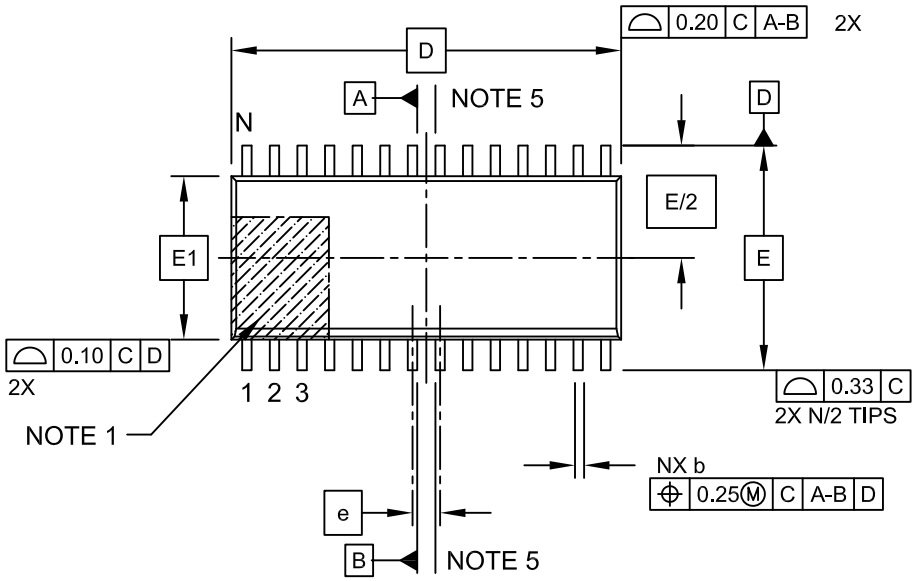
DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical**	**Max**	**Units**	**Conditions**		
Idle Current (I_{IDLE}): Core Off, Clock On Base Current(1)						
MDC45d	64	105	mA	-40°C	3.3V	50 MIPS
MDC45a	64	105	mA	+25°C		
MDC45b	64	105	mA	+85°C		

Note 1: Base Idle current (I_{IDLE}) is measured as follows:

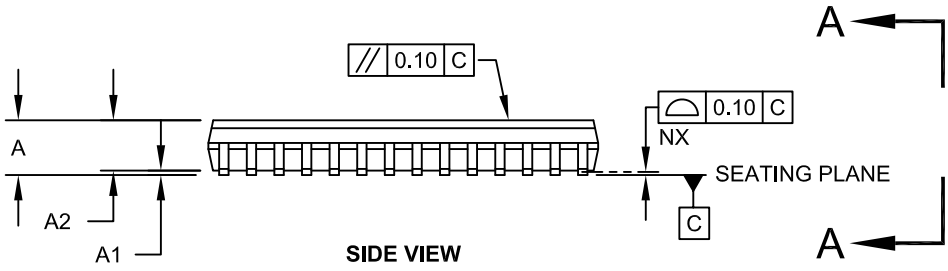
- CPU core is off, oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- JTAG is disabled

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

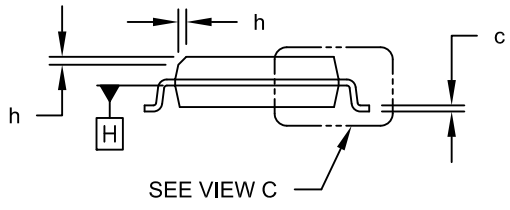
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

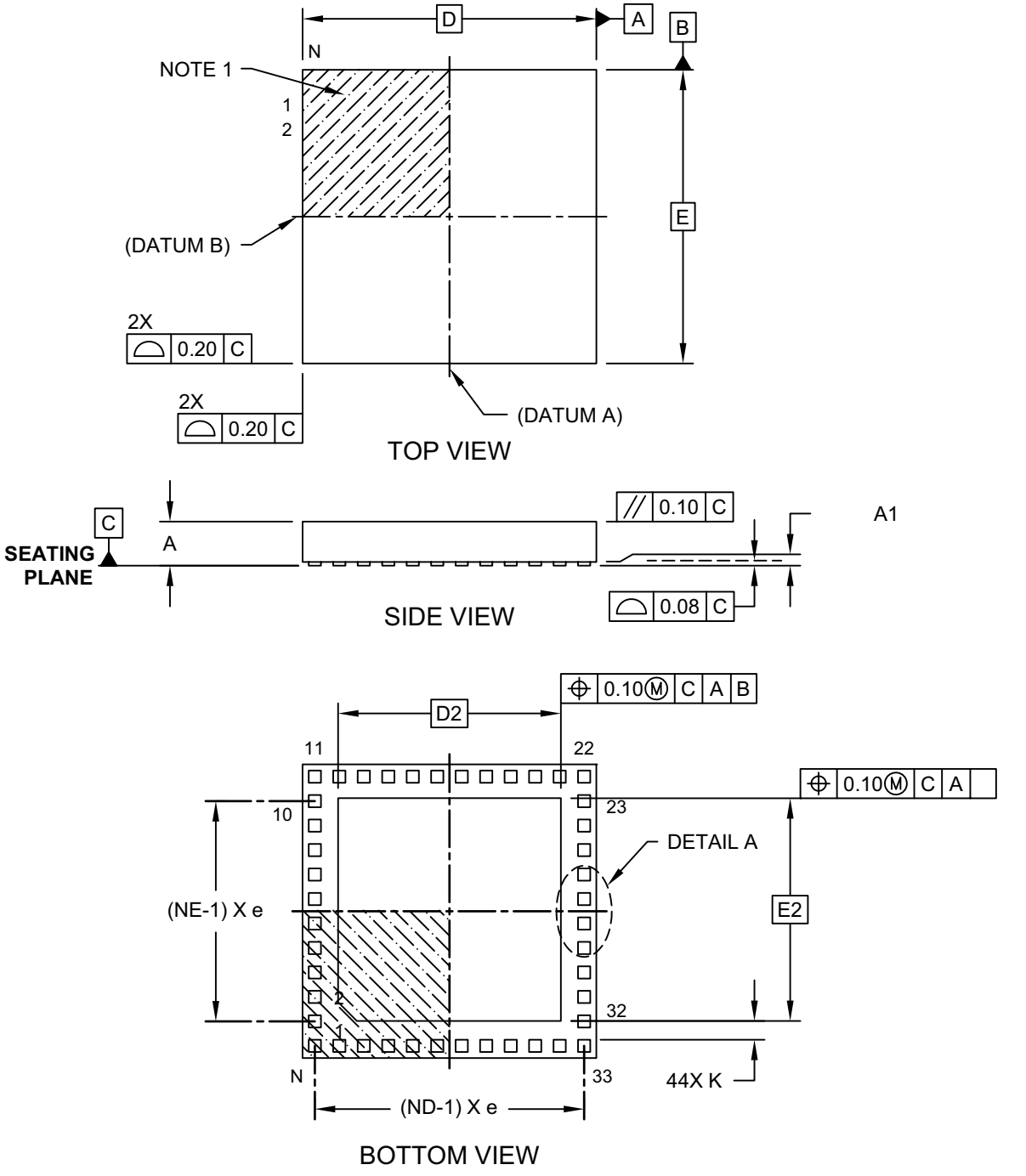


VIEW A-A

Microchip Technology Drawing C04-052C Sheet 1 of 2

44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-157D Sheet 1 of 2

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- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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