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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	16KB (16K × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gs404-h-ml

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The SA and SB bits are modified each time data passes through the adder/subtracter, but can only be cleared by the user application. When set, they indicate that the accumulator has overflowed its maximum range (bit 31 for 32-bit saturation or bit 39 for 40-bit saturation) and will be saturated (if saturation is enabled). When saturation is not enabled, SA and SB default to bit 39 overflow and thus, indicate that a catastrophic overflow has occurred. If the COVTE bit in the INTCON1 register is set, SA and SB bits will generate an arithmetic warning trap when saturation is disabled.

The Overflow and Saturation Status bits can optionally be viewed in the STATUS Register (SR) as the logical OR of OA and OB (in bit OAB) and the logical OR of SA and SB (in bit SAB). Programmers can check one bit in the STATUS Register to determine if either accumulator has overflowed, or one bit to determine if either accumulator has saturated. This is useful for complex number arithmetic, which typically uses both accumulators.

The device supports three Saturation and Overflow modes:

- Bit 39 Overflow and Saturation: When bit 39 overflow and saturation occurs, the saturation logic loads the maximally positive
 9.31 (0x7FFFFFFFF) or maximally negative
 9.31 value (0x800000000) into the target accumulator. The SA or SB bit is set and remains set until cleared by the user application. This condition is referred to as 'super saturation' and provides protection against erroneous data or unexpected algorithm problems (such as gain calculations).
- Bit 31 Overflow and Saturation: When bit 31 overflow and saturation occurs, the saturation logic then loads the maximally positive 1.31 value (0x007FFFFFFF) or maximally negative 1.31 value (0x008000000) into the target accumulator. The SA or SB bit is set and remains set until cleared by the user application. When this Saturation mode is in effect, the guard bits are not used, so the OA, OB or OAB bits are never set.
- Bit 39 Catastrophic Overflow: The bit 39 Overflow Status bit from the adder is used to set the SA or SB bit, which remains set
- until cleared by the user application. No saturation operation is performed, and the accumulator is allowed to overflow, destroying its sign. If the COVTE bit in the INTCON1 register is set, a catastrophic overflow can initiate a trap exception.

3.6.3 ACCUMULATOR 'WRITE BACK'

The MAC class of instructions (with the exception of MPY, MPY.N, ED and EDAC) can optionally write a rounded version of the high word (bits 31 through 16) of the accumulator that is not targeted by the instruction into data space memory. The write is performed across the X bus into combined X and Y address space. The following addressing modes are supported:

- W13, Register Direct: The rounded contents of the non-target accumulator are written into W13 as a 1.15 fraction.
- [W13] + = 2, Register Indirect with Post-Increment: The rounded contents of the non-target accumulator are written into the address pointed to by W13 as a 1.15 fraction. W13 is then incremented by 2 (for a word write).

3.6.3.1 Round Logic

The round logic is a combinational block that performs a conventional (biased) or convergent (unbiased) round function during an accumulator write (store). The Round mode is determined by the state of the RND bit in the CORCON register. It generates a 16-bit, 1.15 data value that is passed to the data space write saturation logic. If rounding is not indicated by the instruction, a truncated 1.15 data value is stored and the least significant word is simply discarded.

Conventional rounding zero-extends bit 15 of the accumulator and adds it to the ACCxH word (bits 16 through 31 of the accumulator).

- If the ACCxL word (bits 0 through 15 of the accumulator) is between 0x8000 and 0xFFFF (0x8000 included), ACCxH is incremented.
- If ACCxL is between 0x0000 and 0x7FFF, ACCxH is left unchanged.

A consequence of this algorithm is that over a succession of random rounding operations, the value tends to be biased slightly positive.

Convergent (or unbiased) rounding operates in the same manner as conventional rounding, except when ACCxL equals 0x8000. In this case, the Least Significant bit (bit 16 of the accumulator) of ACCxH is examined:

- If it is '1', ACCxH is incremented.
- If it is '0', ACCxH is not modified.

Assuming that bit 16 is effectively random in nature, this scheme removes any rounding bias that may accumulate.

TABLE 4-25: HIGH-SPEED 10-BIT ADC REGISTER MAP FOR dsPIC33FJ06GS101 DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADCON	0300	ADON	_	ADSIDL	SLOWCLK	_	GSWTRG	-	FORM	EIE	ORDER	SEQSAMP	ASYNCSAMP	—	ADCS2	ADCS1	ADCS0	0003
ADPCFG	0302	_	_	_	_	_	-	_	_	PCFG7	PCFG6	_	_	PCFG3	PCFG2	PCFG1	PCFG0	0000
ADSTAT	0306			—	—	—	_	_	—					P3RDY	—	P1RDY	P0RDY	0000
ADBASE	0308	ADBASE<15:1>									_	0000						
ADCPC0	030A	IRQEN1	PEND1	SWTRG1	TRGSRC14	TRGSRC13	TRGSRC12	TRGSRC11	TRGSRC10	IRQEN0	PEND0	SWTRG0	TRGSRC04	TRGSRC03	TRGSRC02	TRGSRC01	TRGSRC00	0000
ADCPC1	030C	IRQEN3	PEND3	SWTRG3	TRGSRC34	TRGSRC33	TRGSRC32	TRGSRC31	TRGSRC30	_	_	_	_	_	_	_	_	0000
ADCBUF0	0320								ADC D	ata Buffer	0							xxxx
ADCBUF1	0322								ADC D	ata Buffer	1							xxxx
ADCBUF2	0324	ADC Data Buffer 2 x									xxxx							
ADCBUF3	0326	ADC Data Buffer 3									xxxx							
ADCBUF6	032C	ADC Data Buffer 6 x									xxxx							
ADCBUF7	032E								ADC D	ata Buffer	7							xxxx

x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-26: HIGH-SPEED 10-BIT ADC REGISTER MAP FOR dsPIC33FJ06GS102 DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADCON	0300	ADON	_	ADSIDL	SLOWCLK	—	GSWTRG	—	FORM	EIE	ORDER	SEQSAMP	ASYNCSAMP	—	ADCS2	ADCS1	ADCS0	0003
ADPCFG	0302	_	_	_	_	_	_	_	_	_	_	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
ADSTAT	0306	_	_	_	_	_	_	_	_	_	_	_	_	_	P2RDY	P1RDY	PORDY	0000
ADBASE	0308	ADBASE<15:1>									_	0000						
ADCPC0	030A	IRQEN1	PEND1	SWTRG1	TRGSRC14	TRGSRC13	TRGSRC12	TRGSRC11	TRGSRC10	IRQEN0	PEND0	SWTRG0	TRGSRC04	TRGSRC03	TRGSRC02	TRGSRC01	TRGSRC00	0000
ADCPC1	030C	_	_	_	_	_	_	_	_	IRQEN2	PEND2	SWTRG2	TRGSRC24	TRGSRC23	TRGSRC22	TRGSRC21	TRGSRC20	0000
ADCBUF0	0320								ADC Da	ata Buffer	0							xxxx
ADCBUF1	0322								ADC Da	ata Buffer	1							xxxx
ADCBUF2	0324								ADC Da	ata Buffer	2							xxxx
ADCBUF3	0326	ADC Data Buffer 3 xxx								xxxx								
ADCBUF4	0328	ADC Data Buffer 4								xxxx								
ADCBUF5	032A	ADC Data Buffer 5								xxxx								

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Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

6.3 External Reset (EXTR)

The External Reset is generated by driving the MCLR pin low. The MCLR pin is a Schmitt trigger input with an additional glitch filter. Reset pulses that are longer than the minimum pulse width will generate a Reset. Refer to **Section 24.0** "**Electrical Characteristics**" for minimum pulse width specifications. The External Reset (MCLR) pin (EXTR) bit in the Reset Control (RCON) register is set to indicate the MCLR Reset.

6.3.0.1 EXTERNAL SUPERVISORY CIRCUIT

Many systems have external supervisory circuits that generate Reset signals to reset multiple devices in the system. This External Reset signal can be directly connected to the MCLR pin to reset the device when the rest of the system is reset.

6.3.0.2 INTERNAL SUPERVISORY CIRCUIT

When using the internal power supervisory circuit to reset the device, the External Reset pin (MCLR) should be tied directly or resistively to VDD. In this case, the MCLR pin will not be used to generate a Reset. The External Reset pin (MCLR) does not have an internal pull-up and must not be left unconnected.

6.4 Software RESET Instruction (SWR)

Whenever the RESET instruction is executed, the device will assert SYSRST, placing the device in a special Reset state. This Reset state will not re-initialize the clock. The clock source in effect prior to the RESET instruction will remain. SYSRST is released at the next instruction cycle and the Reset vector fetch will commence.

The Software Reset (SWR) flag (instruction) in the Reset Control (RCON<6>) register is set to indicate the Software Reset.

6.5 Watchdog Timer Time-out Reset (WDTO)

Whenever a Watchdog time-out occurs, the device will asynchronously assert SYSRST. The clock source will remain unchanged. A WDT time-out during Sleep or Idle mode will wake-up the processor, but will not reset the processor.

The Watchdog Timer Time-out (WDTO) flag in the Reset Control (RCON<4>) register is set to indicate the Watchdog Timer Reset. Refer to **Section 21.4 "Watchdog Timer (WDT)**" for more information on the Watchdog Timer Reset.

6.6 Trap Conflict Reset

If a lower priority hard trap occurs while a higher priority trap is being processed, a hard Trap Conflict Reset occurs. The hard traps include exceptions of Priority Levels 13 through 15, inclusive. The address error (Level 13) and oscillator error (Level 14) traps fall into this category.

The Trap Reset (TRAPR) flag in the Reset Control (RCON<15>) register is set to indicate the Trap Conflict Reset. Refer to **Section 7.0 "Interrupt Controller"** for more information on Trap Conflict Resets.

6.7 Configuration Mismatch Reset

To maintain the integrity of the Peripheral Pin Select Control registers, they are constantly monitored with shadow registers in hardware. If an unexpected change in any of the registers occur (such as cell disturbances caused by ESD or other external events), a Configuration Mismatch Reset occurs.

The Configuration Mismatch (CM) flag in the Reset Control (RCON<9>) register is set to indicate the Configuration Mismatch Reset. Refer to **Section 10.0 "I/O Ports"** for more information on the Configuration Mismatch Reset.

Note:	The	Configuration	Mismatch	Reset			
	featu	are not					
	available on all devices.						

6.8 Illegal Condition Device Reset

An illegal condition device Reset occurs due to the following sources:

- Illegal Opcode Reset
- Uninitialized W Register Reset
- Security Reset

The Illegal Opcode or Uninitialized W Access Reset (IOPUWR) flag in the Reset Control (RCON<14>) register is set to indicate the illegal condition device Reset.

6.8.1 ILLEGAL OPCODE RESET

A device Reset is generated if the device attempts to execute an illegal opcode value that is fetched from program memory.

The Illegal Opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the Illegal Opcode Reset, use only the lower 16 bits of each program memory section to store the data values. The upper 8 bits should be programmed with 3Fh, which is an illegal opcode value.

10.0 I/O PORTS

- Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "I/O Ports" (DS70193) in the "dsPIC33F/PIC24H Family Reference Manual", which is available on Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

All of the device pins (except VDD, VSS, MCLR and OSC1/CLKI) are shared among the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

10.1 Parallel I/O (PIO) Ports

Generally a parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through", in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 10-1 shows how ports are shared with other peripherals and the associated I/O pin to which they are connected.

When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have three registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers and the port pin will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

FIGURE 10-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



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REGISTER 10-5: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
—	—	—	—	—	—	—	—				
bit 15	bit 15 bit 8										
U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1				
	—	OCFAR5	OCFAR4	OCFAR3	OCFAR2	OCFAR1	OCFAR0				
bit 7			•			•	bit 0				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 Unimplemented: Read as '0'

bit 5-0

OCFAR<5:0>: Assign Output Capture A (OCFA) to the Corresponding RPn Pin bits

111111 = Input tied to Vss 100011 = Input tied to RP35 100010 = Input tied to RP34 100001 = Input tied to RP33 100000 = Input tied to RP32

•

00000 = Input tied to RP0

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

-n = Value at POR '1' = Bit is set				'0' = Bit is cleared x = Bit is unknown					
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	l as '0'			
Legend:									
							bit 0		
bit 7							bit 0		
_	_	RP26R5	RP26R4	RP26R3	RP26R2	RP26R1	RP26R0		
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
bit 15							bit 8		
—	—	RP27R5	RP27R4	RP27R3	RP27R2	RP27R1	RP27R0		
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		

REGISTER 10-28: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13⁽¹⁾

Dit 15-14	Unimplemented: Read as 0
bit 13-8	RP27R<5:0>: Peripheral Output Function is Assigned to RP27 Output Pin bits (see Table 10-2 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	RP26R<5:0>: Peripheral Output Function is Assigned to RP26 Output Pin bits (see Table 10-2 for peripheral function numbers)

Note 1: This register is implemented in the dsPIC33FJ16GS404 and dsPIC33FJ16GS504 devices only.

REGISTER 10-29: RPOR14: PERIPHERAL PIN SELECT OUTPUT REGISTER 14⁽¹⁾

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP29R5	RP29R4	RP29R3	RP29R2	RP29R1	RP29R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP28R5	RP28R4	RP28R3	RP28R2	RP28R1	RP28R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 13-8	RP29R<5:0>: Peripheral Output Function is Assigned to RP29 Output Pin bits					
	(see Table 10-2 for peripheral function numbers)					
bit 7-6	Unimplemented: Read as '0'					

bit 5-0 **RP28R<5:0>:** Peripheral Output Function is Assigned to RP28 Output Pin bits (see Table 10-2 for peripheral function numbers)

Note 1: This register is implemented in the dsPIC33FJ16GS404 and dsPIC33FJ16GS504 devices only.

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R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0				
TON		TSIDL	—			_	—				
bit 15							bit 8				
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0				
	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—				
bit 7							bit 0				
Legend:											
R = Readabl	e bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'					
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	iown				
bit 15	TON: Timer1	On bit									
	1 = Starts 16- 0 = Stops 16-	·bit Timer1 ·bit Timer1									
bit 14	Unimplemen	ted: Read as '	0'								
bit 13	TSIDL: Timer	1 Stop in Idle N	Node bit								
	1 = Discontin	ues module op	eration when	device enters l	ldle mode						
	0 = Continue	s module opera	ation in Idle m	ode							
bit 12-7	Unimplemen	ted: Read as '	0'								
bit 6	TGATE: Time	GATE: Timer1 Gated Time Accumulation Enable bit									
	This bit is ign	<u>⊥:</u> ored.									
	When TCS =	0:									
	1 = Gated times	ne accumulation	n is enabled								
	0 = Gated tim	Time accumulation	n is disabled	- O-l							
DIT 5-4	10KPS<1:0>		JOCK Prescal	e Select bits							
	10 = 1.230 10 = 1.64										
	01 = 1:8										
h it 0	00 = 1:1	tad. Daad aa (0'								
DIT 3		ited: Read as	U aak Innut Sun	obranization C	alaat hit						
DIL Z	When TCS =		ock input Syn	chronization Se							
	1 = Synchron	<u>izes external c</u>	lock input								
	0 = Does not	synchronize ex	kternal clock i	nput							
	When TCS =	<u>0:</u> ored									
bit 1	TCS: Timer1	Clock Source S	Select bit								
	1 = External of	clock from T1C	K pin (on the	rising edge)							
	0 = Internal c	lock (FCY)		,							
bit 0	Unimplemen	ted: Read as '	0'								

REGISTER 11-1: T1CON: TIMER1 CONTROL REGISTER

FIGURE 12-3: 32-BIT TIMER BLOCK DIAGRAM



	REGISTER 15-10:	SPHASEX: PWMx SECONDARY PHASE-SHIFT REGISTER ^(1,2)
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R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
SPHASEx<15:8>								
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	SPHASEx<7:0>							
bit 7	bit 7 bit 0							
Legend:								
R = Readable bit W = Writable bit			U = Unimplen	nented bit, read	d as '0'			
-n = Value at POR '1' = E		'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown	

bit 15-0 SPHASEx<15:0>: Secondary Phase Offset for PWMxL Output Pin bits (used in Independent PWM mode only)

- **Note 1:** If PWMCONx<ITB> = 0, the following applies based on the mode of operation:
 - Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10); SPHASEx<15:0> = Not used
 - True Independent Output mode (IOCONx<PMOD> = 11); PHASEx<15:0> = Phase-shift value for PWMxL only
 - **2:** If PWMCONx<ITB> = 1, the following applies based on the mode of operation:
 - Complementary, Redundant and Push-Pull Output mode (IOCONx<PMOD> = 00, 01, or 10); SPHASEx<15:0> = Not used
 - True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11); PHASEx<15:0> = Independent Time Base period value for PWMxL only

B/W/ 0	11.0	DAM 0	11.0	11.0		11.0	11.0
	0-0		0-0	0-0	0-0	0-0	0-0
SFIEN	_	SFISIDL					hit 9
DIL 15							DILO
U-0	R/C-0	U-0	U-0	U-0	U-0	R-0	R-0
_	SPIROV		—		—	SPITBF	SPIRBF
bit 7						L	bit 0
Legend:		C = Clearable	bit				
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15 bit 14 bit 13 bit 12-7 bit 6	 SPIEN: SPIx Enable bit 1 = Enables module and configures SCKx, SDOx, SDIx and SSx as serial port pins 0 = Disables module Unimplemented: Read as '0' SPISIDL: SPIx Stop in Idle Mode bit 1 = Discontinues module operation when device enters Idle mode 0 = Continues module operation in Idle mode Unimplemented: Read as '0' SPIROV: SPIx Receive Overflow Flag bit 1 = A new byte/word is completely received and discarded. The user software has not read the previous data in the SPIxBUF register. 						
bit 5-2	Unimplemen	ted: Read as '	י)				
bit 1	SPITBF: SPIx Transmit Buffer Full Status bit						
	 1 = Transmit not yet started, SPIxTXB is full 0 = Transmit started, SPIxTXB is empty. Automatically set in hardware when CPU writes the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR. 						
bit 0	SPIRBF: SPI	x Receive Buffe	er Full Status	bit			
	 1 = Receive complete, SPIxRXB is full 0 = Receive is not complete, SPIxRXB is empty. Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when core reads the SPIxBUF location, reading SPIxRXB. 						

REGISTER 16-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER

17.0 INTER-INTEGRATED CIRCUIT (I²C[™])

- Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Inter-Integrated Circuit (I²C[™])" (DS70000195) in the "dsPIC33/PIC24 Family Reference Manual", which is available on the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Inter-Integrated Circuit (l^2C) module provides complete hardware support for both Slave and Multi-Master modes of the l^2C serial communication standard with a 16-bit interface.

The I²C module has a 2-pin interface, where:

- The SCLx pin is clock
- The SDAx pin is data

The I²C module offers the following key features:

- I²C interface supporting both Master and Slave modes of operation
- I²C Slave mode supports 7-bit and 10-bit addressing
- I²C Master mode supports 7-bit and 10-bit addressing
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I²C supports multi-master operation, detects bus collision and arbitrates accordingly

17.1 Operating Modes

The hardware fully implements all the master and slave functions of the I^2C Standard and Fast mode specifications, as well as 7-bit and 10-bit addressing.

The I²C module can operate either as a slave or a master on an I²C bus.

The following types of I^2C operation are supported:

- I²C slave operation with 7-bit addressing
- I²C slave operation with 10-bit addressing
- I²C master operation with 7-bit or 10-bit addressing

21.2 On-Chip Voltage Regulator

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices power their core digital logic at a nominal 2.5V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. When the regulator is enabled, a low-ESR (less than 5 ohms) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 21-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 24-13 located in **Section 24.1 "DC Characteristics"**.

Note:	It is important for the low-ESR capacitor to
	be placed as close as possible to the VCAP
	pin.

On a POR, it takes approximately 20 μ s for the on-chip voltage regulator to generate an output voltage. During this time, designated as TSTARTUP, code execution is disabled. TSTARTUP is applied every time the device resumes operation after any power-down.

FIGURE 21-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR^(1,2,3)



21.3 BOR: Brown-out Reset

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines, or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM = 100 is applied. The total delay in this case is TFSCM.

The BOR Status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

FIGURE 24-14: SPIX MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS



TABLE 24-33:SPIX MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING
REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
SP10	TscP	Maximum SCKx Frequency	_	—	9	MHz	-40°C to +125°C and see Note 3
SP20	TscF	SCKx Output Fall Time	_		_	ns	See Parameter DO32 and Note 4
SP21	TscR	SCKx Output Rise Time				ns	See Parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	_	—	_	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	_	—	—	ns	See Parameter DO31 and Note 4
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30			ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—		ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30		_	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

4: Assumes 50 pF load on all SPIx pins.

^{3:} The minimum clock period for SCKx is 111 ns. The clock generated in Master mode must not violate this specification.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

TABLE 25-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACT	ERISTICS		Standard O (unless oth Operating to	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature				
Parameter No.	Typical ⁽¹⁾	Мах	Units	Conditions				
Power-Down Current (IPD) ^(2,4)								
HDC60e	1000	2000	μA	+150°C	3.3V	Base Power-Down Current		
HDC61c	100	110	μΑ	+150°C	3.3V	Watchdog Timer Current: △IwDT ⁽³⁾		

Note 1: Data in the Typical column is at 3.3V, +25°C unless otherwise stated.

2: IPD (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to Vss
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all ones)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to stand-by while the device is in Sleep mode)
- JTAG disabled
- **3:** The ∆ current is the additional current consumed when the WDT module is enabled. This current should be added to the base IPD current.
- 4: These currents are measured on the device containing the most memory in this family.

Revision F (January 2012)

All occurrences of VDDCORE have been removed throughout the document.

This revision also includes minor typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in the following table.

TABLE A-4: MAJOR SECTION UPDATES

Section Name	Update Description						
"16-Bit Digital Signal Controllers (up to 16-Kbyte Flash and up to 2-Kbyte SRAM) with High-Speed PWM, ADC and Comparators"	Added the VTLA package to the dsPIC33FJ16GS404 and dsPIC33FJ16GS504 devices (see TABLE 1: "dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Controller Families").						
	Added the "Referenced Sources" section.						
	The following updates were made to the "Pin Diagrams" section:						
	 Added 5V tolerant pin shading to pins 24-26 in the 28-pin SPDIP, SOIC package for the dsPIC33FJ16GS402 						
	• Updated pin 31 of the 44-pin QFN package for the dsPIC33FJ16GS404						
	Added VTLA pin diagrams for the dsPIC33FJ16GS404 and dsPIC33FJ16GS504 devices						
Section 1.0 "Device Overview"	Removed the Precision Band Gap Reference from the device block diagram (see Figure 1-1).						
	Updated the Pinout I/O Descriptions for AVDD, and AVSS (see Table 1-1).						
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers"	Updated the Minimum Recommended Connection (see Figure 2-1).						
Section 8.0 "Oscillator	Updated the Oscillator System Diagram (see Figure 8-1).						
Configuration	Added auxiliary clock configuration restrictions in Section 8.2 "Auxiliary Clock Generation ".						
	Updated or added notes regarding register reset on a POR (see Register 8-1 through Register 8-5).						
Section 19.0 "High-Speed 10-bit Analog-to-Digital Converter (ADC)"	Added Note 2 to ADCON: Analog-to-Digital Control Register (see Register 19-1).						
	Removed all notes from ADSTAT: Analog-to-Digital Status Register (see Register 19-2).						
Section 20.0 "High-Speed Analog Comparator"	Updated the Comparator Module Block Diagram (see Figure 20-1).						
Section 21.0 "Special Features"	Add a new paragraph at the beginning of Section 21.1 " Configuration Bits ".						
	Added the RTSP Effect column to the dsPIC33F Configuration Bits Description table (see Table 21-2).						
	Updated the Connections for the On-chip Voltage Regulator diagram (see Figure 21-1).						
	Updated the first paragraph of Section 21.7 "In-Circuit Debugger".						

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