



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gs404-h-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

dsPIC33FJ06GS101/X02 AND dsPIC33FJ16GSX02/X04 PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed below. The following pages show their pinout diagrams.

TABLE 1: dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 CONTROLLER FAMILIES

		(si				Rer	napp	able I	Perip	herals						ADC			
Device	Pins	Program Flash Memory (Kbyte	RAM (Bytes)	Remappable Pins	16-Bit Timer	Input Capture	Output Compare	UART	SPI	PWM ⁽²⁾	Analog Comparator	External Interrupts ⁽³⁾	DAC Output	I ² C TM	SARs	Sample-and-Hold (S&H) Circuit	Analog-to-Digital Inputs	I/O Pins	Packages
dsPIC33FJ06GS101	18	6	256	8	2	0	1	1	1	2x2 ⁽¹⁾	0	3	0	1	1	3	6	13	SOIC
dsPIC33FJ06GS102	28	6	256	16	2	0	1	1	1	2x2	0	3	0	1	1	3	6	21	SPDIP, SOIC, QFN-S
dsPIC33FJ06GS202	28	6	1K	16	2	1	1	1	1	2x2	2	3	1	1	1	3	6	21	SPDIP, SOIC, QFN-S
dsPIC33FJ16GS402	28	16	2K	16	3	2	2	1	1	3x2	0	3	0	1	1	4	8	21	SPDIP, SOIC, QFN-S
dsPIC33FJ16GS404	44	16	2K	30	3	2	2	1	1	3x2	0	3	0	1	1	4	8	35	QFN, TQFP, VTLA
dsPIC33FJ16GS502	28	16	2K	16	3	2	2	1	1	4x2 ⁽¹⁾	4	3	1	1	2	6	8	21	SPDIP, SOIC, QFN-S, UQFN
dsPIC33FJ16GS504	44	16	2K	30	3	2	2	1	1	4x2 ⁽¹⁾	4	3	1	1	2	6	12	35	QFN, TQFP, VTLA

Note 1: The PWM4H:PWM4L pins are remappable.

2: The PWM Fault pins and PWM synchronization pins are remappable.

3: Only two out of three interrupts are remappable.

Pin Diagrams (Continued)



4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Program Memory" (DS70202) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/ X04 architecture features separate program and data memory spaces and buses. This architecture also allows the direct access to program memory from the data space during code execution.

4.1 Program Address Space

The program address memory space of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit Program Counter (PC) during program execution, or from table operation or data space remapping, as described in **Section 4.6 "Interfacing Program and Data Memory Spaces"**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

The memory maps for the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices are shown in Figure 4-1.

FIGURE 4-1: PROGRAM MEMORY MAPS FOR dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 DEVICES



File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	_	MATHERR	ADDRERR	STKERR	OSCFAIL	_	0000
INTCON2	0082	ALTIVT	DISI	—	—	_	—	—	—	_	_	_	—	—	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	—	ADIF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	—	T1IF	OC1IF	IC1IF	INTOIF	0000
IFS1	0086	—	—	INT2IF	_	_	—	—	—	_	_	_	INT1IF	CNIF	AC1IF	MI2C1IF	SI2C1IF	0000
IFS3	008A	—	_	_	_	_	_	PSEMIF	_	_	_	_	_	_	_	_	_	0000
IFS4	008C	—	_	_	_	_	_	_	_	_	_	_	_	_	_	U1EIF	_	0000
IFS5	008E	PWM2IF	PWM1IF	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
IFS6	0090	ADCP1IF	ADCP0IF	_	_	_	_	AC4IF	AC3IF	AC2IF	_	_	_	_	_	PWM4IF	PWM3IF	0000
IFS7	0092	—	_	_	_	_	_	_	_	_	_	_	ADCP6IF	_	_	ADCP3IF	ADCP2IF	0000
IEC0	0094	—	_	ADIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	_	T1IE	OC1IE	IC1IE	INTOIE	0000
IEC1	0096	—	_	INT2IE	_	—		—	—	_	—	—	INT1IE	CNIE	AC1IE	MI2C1IE	SI2C1IE	0000
IEC3	009A	_	_		—	—		PSEMIE	_	_	—	—	_	_	_	_	_	0000
IEC4	009C	_	_		—	—		_	_	_	—	—	_	_	_	U1EIE	_	0000
IEC5	009E	PWM2IE	PWM1IE		—	—		_	_	_	—	—	_	_	_	_	_	0000
IEC6	00A0	ADCP1IE	ADCP0IE		—	—		AC4IE	AC3IE	AC2IE	—	—	_	_	_	PWM4IE	PWM3IE	0000
IEC7	00A2	_	_		—	—		_	_	_	—	—	ADCP6IE	_	_	ADCP3IE	ADCP2IE	0000
IPC0	00A4	_	T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0	_	IC1IP2	IC1IP1	IC1IP0	_	INT0IP2	INT0IP1	INT0IP2	4444
IPC1	00A6	_	T2IP2	T2IP1	T2IP0	—	OC2IP2	OC2IP1	OC2IP0	_	IC2IP2	IC2IP1	IC2IP0		_	_	_	4440
IPC2	00A8	_	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0	_	SPI1EIP2	SPI1EIP1	SPI1EIP0	_	T3IP2	T3IP1	T3IP0	4444
IPC3	00AA	_	_		—	—		_	_	-	ADIP2	ADIP1	ADIP0	_	U1TXIP2	U1TXIP1	U1TXIP0	0044
IPC4	00AC	_	CNIP2	CNIP1	CNIP0	—	AC1IP2	AC1IP1	AC1IP0	_	MI2C1IP2	MI2C1IP1	MI2C1IP0	_	SI2C1IP2	SI2C1IP1	SI2C1IP0	4444
IPC5	00AE	_	_		—	—		_	_	_	—	—	_	_	INT1IP2	INT1IP1	INT1IP0	0004
IPC7	00B2	_	_		—	—		_	_	_	INT2IP2	INT2IP1	INT2IP0	_	_	_	_	0040
IPC14	00C0	_	_			_		_	_	—	PSEMIP2	PSEMIP1	PSEMIP0	_	_	—	—	0040
IPC16	00C4	—	—	_	—	_	—	—	—	—	U1EIP2	U1EIP1	U1EIP0	—	_	—	—	0040
IPC23	00D2	—	PWM2IP2	PWM2IP1	PWM2IP0	—	PWM1IP2	PWM1IP1	PWM1IP0	—	_	—	—	—	_	—	—	4400
IPC24	00D4	—	—	_	—	_	—	—	—	—	PWM4IP2	PWM4IP1	PWM4IP0	—	PWM3IP2	PWM3IP1	PWM3IP0	0044
IPC25	00D6	_	AC2IP2	AC2IP1	AC2IP0	—		_	_	_	—	—	_	_	_	_	_	4000
IPC26	00D8	—	—	_	—	_	—	—	—	—	AC4IP2	AC4IP1	AC4IP0	—	AC3IP2	AC3IP1	AC3IP0	0044
IPC27	00DA	—	ADCP1IP2	ADCP1IP1	ADCP1IP0	—	ADCP0IP2	ADCP0IP1	ADCP0IP0		—	_	—	—	—	_	—	4400
IPC28	00DC	—	—	—	_	_	—	—	—	-	ADCP3IP2	ADCP3IP1	ADCP3IP0	—	ADCP2IP2	ADCP2IP1	ADCP2IP0	0044
IPC29	00DE	—	—	—	_	_	—	—	—	-	—	_	—	—	ADCP6IP2	ADCP6IP1	ADCP6IP0	0004
INTTREG	00E0	_	_		_	ILR3	ILR2	ILR1	ILR0		VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0	0000

TABLE 4-9: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33FJ16GS502 DEVICES ONLY

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

TABLE 4-11: TIMER REGISTER MAP FOR dsPIC33FJ06GS101 AND dsPIC33FJ06GSX02

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100								Timer1 Re	egister								0000
PR1	0102								Period Reg	gister 1								FFFF
T1CON	0104	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKPS1	TCKPS0	_	TSYNC	TCS	_	0000
TMR2	0106								Timer2 Re	egister								0000
PR2	010C								Period Reg	gister 2								FFFF
T2CON	0110	TON	—	TSIDL	—	—	_	_	_	—	TGATE	TCKPS1	TCKPS0	_	_	TCS	_	0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-12: TIMER REGISTER MAP FOR dsPIC33FJ16GSX02 AND dsPIC33FJ16GSX04

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100								Timer1 R	egister								0000
PR1	0102								Period Re	gister 1								FFFF
T1CON	0104	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKPS1	TCKPS0	_	TSYNC	TCS	_	0000
TMR2	0106								Timer2 R	egister								0000
TMR3HLD	0108						Timer3	Holding Re	gister (for 3	2-bit timer o	operations o	only)						xxxx
TMR3	010A								Timer3 R	egister								0000
PR2	010C								Period Re	gister 2								FFFF
PR3	010E	Period Register 3										FFFF						
T2CON	0110	TON	_	TSIDL	—	_	_	_	_	_	TGATE	TCKPS1	TCKPS0	T32	_	TCS	_	0000
T3CON	0112	TON	—	TSIDL	—	_	—	_	—		TGATE	TCKPS1	TCKPS0		_	TCS		0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-13: INPUT CAPTURE REGISTER MAP FOR dsPIC33FJ06GS202

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IC1BUF	0140							Inp	ut Capture	1 Register								xxxx
IC1CON	0142		-	ICSIDL		-	-		-	ICTMR	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.2.6 SOFTWARE STACK

In addition to its use as a Working register, the W15 register in the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices is also used as a software Stack Pointer. The Stack Pointer always points to the first available free word and grows from lower to higher addresses. It predecrements for stack pops and post-increments for stack pushes, as shown in Figure 4-6. For a PC push during any CALL instruction, the MSb of the PC is zero-extended before the push, ensuring that the MSb is always clear.

Note:	A PC push during exception processing
	concatenates the SRL register to the MSb
	of the PC prior to the push.

The Stack Pointer Limit register (SPLIM) associated with the Stack Pointer sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' because all stack operations must be word-aligned.

Whenever an EA is generated using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal and a push operation is performed, a stack error trap will not occur. The stack error trap will occur on a subsequent push operation. For example, to cause a stack error trap when the stack grows beyond address 0x1000 in RAM, initialize the SPLIM with the value 0x0FFE.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0x0800. This prevents the stack from interfering with the Special Function Register (SFR) space.

A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.





4.3 Instruction Addressing Modes

The addressing modes shown in Table 4-48 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.3.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a Working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire data space.

4.3.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where, Operand 1 is always a Working register (that is, the addressing mode can only be register direct), which is referred to as Wb. Operand 2 can be a W register, fetched from data memory, or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-bit or 10-bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	—	ADIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE
bit 15							bit 8
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IE	OC2IE	IC2IE	_	T1IE	OC1IE	IC1IE	INTOIE
bit 7	00111						bit C
Lovende							
Legena:	- h:4		L.14		a a value of the life in a ca	d a a (0)	
R = Readable			DIT	U = Unimpler	nented bit, rea	d as 'U'	
-n = value at	PUR	"I" = Bit is set	[$0^{\circ} = Bit is cie$	ared	X = BIT IS UNKN	own
bit 15-14	Unimplemer	nted: Read as '	0'				
bit 13	ADIE: ADC1	Conversion Co	omplete Interru	ipt Enable bit			
	1 = Interrupt 0 = Interrupt	request enable request not ena	d abled				
bit 12	U1TXIE: UA	RT1 Transmitte	r Interrupt Ena	ble bit			
	1 = Interrupt	request enable	d				
	0 = Interrupt	request not ena	abled				
bit 11	U1RXIE: UA	RT1 Receiver I	nterrupt Enabl	e bit			
	1 = Interrupt	request enable	d				
hit 10		Event Interrur	ableu ht Enable hit				
	1 = Interrupt	request enable	d				
	0 = Interrupt	request not en	abled				
bit 9	SPI1EIE: SP	11 Event Interru	upt Enable bit				
	1 = Interrupt 0 = Interrupt	request enable request not ena	d abled				
bit 8	T3IE: Timer3	Interrupt Enab	le bit				
	1 = Interrupt 0 = Interrupt	request enable request not ena	d abled				
bit 7	T2IE: Timer2	Interrupt Enab	le bit				
	1 = Interrupt 0 = Interrupt	request enable	d abled				
bit 6	OC2IE: Outp	ut Compare Ch	nannel 2 Interru	upt Enable bit			
	1 = Interrupt 0 = Interrupt	request enable	d abled				
bit 5		Capture Chann	el 2 Interrunt F	- nable bit			
	1 = Interrupt	request enable	d				
	0 = Interrupt	request not en	abled				
bit 4	Unimplemer	nted: Read as '	0'				
bit 3	T1IE: Timer1	Interrupt Enab	le bit				
	1 = Interrupt	request enable	d				
h it 0		request not ena		und Excelsion 1.11			
DIT 2	OCTIE: Outp	out Compare Ch	nannei 1 Interri	upt Enable bit			
	1 - Interrupt	roquest enable	d				

DECISTED 7-12 IECO INTERRIET ENABLE CONTROL DECISTER O

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 9	-3: PMD	3: PERIPHER	AL MODULE	DISABLE C	ONTROL RE	GISTER 3	
U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	—	—	—	—	CMPMD	—	_
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_	—	_	—	_
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	bit	U = Unimplem	nented bit, read	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own

bit 15-11	Unimplemented: Read as '0'
bit 10	CMPMD: Analog Comparator Module Disable bit
	1 = Analog comparator module is disabled
	0 = Analog comparator module is enabled
bit 9-0	Unimplemented: Read as '0'

REGISTER 9-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
—	—	—	—	REFOMD	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4	Unimplemented: Read as '0	,'
----------	---------------------------	----

bit 3 **REFOMD**: Reference Clock Generator Module Disable bit

1 = Reference clock generator module is disabled

- 0 = Reference clock generator module is enabled
- bit 2-0 Unimplemented: Read as '0'

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 10-5: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
—	—	—					—	
bit 15							bit 8	
U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	
	—	OCFAR5	OCFAR4	OCFAR3	OCFAR2	OCFAR1	OCFAR0	
bit 7			•			•	bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 Unimplemented: Read as '0'

bit 5-0

OCFAR<5:0>: Assign Output Capture A (OCFA) to the Corresponding RPn Pin bits

111111 = Input tied to Vss 100011 = Input tied to RP35 100010 = Input tied to RP34 100001 = Input tied to RP33 100000 = Input tied to RP32

•

00000 = Input tied to RP0

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	
	—	U1CTSR5	U1CTSR4	U1CTSR3	U1CTSR2	U1CTSR1	U1CTSR0	
bit 15							bit 8	
U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	
		U1RXR5	U1RXR4	U1RXR3	U1RXR2	U1RXR1	U1RXR0	
bit 7							bit 0	
F								
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'		
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown	
bit 15-14 bit 13-8	bit 15-14 Unimplemented: Read as '0' bit 13-8 U1CTSR<5:0>: Assign UART1 Clear-to-Send (U1CTS) to the Corresponding RPn Pin bits 111111 = Input tied to Vss 100011 = Input tied to RP35 100010 = Input tied to RP34 100001 = Input tied to RP32 • •						bits	
bit 7-6 bit 5-0	Unimplemented: Read as '0' U1RXR<5:0>: Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits 11111 = Input tied to Vss 100011 = Input tied to RP35 100010 = Input tied to RP34 100001 = Input tied to RP33 100000 = Input tied to RP32 •							

REGISTER 10-6: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP3R5	RP3R4	RP3R3	RP3R2	RP3R1	RP3R0
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

REGISTER 10-16: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13-8	RP3R<5:0>: Peripheral Output Function is Assigned to RP3 Output Pin bits (see Table 10-2 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	RP2R<5:0>: Peripheral Output Function is Assigned to RP2 Output Pin bits (see Table 10-2 for peripheral function numbers)

REGISTER 10-17: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP5R5	RP5R4	RP5R3	RP5R2	RP5R1	RP5R0
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP4R5	RP4R4	RP4R3	RP4R2	RP4R1	RP4R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

bit 7

bit 13-8 **RP5R<5:0>:** Peripheral Output Function is Assigned to RP5 Output Pin bits (see Table 10-2 for peripheral function numbers)

- bit 7-6 Unimplemented: Read as '0'
- bit 5-0 **RP4R<5:0>:** Peripheral Output Function is Assigned to RP4 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 0

REGISTER 17-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 5	ACKDT: Acknowledge Data bit (when operating as I ² C master, applicable during master receive)
	Value that is transmitted when the software initiates an Acknowledge sequence. 1 = Sends NACK during Acknowledge 0 = Sends ACK during Acknowledge
bit 4	ACKEN: Acknowledge Sequence Enable bit (when operating as I ² C master, applicable during master receive)
	 1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits the ACKDT data bit. Hardware is clear at end of master Acknowledge sequence. 0 = Acknowledge sequence is not in progress
bit 3	RCEN: Receive Enable bit (when operating as I ² C master)
	1 = Enables Receive mode for I^2C . Hardware is clear at end of eighth bit of master receive data byte. 0 = Receive sequence is not in progress
bit 2	PEN: Stop Condition Enable bit (when operating as I ² C master)
	1 = Initiates Stop condition on SDAx and SCLx pins. Hardware is clear at end of master Stop sequence.0 = Stop condition is not in progress
bit 1	RSEN: Repeated Start Condition Enable bit (when operating as I ² C master)
	1 = Initiates Repeated Start condition on SDAx and SCLx pins. Hardware is clear at end of master Repeated Start sequence.
	0 = Repeated Start condition is not in progress
bit 0	SEN: Start Condition Enable bit (when operating as I ² C master)
	1 = Initiates Start condition on SDAx and SCLx pins. Hardware is clear at end of master Start sequence.
	0 = Start condition is not in progress

DC CHARACTERISTICS			Standard ((unless of Operating	Operating Co herwise state temperature	nditions: 3.0V d) -40°C ≤ TA ≤ + -40°C ≤ TA ≤ +	to 3.6V 85°C for Industrial 125°C for Extended			
Parameter No.	Typical ⁽¹⁾	Мах	Units	Conditions					
Operating C	Operating Current (IDD) ⁽²⁾								
DC27d	111	140	mA	-40°C		40 MIPS			
DC27a	108	130	mA	+25°C	2 21/	See Note 2, except PWM is			
DC27b	105	130	mA	+85°C	5.5V	operating at 1/4 speed			
DC27c	103	130	mA	+125°C		(PTCON2 = 0x0002)			
DC28d	102	130	mA	-40°C		40 MIPS			
DC28a	100	120	mA	+25°C	2 21/	See Note 2, except PWM is			
DC28b	100	120	mA	+85°C	3.3V	operating at 1/8 speed			
DC28c	100	120	mA	+125°C		(PTCON2 = 0x0003)			

TABLE 24-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD) (CONTINUED)

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

• Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- CPU executing while(1) statement
- JTAG disabled
- **3:** These parameters are characterized but not tested in manufacturing.

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions	
	VIL	Input Low Voltage						
DI10		I/O Pins	Vss		0.2 Vdd	V		
DI15		MCLR	Vss	—	0.2 Vdd	V		
DI16		I/O Pins with OSC1	Vss	—	0.2 Vdd	V		
DI18		I/O Pins with SDAx, SCLx	Vss		0.3 Vdd	V	SMBus disabled	
DI19		I/O Pins with SDAx, SCLx	Vss	—	0.8	V	SMBus enabled	
	VIH	Input High Voltage						
DI20 DI21		I/O Pins Not 5V Tolerant ⁽⁴⁾ I/O Pins 5V Tolerant ⁽⁴⁾	0.7 Vdd 0.7 Vdd	— —	Vdd 5.5	V V		
DI28		SDA1, SCL1	0.7 VDD		5.5	V	SMBus disabled	
DI29		SDA1, SCL1	2.1		5.5	V	SMBus enabled	
	ICNPU	CNx Pull-up Current						
DI30		(234)		250		μA	VDD = 3.3V, VPIN = VSS	
DI50	IIL	I/O Pins with: 4x Driver Pins - RA0-RA2, RB0-RB2, RB5-RB10, RB15, RC1, RC2, RC9, RC10	_	_	±2	μΑ	Vss ≤ VPIN ≤ VDD, Pin at high-impedance	
		8x Driver Pins - RC0, RC3-RC8, RC11-RC13	_	—	±4	μA	$\label{eq:VSS} \begin{array}{l} VSS \leq VPIN \leq VDD, \\ Pin \text{ at high-impedance} \end{array}$	
		16x Driver Pins - RA3, RA4, RB3, RB4, RB11-RB14	_	_	±8	μA	$\label{eq:VSS} \begin{array}{l} \leq \mbox{VPIN} \leq \mbox{VDD}, \\ \mbox{Pin at high-impedance} \end{array}$	
DI55		MCLR	-	—	±2	μA	$Vss \leq V \text{PIN} \leq V \text{DD}$	
DI56		OSC1	—	—	±2	μA	VSS \leq VPIN \leq VDD, XT and HS modes	

TABLE 24-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

- 3: Negative current is defined as current sourced by the pin.
- 4: See "Pin Diagrams" for the list of 5V tolerant I/O pins.
- 5: VIL source < (Vss 0.3). Characterized but not tested.

6: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

- 7: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 8: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.
- **9:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.



FIGURE 24-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04



FIGURE 24-17: SPIX SLAVE MODE (FULL-DUPLEX CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

25.0 HIGH-TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

Note: Programming of the Flash memory is not allowed above +125°C.

The specifications between -40° C to $+150^{\circ}$ C are identical to those shown in **Section 24.0** "**Electrical Characteristics**" for operation between -40° C to $+125^{\circ}$ C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter DC10 in **Section 24.0 "Electrical Characteristics"** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 high-temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

40°C to +150°C
65°C to +160°C
0.3V to +4.0V
0.3V to (VDD + 0.3V)
0.3V to (VDD + 0.3V)
0.3V to 5.6V
60 mA
60 mA
+155°C
4 mA
8 mA
16 mA
180 mA
180 mA

- **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.
 - 2: Maximum allowable current is a function of device maximum power dissipation (see Table 25-2).
 - **3:** AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.
 - 4: Refer to the "Pin Diagrams" section for 5V tolerant pins.

25.1 High-Temperature DC Characteristics

TABLE 25-1: OPERATING MIPS VS. VOLTAGE

	Voo Bango	Tomporaturo Pango	Max MIPS		
Characteristic	(in Volts)	(in °C)	dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04		
_	3.0V to 3.6V ⁽¹⁾	-40°C to +150°C	20		

Note 1: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested but not characterized. All device analog modules such as the ADC, etc., will function but with degraded performance below VDDMIN. Refer to Parameter BO10 in Table 24-11 for BOR values.

TABLE 25-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Тур	Max	Unit
High-Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+155	°C
Operating Ambient Temperature Range	TA	-40	—	+150	°C
Power Dissipation: Internal chip power dissipation: $PINT = VDD x (IDD - \Sigma IOH)$ I/O Pin Power Dissipation: $I/O = \Sigma (\{VDD - VOH\} x IOH) + \Sigma (VOL x IOL)$		PINT + PI/O		W	
Maximum Allowed Power Dissipation		(Тј - Та)/θја			W

TABLE 25-3: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARA	Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature						
Parameter No. Symbol Characteristic			Min	Тур	Max	Units	Conditions
Operating V	Voltage						
HDC10	Supply Voltage						
	Vdd		3.0	3.3	3.6	V	-40°C to +150°C

28-Lead Plastic Quad Flat, No Lead Package (MX) - 6x6x0.5mm Body [UQFN] Ultra-Thin with 0.40 x 0.60 mm Terminal Width/Length and Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimensior	n Limits	MIN	NOM	MAX	
Number of Pins	N	28			
Pitch	е	0.65 BSC			
Overall Height	Α	0.40	0.50	0.60	
Standoff	A1	0.00	0.02	0.05	
Terminal Thickness	(A3)	0.127 REF			
Overall Width		6.00 BSC			
Exposed Pad Width	E2		4.00		
Overall Length	D	6.00 BSC			
Exposed Pad Length	D2		4.00		
Terminal Width	b	0.35	0.40	0.45	
Corner Pad	b2	0.25	0.40	0.45	
Terminal Length	L	0.55	0.60	0.65	
Terminal-to-Exposed Pad	K	0.20	-	-	

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated
- 3. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.
- 4. Outermost portions of corner structures may vary slightly.

Microchip Technology Drawing C04-0209B Sheet 2 of 2

Revision F (January 2012)

All occurrences of VDDCORE have been removed throughout the document.

This revision also includes minor typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in the following table.

TABLE A-4: MAJOR SECTION UPDATES

Section Name	Update Description				
"16-Bit Digital Signal Controllers (up to 16-Kbyte Flash and up to 2-Kbyte SRAM) with High-Speed PWM, ADC and Comparators"	Added the VTLA package to the dsPIC33FJ16GS404 and dsPIC33FJ16GS504 devices (see TABLE 1: "dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Controller Families").				
	Added the "Referenced Sources" section.				
	The following updates were made to the "Pin Diagrams" section:				
	 Added 5V tolerant pin shading to pins 24-26 in the 28-pin SPDIP, SOIC package for the dsPIC33FJ16GS402 				
	• Updated pin 31 of the 44-pin QFN package for the dsPIC33FJ16GS404				
	 Added VTLA pin diagrams for the dsPIC33FJ16GS404 and dsPIC33FJ16GS504 devices 				
Section 1.0 "Device Overview"	Removed the Precision Band Gap Reference from the device block diagram (see Figure 1-1).				
	Updated the Pinout I/O Descriptions for AVDD, and AVSS (see Table 1-1).				
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers"	Updated the Minimum Recommended Connection (see Figure 2-1).				
Section 8.0 "Oscillator	Updated the Oscillator System Diagram (see Figure 8-1).				
Configuration	Added auxiliary clock configuration restrictions in Section 8.2 "Auxiliary Clock Generation ".				
	Updated or added notes regarding register reset on a POR (see Register 8-1 through Register 8-5).				
Section 19.0 "High-Speed 10-bit Analog-to-Digital Converter (ADC)"	Added Note 2 to ADCON: Analog-to-Digital Control Register (see Register 19-1).				
	Removed all notes from ADSTAT: Analog-to-Digital Status Register (see Register 19-2).				
Section 20.0 "High-Speed Analog Comparator"	Updated the Comparator Module Block Diagram (see Figure 20-1).				
Section 21.0 "Special Features"	Add a new paragraph at the beginning of Section 21.1 " Configuration Bits ".				
	Added the RTSP Effect column to the dsPIC33F Configuration Bits Description table (see Table 21-2).				
	Updated the Connections for the On-chip Voltage Regulator diagram (see Figure 21-1).				
	Updated the first paragraph of Section 21.7 "In-Circuit Debugger".				