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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gs404-i-pt

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

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dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS Capable	Description
CMP1A	I	Analog	No	Comparator 1 Channel A.
CMP1B	I	Analog	No	Comparator 1 Channel B.
CMP1C	I	Analog	No	Comparator 1 Channel C.
CMP1D	I	Analog	No	Comparator 1 Channel D.
CMP2A	I	Analog	No	Comparator 2 Channel A.
CMP2B	I	Analog	No	Comparator 2 Channel B.
CMP2C	I	Analog	No	Comparator 2 Channel C.
CMP2D	I	Analog	No	Comparator 2 Channel D.
CMP3A	I	Analog	No	Comparator 3 Channel A.
CMP3B	I	Analog	No	Comparator 3 Channel B.
CMP3C	I	Analog	No	Comparator 3 Channel C.
CMP3D	I	Analog	No	Comparator 3 Channel D.
CMP4A	I	Analog	No	Comparator 4 Channel A.
CMP4B	I	Analog	No	Comparator 4 Channel B.
CMP4C	I	Analog	No	Comparator 4 Channel C.
CMP4D	I	Analog	No	Comparator 4 Channel D.
DACOUT	O	—	No	DAC output voltage.
ACMP1-ACMP4	O	—	Yes	DAC trigger to PWM module.
EXTREF	I	Analog	No	External voltage reference input for the reference DACs.
REFCLKO	O	—	Yes	REFCLKO output signal is a postscaled derivative of the system clock.
FLT1-FLT8	I	ST	Yes	Fault Inputs to PWM module.
SYNCI1-SYNCI2	I	ST	Yes	External synchronization signal to PWM master time base.
SYNCO1	O	—	Yes	PWM master time base for external device synchronization.
PWM1L	O	—	No	PWM1 low output.
PWM1H	O	—	No	PWM1 high output.
PWM2L	O	—	No	PWM2 low output.
PWM2H	O	—	No	PWM2 high output.
PWM3L	O	—	No	PWM3 low output.
PWM3H	O	—	No	PWM3 high output.
PWM4L	O	—	Yes	PWM4 low output.
PWM4H	O	—	Yes	PWM4 high output.
PGED1	I/O	ST	No	Data I/O pin for programming/debugging Communication Channel 1.
PGEC1	I	ST	No	Clock input pin for programming/debugging Communication Channel 1.
PGED2	I/O	ST	No	Data I/O pin for programming/debugging Communication Channel 2.
PGEC2	I	ST	No	Clock input pin for programming/debugging Communication Channel 2.
PGED3	I/O	ST	No	Data I/O pin for programming/debugging Communication Channel 3.
PGEC3	I	ST	No	Clock input pin for programming/debugging Communication Channel 3.
MCLR	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	P	P	No	Positive supply for analog modules. This pin must be connected at all times. AVDD is connected to VDD.
AVSS	P	P	No	Ground reference for analog modules. AVSS is connected to VSS.
VDD	P	—	No	Positive supply for peripheral logic and I/O pins.
VCAP	P	—	No	CPU logic filter capacitor connection.
VSS	P	—	No	Ground reference for logic and I/O pins.

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-Transistor Logic

Analog = Analog input

P = Power

PPS = Peripheral Pin Select

I = Input

O = Output

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

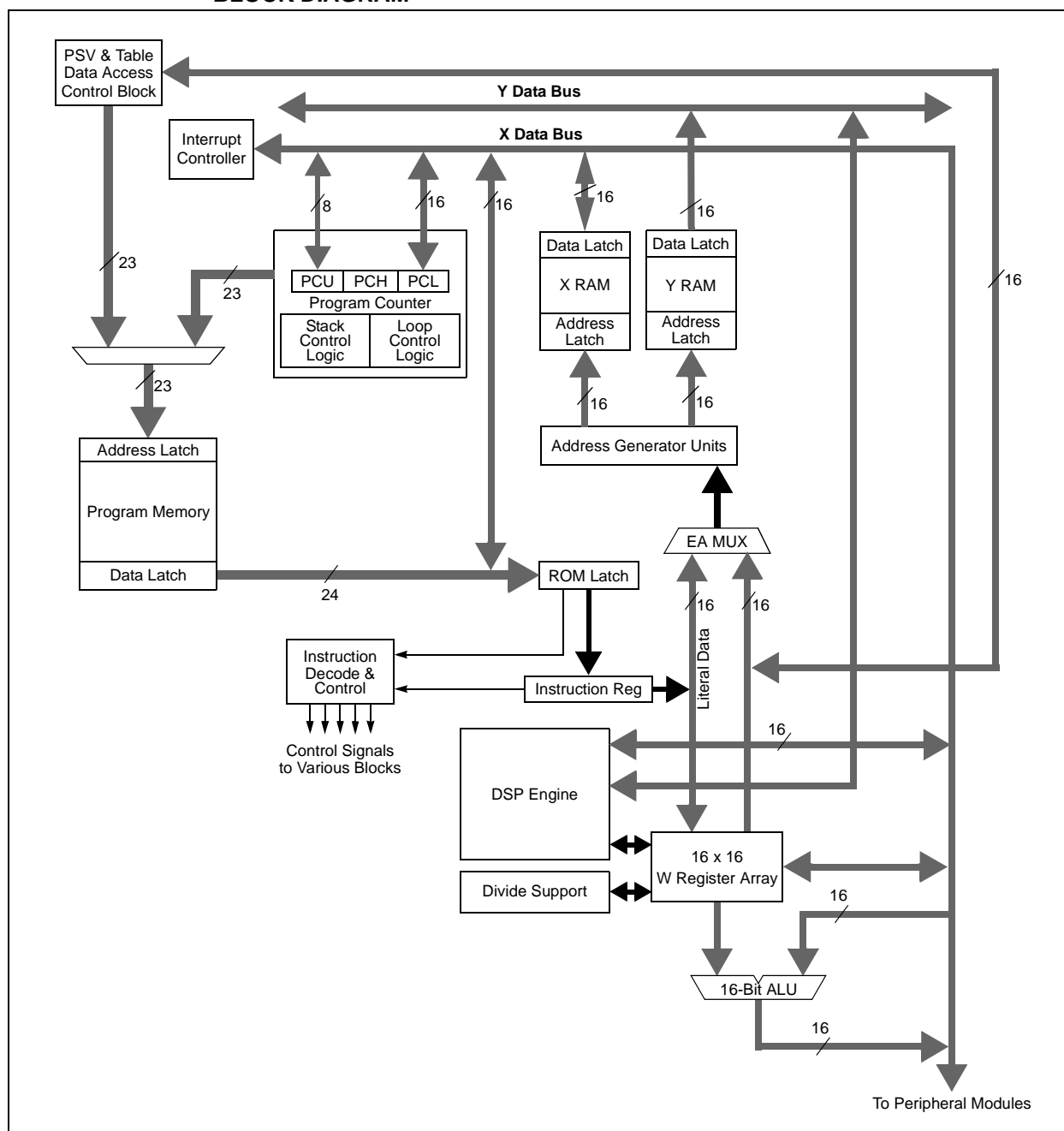
3.3 Special MCU Features

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices feature a 17-bit by 17-bit single-cycle multiplier that is shared by both the MCU ALU and DSP engine. The multiplier can perform signed, unsigned and mixed sign multiplication. Using a 17-bit by 17-bit multiplier for 16-bit by 16-bit multiplication not only allows you to perform mixed sign multiplication, it also achieves accurate results for special operations, such as $(-1.0) \times (1.0)$.

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices support 16/16 and 32/16 divide operations, both fractional and integer. All divide instructions are iterative operations. They must be executed within a REPEAT loop, resulting in a total execution time of 19 instruction cycles. The divide operation can be interrupted during any of those 19 cycles without loss of data.

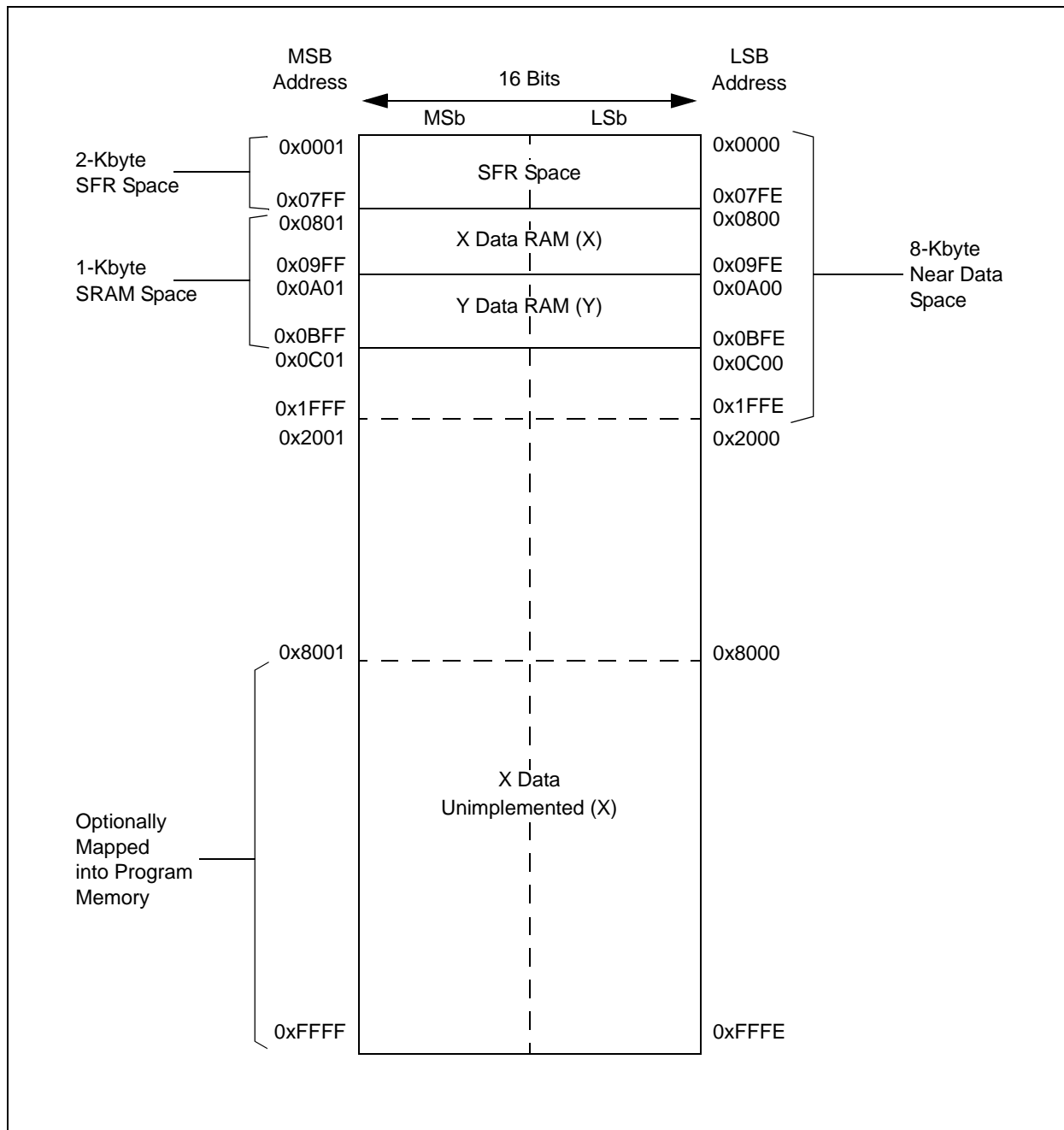
A 40-bit barrel shifter is used to perform up to a 16-bit left or right shift in a single cycle. The barrel shifter can be used by both MCU and DSP instructions.

FIGURE 3-1: dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 CPU CORE BLOCK DIAGRAM



dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

FIGURE 4-4: DATA MEMORY MAP FOR dsPIC33FJ06GS202 DEVICE WITH 1-KBYTE RAM



dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

FIGURE 4-5: DATA MEMORY MAP FOR dsPIC33FJ16GS402/404/502/504 DEVICES WITH 2-KBYTE RAM

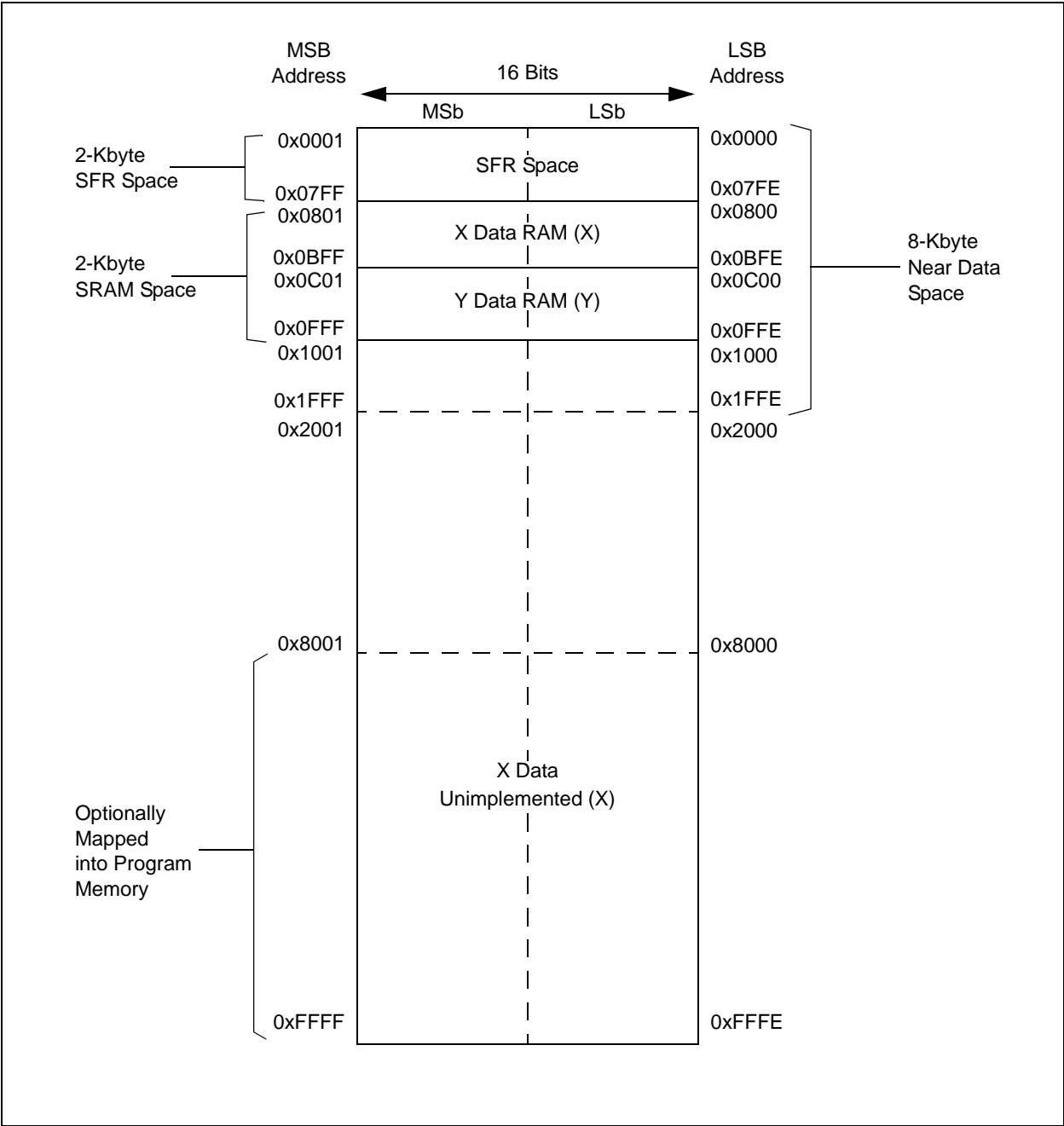


TABLE 4-22: I2C1 REGISTER MAP

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	0200	—	—	—	—	—	—	—	—	I2C1 Receive Register								0000
I2C1TRN	0202	—	—	—	—	—	—	—	—	I2C1 Transmit Register								00FF
I2C1BRG	0204	—	—	—	—	—	—	—	Baud Rate Generator Register									0000
I2C1CON	0206	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1STAT	0208	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
I2C1ADD	020A	—	—	—	—	—	—	I2C1 Address Register										0000
I2C1MSK	020C	—	—	—	—	—	—	AMSK<9:0>										0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-23: UART1 REGISTER MAP

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART1 Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	0228	Baud Rate Generator Prescaler																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-24: SPI1 REGISTER MAP

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	—	—	—	—	SPIROV	—	—	—	—	SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	—	0000
SPI1BUF	0248	SPI1 Transmit and Receive Buffer Register																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-31: ANALOG COMPARATOR CONTROL REGISTER MAP FOR dsPIC33FJ06GS202 DEVICES ONLY

File Name	ADR	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMPCON1	0540	CMPON	—	CMPSIDL	—	—	—	—	DACOE	INSEL1	INSEL0	EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC1	0542	—	—	—	—	—	—	CMREF<9:0>										0000
CMPCON2	0544	CMPON	—	CMPSIDL	—	—	—	—	DACOE	INSEL1	INSEL0	EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC2	0546	—	—	—	—	—	—	CMREF<9:0>										0000

TABLE 4-32: ANALOG COMPARATOR CONTROL REGISTER MAP dsPIC33FJ16GS502/504 DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMPCON1	0540	CMPON	—	CMPSIDL	—	—	—	—	DACOE	INSEL1	INSEL0	EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC1	0542	—	—	—	—	—	—	CMREF<9:0>										0000
CMPCON2	0544	CMPON	—	CMPSIDL	—	—	—	—	DACOE	INSEL1	INSEL0	EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC2	0546	—	—	—	—	—	—	CMREF<9:0>										0000
CMPCON3	0548	CMPON	—	CMPSIDL	—	—	—	—	DACOE	INSEL1	INSEL0	EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC3	054A	—	—	—	—	—	—	CMREF<9:0>										0000
CMPCON4	054C	CMPON	—	CMPSIDL	—	—	—	—	DACOE	INSEL1	INSEL0	EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC4	054E	—	—	—	—	—	—	CMREF<9:0>										0000

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

4.2.6 SOFTWARE STACK

In addition to its use as a Working register, the W15 register in the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices is also used as a software Stack Pointer. The Stack Pointer always points to the first available free word and grows from lower to higher addresses. It predecrements for stack pops and post-increments for stack pushes, as shown in Figure 4-6. For a PC push during any CALL instruction, the MSb of the PC is zero-extended before the push, ensuring that the MSb is always clear.

Note: A PC push during exception processing concatenates the SRL register to the MSb of the PC prior to the push.

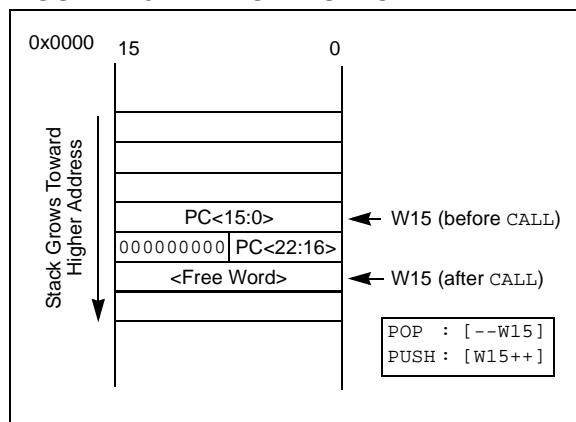
The Stack Pointer Limit register (SPLIM) associated with the Stack Pointer sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' because all stack operations must be word-aligned.

Whenever an EA is generated using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal and a push operation is performed, a stack error trap will not occur. The stack error trap will occur on a subsequent push operation. For example, to cause a stack error trap when the stack grows beyond address 0x1000 in RAM, initialize the SPLIM with the value 0x0FFE.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0x0800. This prevents the stack from interfering with the Special Function Register (SFR) space.

A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

FIGURE 4-6: CALL STACK FRAME



4.3 Instruction Addressing Modes

The addressing modes shown in Table 4-48 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.3.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a Working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire data space.

4.3.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where, Operand 1 is always a Working register (that is, the addressing mode can only be register direct), which is referred to as Wb. Operand 2 can be a W register, fetched from data memory, or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-bit or 10-bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

4.6.3 READING DATA FROM PROGRAM MEMORY USING PROGRAM SPACE VISIBILITY

The upper 32 Kbytes of data space may optionally be mapped into any 16K word page of the program space. This option provides transparent access to stored constant data from the data space without the need to use special instructions (such as `TBLRD/L/H`).

Program space access through the data space occurs if the Most Significant bit of the data space EA is '1' and Program Space Visibility (PSV) is enabled by setting the PSV bit in the Core Control register (`CORCON<2>`). The location of the program memory space to be mapped into the data space is determined by the Program Space Visibility Page register (`PSVPAG`). This 8-bit register defines any one of 256 possible pages of 16K words in program space. In effect, `PSVPAG` functions as the upper 8 bits of the program memory address, with the 15 bits of the EA functioning as the lower bits. By incrementing the PC by 2 for each program memory word, the lower 15 bits of data space addresses directly map to the lower 15 bits in the corresponding program space addresses.

Data reads to this area add a cycle to the instruction being executed, since two program memory fetches are required.

Although each data space address 8000h and higher maps directly into a corresponding program memory address (see Figure 4-11), only the lower 16 bits of the

24-bit program word are used to contain the data. The upper 8 bits of any program space location used as data should be programmed with '1111 1111' or '0000 0000' to force a NOP. This prevents possible issues should the area of code ever be accidentally executed.

Note: PSV access is temporarily disabled during Table Reads/Writes.

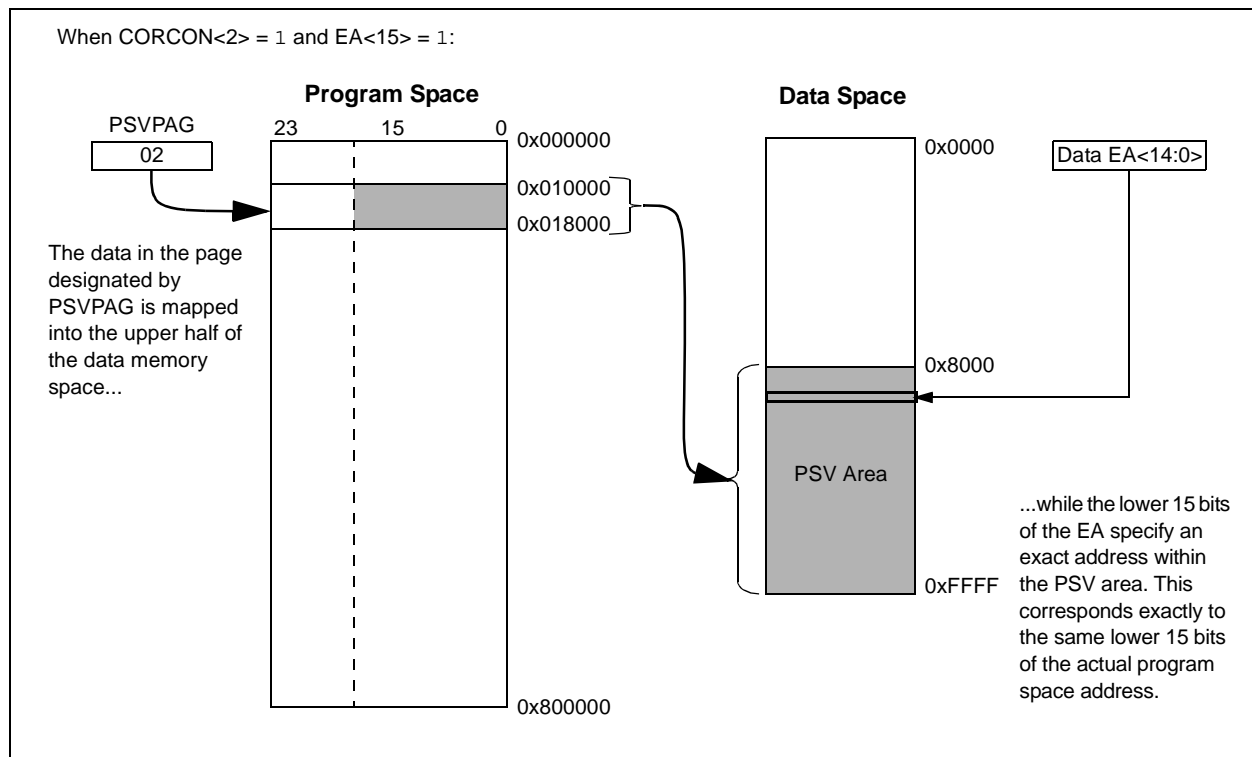
For operations that use PSV and are executed outside a `REPEAT` loop, the `MOV` and `MOV.D` instructions require one instruction cycle in addition to the specified execution time. All other instructions require two instruction cycles in addition to the specified execution time.

For operations that use PSV, and are executed inside a `REPEAT` loop, these instances require two instruction cycles in addition to the specified execution time of the instruction:

- Execution in the first iteration
- Execution in the last iteration
- Execution prior to exiting the loop due to an interrupt
- Execution upon re-entering the loop after an interrupt is serviced

Any other iteration of the `REPEAT` loop will allow the instruction using PSV to access data, to execute in a single cycle.

FIGURE 4-11: PROGRAM SPACE VISIBILITY OPERATION



dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

6.8.2 UNINITIALIZED W REGISTER RESET

Any attempt to use the Uninitialized W register as an Address Pointer will reset the device. The W register array (with the exception of W15) is cleared during all Resets and is considered uninitialized until written to.

6.8.3 SECURITY RESET

If a Program Flow Change (PFC) or Vector Flow Change (VFC) targets a restricted location in a protected segment (boot and secure segment), that operation will cause a Security Reset.

The PFC occurs when the Program Counter is reloaded as a result of a call, jump, computed jump, return, return from subroutine or other form of branch instruction.

The VFC occurs when the Program Counter is reloaded with an interrupt or trap vector.

Refer to **Section 21.8 “Code Protection and CodeGuard™ Security”** for more information on Security Reset.

6.9 Using the RCON Status Bits

The user application can read the Reset Control (RCON) register after any device Reset to determine the cause of the Reset.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

Table 6-3 provides a summary of the Reset flag bit operation.

TABLE 6-3: RESET FLAG BIT OPERATION

Flag Bit	Set by:	Cleared by:
TRAPR (RCON<15>)	Trap conflict event	POR, BOR
IOPWR (RCON<14>)	Illegal opcode or Uninitialized W register access or Security Reset	POR, BOR
CM (RCON<9>)	Configuration Mismatch	POR, BOR
EXTR (RCON<7>)	MCLR Reset	POR
SWR (RCON<6>)	RESET instruction	POR, BOR
WDTO (RCON<4>)	WDT time-out	PWRSV instruction, CLRWDT instruction, POR, BOR
SLEEP (RCON<3>)	PWRSV #SLEEP instruction	POR, BOR
IDLE (RCON<2>)	PWRSV #IDLE instruction	POR, BOR
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR	—

Note: All Reset flag bits can be set or cleared by user software.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

TABLE 7-1: INTERRUPT VECTORS

Vector Number	Interrupt Request (IQR)	IVT Address	AIVT Address	Interrupt Source
Highest Natural Order Priority				
8	0	0x000014	0x000114	INT0 – External Interrupt 0
9	1	0x000016	0x000116	IC1 – Input Capture 1
10	2	0x000018	0x000118	OC1 – Output Compare 1
11	3	0x00001A	0x00011A	T1 – Timer1
12	4	0x00001C	0x00011C	Reserved
13	5	0x00001E	0x00011E	IC2 – Input Capture 2
14	6	0x000020	0x000120	OC2 – Output Compare 2
15	7	0x000022	0x000122	T2 – Timer2
16	8	0x000024	0x000124	T3 – Timer3
17	9	0x000026	0x000126	SPI1E – SPI1 Fault
18	10	0x000028	0x000128	SPI1 – SPI1 Transfer Done
19	11	0x00002A	0x00012A	U1RX – UART1 Receiver
20	12	0x00002C	0x00012C	U1TX – UART1 Transmitter
21	13	0x00002E	0x00012E	ADC – ADC Group Convert Done
22-23	14-15	0x000030-0x000032	0x000130-0x000132	Reserved
24	16	0x000034	0x000134	SI2C1 – I2C1 Slave Event
25	17	0x000036	0x000136	MI2C1 – I2C1 Master Event
26	18	0x000038	0x000138	CMP1 – Analog Comparator 1 Interrupt
27	19	0x00003A	0x00013A	CN – Input Change Notification Interrupt
28	20	0x00003C	0x00013C	INT1 – External Interrupt 1
29-36	21-28	0x00003E-0x00004C	0x00013E-0x00014C	Reserved
37	29	0x00004E	0x00014E	INT2 – External Interrupt 2
38-64	30-56	0x000050-0x000084	0x000150-0x000184	Reserved
65	57	0x000086	0x000186	PWM PSEM Special Event Match
66-72	58-64	0x000088-0x000094	0x000188-0x000194	Reserved
73	65	0x000096	0x000196	U1E – UART1 Error Interrupt
74-101	66-93	0x000098-0x0000CE	0x000198-0x0001CE	Reserved
102	94	0x0000D0	0x0001D0	PWM1 – PWM1 Interrupt
103	95	0x0000D2	0x0001D2	PWM2 – PWM2 Interrupt
104	96	0x0000D4	0x0001D4	PWM3 – PWM3 Interrupt
105	97	0x0000D6	0x0001D6	PWM4 – PWM4 Interrupt
106-110	98-102	0x0000D8-0x0000E0	0x0001D8-0x0001E0	Reserved
111	103	0x0000E2	0x0001E2	CMP2 – Analog Comparator 2
112	104	0x0000E4	0x0001E4	CMP3 – Analog Comparator 3
113	105	0x0000E6	0x0001E6	CMP4 – Analog Comparator 4
114-117	106-109	0x0000E8-0x0000EE	0x0001E8-0x0001EE	Reserved
118	110	0x0000F0	0x0001F0	ADC Pair 0 Convert Done
119	111	0x0000F2	0x0001F2	ADC Pair 1 Convert Done
120	112	0x0000F4	0x0001F4	ADC Pair 2 Convert Done
121	113	0x0000F6	0x0001F6	ADC Pair 3 Convert Done
122	114	0x0000F8	0x0001F8	ADC Pair 4 Convert Done
123	115	0x0000FA	0x0001FA	ADC Pair 5 Convert Done
124	116	0x0000FC	0x0001FC	ADC Pair 6 Convert Done
125	117	0x0000FE	0x0001FE	Reserved
Lowest Natural Order Priority				

7.3 Interrupt Control and Status Registers

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices implement 27 registers for the interrupt controller:

- INTCON1
- INTCON2
- IFSx
- IECx
- IPCx
- INTTREG

7.3.1 INTCON1 AND INTCON2

Global interrupt control functions are controlled from INTCON1 and INTCON2. INTCON1 contains the Interrupt Nesting Disable (NSTDIS) bit as well as the control and status flags for the processor trap sources. The INTCON2 register controls the external interrupt request signal behavior and the use of the Alternate Interrupt Vector Table.

7.3.2 IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

7.3.3 IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

7.3.4 IPCx

The IPCx registers are used to set the Interrupt Priority Level for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

7.3.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number (VECNUM<6:0>) and Interrupt Level (ILR<3:0>) bit fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence that they are listed in Table 7-1. For example, the INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit is found in IEC0<0> and the INT0IP bits are found in the first position of IPC0 (IPC0<2:0>).

7.3.6 STATUS/CONTROL REGISTERS

Although they are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality.

- The CPU STATUS Register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU Interrupt Priority Level. The user can change the current CPU priority level by writing to the IPL bits.
- The CORCON register contains the IPL3 bit, which together with IPL<2:0>, indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 7-1 through Register 7-35 in the following pages.

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REGISTER 7-10: IFS6: INTERRUPT FLAG STATUS REGISTER 6

R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
ADCP1IF	ADCP0IF	—	—	—	—	AC4IF	AC3IF
bit 15						bit 8	

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
AC2IF	—	—	—	—	—	PWM4IF	PWM3IF
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ADCP1IF:** ADC Pair 1 Conversion Done Interrupt Flag Status bit

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

bit 14 **ADCP0IF:** ADC Pair 0 Conversion Done Interrupt Flag Status bit

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

bit 13-10 **Unimplemented:** Read as '0'

bit 9 **AC4IF:** Analog Comparator 4 Interrupt Flag Status bit

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

bit 8 **AC3IF:** Analog Comparator 3 Interrupt Flag Status bit

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

bit 7 **AC2IF:** Analog Comparator 2 Interrupt Flag Status bit

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

bit 6-2 **Unimplemented:** Read as '0'

bit 1 **PWM4IF:** PWM4 Interrupt Flag Status bit

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

bit 0 **PWM3IF:** PWM3 Interrupt Flag Status bit

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

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REGISTER 10-6: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	U1CTSR5	U1CTSR4	U1CTSR3	U1CTSR2	U1CTSR1	U1CTSR0
bit 15						bit 8	

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	U1RXR5	U1RXR4	U1RXR3	U1RXR2	U1RXR1	U1RXR0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **U1CTSR<5:0>:** Assign UART1 Clear-to-Send (U1CTS) to the Corresponding RPn Pin bits

111111 = Input tied to Vss

100011 = Input tied to RP35

100010 = Input tied to RP34

100001 = Input tied to RP33

100000 = Input tied to RP32

•

•

•

00000 = Input tied to RP0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **U1RXR<5:0>:** Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits

111111 = Input tied to Vss

100011 = Input tied to RP35

100010 = Input tied to RP34

100001 = Input tied to RP33

100000 = Input tied to RP32

•

•

•

00000 = Input tied to RP0

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TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
48	MPY	MPY $Wm * Wn, Acc, Wx, Wxd, Wy, Wyd$	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
		MPY $Wm * Wm, Acc, Wx, Wxd, Wy, Wyd$	Square Wm to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
49	MPY.N	MPY.N $Wm * Wn, Acc, Wx, Wxd, Wy, Wyd$	-(Multiply Wm by Wn) to Accumulator	1	1	None
50	MSC	MSC $Wm * Wm, Acc, Wx, Wxd, Wy, Wyd, AWB$	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
51	MUL	MUL.SS Wb, Ws, Wnd	$\{Wnd + 1, Wnd\} = \text{signed}(Wb) * \text{signed}(Ws)$	1	1	None
		MUL.SU Wb, Ws, Wnd	$\{Wnd + 1, Wnd\} = \text{signed}(Wb) * \text{unsigned}(Ws)$	1	1	None
		MUL.US Wb, Ws, Wnd	$\{Wnd + 1, Wnd\} = \text{unsigned}(Wb) * \text{signed}(Ws)$	1	1	None
		MUL.UU Wb, Ws, Wnd	$\{Wnd + 1, Wnd\} = \text{unsigned}(Wb) * \text{unsigned}(Ws)$	1	1	None
		MUL.SU $Wb, \#lit5, Wnd$	$\{Wnd + 1, Wnd\} = \text{signed}(Wb) * \text{unsigned}(lit5)$	1	1	None
		MUL.UU $Wb, \#lit5, Wnd$	$\{Wnd + 1, Wnd\} = \text{unsigned}(Wb) * \text{unsigned}(lit5)$	1	1	None
		MUL f	$W3:W2 = f * WREG$	1	1	None
52	NEG	NEG Acc	Negate Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
		NEG f	$f = \bar{f} + 1$	1	1	C,DC,N,OV,Z
		NEG $f, WREG$	$WREG = \bar{f} + 1$	1	1	C,DC,N,OV,Z
		NEG Ws, Wd	$Wd = \overline{Ws} + 1$	1	1	C,DC,N,OV,Z
53	NOP	NOP	No Operation	1	1	None
		NOPR	No Operation	1	1	None
54	POP	POP f	Pop f from Top-of-Stack (TOS)	1	1	None
		POP Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
		POP.D Wnd	Pop from Top-of-Stack (TOS) to $W(nd):W(nd + 1)$	1	2	None
		POP.S	Pop Shadow Registers	1	1	All
55	PUSH	PUSH f	Push f to Top-of-Stack (TOS)	1	1	None
		PUSH Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
		PUSH.D Wns	Push $W(ns):W(ns + 1)$ to Top-of-Stack (TOS)	1	2	None
		PUSH.S	Push Shadow Registers	1	1	None
56	PWRSV	PWRSV $\#lit1$	Go into Sleep or Idle mode	1	1	WDTO,Sleep
57	RCALL	RCALL $Expr$	Relative Call	1	2	None
		RCALL Wn	Computed Call	1	2	None
58	REPEAT	REPEAT $\#lit14$	Repeat Next Instruction $lit14 + 1$ times	1	1	None
		REPEAT Wn	Repeat Next Instruction $(Wn) + 1$ times	1	1	None
59	RESET	RESET	Software Device Reset	1	1	None
60	RETFIE	RETFIE	Return from interrupt	1	3 (2)	None
61	RETLW	RETLW $\#lit10, Wn$	Return with Literal in Wn	1	3 (2)	None
62	RETURN	RETURN	Return from Subroutine	1	3 (2)	None
63	RLC	RLC f	$f = \text{Rotate Left through Carry } f$	1	1	C,N,Z
		RLC $f, WREG$	$WREG = \text{Rotate Left through Carry } f$	1	1	C,N,Z
		RLC Ws, Wd	$Wd = \text{Rotate Left through Carry } Ws$	1	1	C,N,Z
64	RLNC	RLNC f	$f = \text{Rotate Left (No Carry) } f$	1	1	N,Z
		RLNC $f, WREG$	$WREG = \text{Rotate Left (No Carry) } f$	1	1	N,Z
		RLNC Ws, Wd	$Wd = \text{Rotate Left (No Carry) } Ws$	1	1	N,Z
65	RRC	RRC f	$f = \text{Rotate Right through Carry } f$	1	1	C,N,Z
		RRC $f, WREG$	$WREG = \text{Rotate Right through Carry } f$	1	1	C,N,Z
		RRC Ws, Wd	$Wd = \text{Rotate Right through Carry } Ws$	1	1	C,N,Z

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25.2 AC Characteristics and Timing Parameters

The information contained in this section defines dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 AC characteristics and timing parameters for high-temperature devices. However, all AC timing specifications in this section are the same as those in **Section 24.2 “AC Characteristics and Timing Parameters”**, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter OS53 in **Section 24.2 “AC Characteristics and Timing Parameters”** is the Industrial and Extended temperature equivalent of HOS53.

TABLE 25-7: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)
	Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature Operating voltage V_{DD} range as described in Table 25-1.

FIGURE 25-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

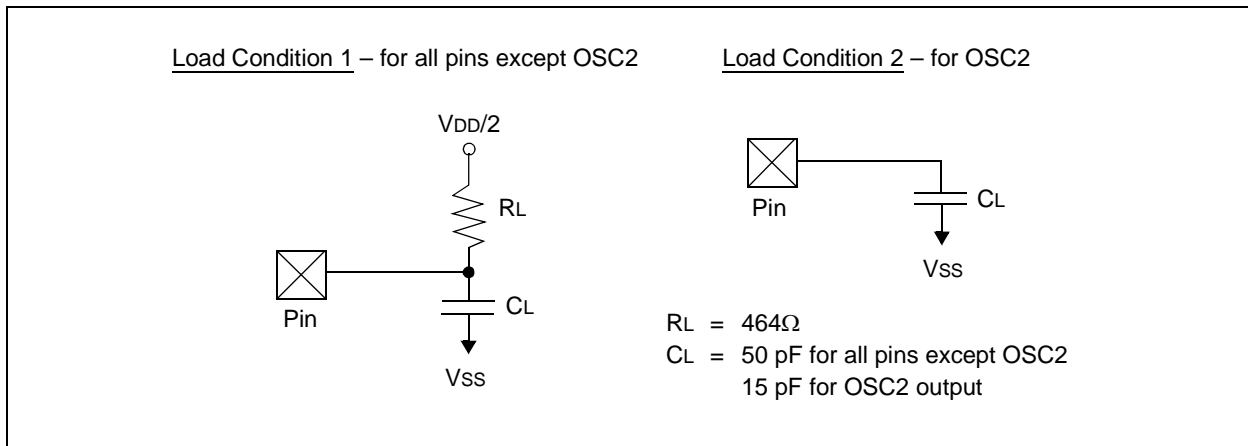


TABLE 25-8: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)					
		Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
HOS53	DCLK	CLKO Stability (Jitter) ⁽¹⁾	-5	0.5	5	%	Measured over 100 ms period

Note 1: These parameters are characterized, but are not tested in manufacturing.

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TABLE 25-11: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ	Max	Units	Conditions
HSP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	35	ns	
HSP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	25	—	—	ns	
HSP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	25	—	—	ns	
HSP51	TssH2doZ	$\overline{\text{SS}}_x \uparrow$ to SDOx Output High-Impedance	15	—	55	ns	See Note 2

Note 1: These parameters are characterized but not tested in manufacturing.

2: Assumes 50 pF load on all SPIx pins.

TABLE 25-12: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ	Max	Units	Conditions
HSP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	35	ns	
HSP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	25	—	—	ns	
HSP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	25	—	—	ns	
HSP51	TssH2doZ	$\overline{\text{SS}}_x \uparrow$ to SDOx Output High-Impedance	15	—	55	ns	See Note 2
HSP60	TssL2doV	SDOx Data Output Valid after $\overline{\text{SS}}_x$ Edge	—	—	55	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Assumes 50 pF load on all SPIx pins.

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TABLE 26-3: DC CHARACTERISTICS: IDLE CURRENT (IDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial		
Parameter No.	Typical	Max	Units	Conditions	
Idle Current (IDLE): Core Off, Clock On Base Current ⁽¹⁾					
MDC45d	64	105	mA	-40°C	3.3V 50 MIPS
MDC45a	64	105	mA	+25°C	
MDC45b	64	105	mA	+85°C	

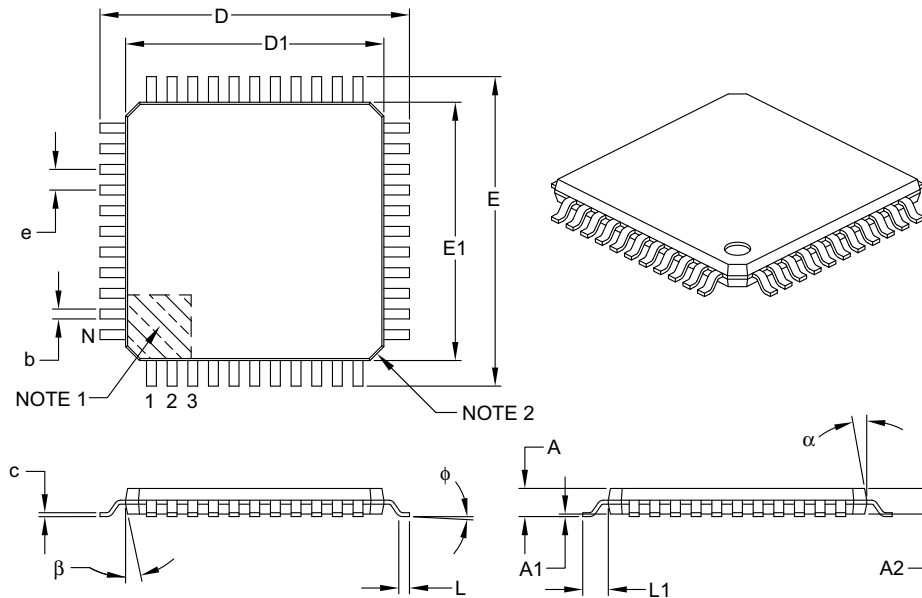
Note 1: Base Idle current (IDLE) is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}} = \text{VDD}$, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- JTAG is disabled

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44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Leads	N	44		
Lead Pitch	e	0.80 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	12.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

Revision G (May 2014)

The values for the TUN<5:0> bits in Register 8-4 (OSCTUN) have changed.

The DC Characteristics Idle Current values in **Section 24.0 “Electrical Characteristics”** have been updated.

The timer specifications in **Section 26.0 “50 MIPS Electrical Characteristics”** have been removed.

All diagrams in **Section 28.0 “Packaging Information”** have been updated.

Minor text edits have been applied throughout the document.