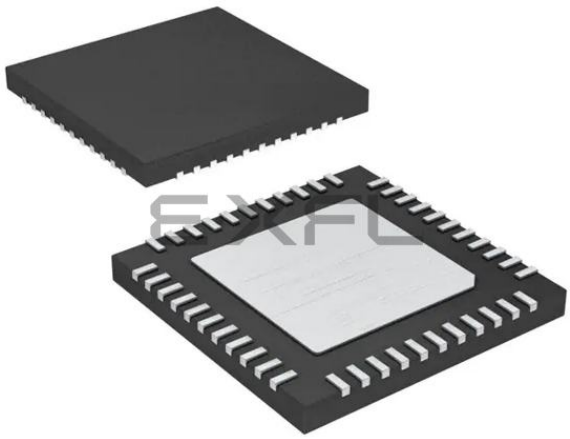
Microchip Technology - DSPIC33FJ16GS404T-I/ML Datasheet



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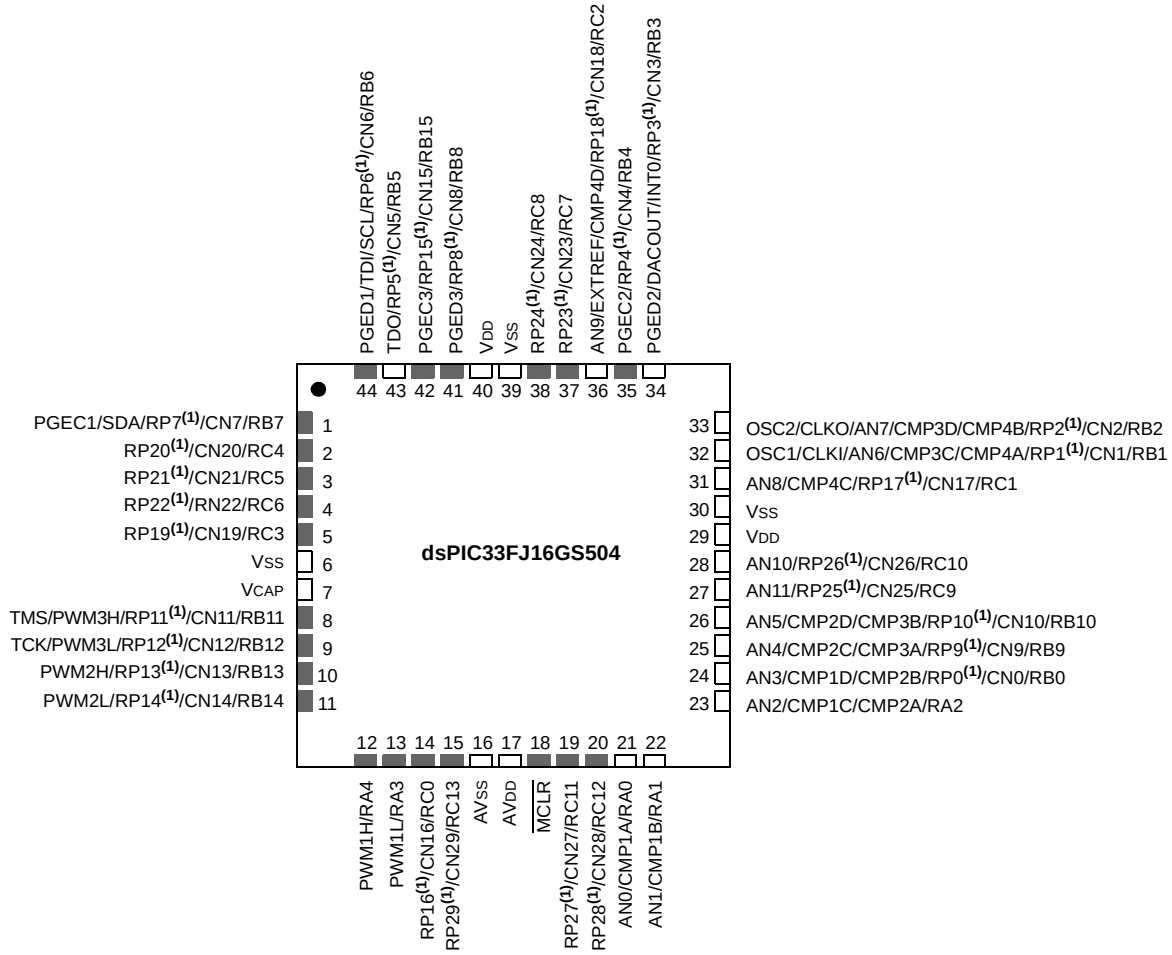
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gs404t-i-ml

Pin Diagrams (Continued)

44-Pin QFN(2)

■ = Pins are up to 5V tolerant



Note 1: The RPn pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.

2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

3.6.1 MULTIPLIER

The 17-bit x 17-bit multiplier is capable of signed or unsigned operation and can multiplex its output using a scaler to support either 1.31 fractional (Q31) or 32-bit integer results. Unsigned operands are zero-extended into the 17th bit of the multiplier input value. Signed operands are sign-extended into the 17th bit of the multiplier input value. The output of the 17-bit x 17-bit multiplier/scaler is a 33-bit value that is sign-extended to 40 bits. Integer data is inherently represented as a signed 2's complement value, where the Most Significant bit (MSb) is defined as a sign bit. The range of an N-bit 2's complement integer is -2^{N-1} to $2^{N-1} – 1$.

- For a 16-bit integer, the data range is -32768 (0x8000) to 32767 (0x7FFF), including 0.
- For a 32-bit integer, the data range is -2,147,483,648 (0x8000 0000) to 2,147,483,647 (0x7FFF FFFF).

When the multiplier is configured for fractional multiplication, the data is represented as a 2's complement fraction, where the MSb is defined as a sign bit and the radix point is implied to lie just after the sign bit (QX format). The range of an N-bit 2's complement fraction with this implied radix point is -1.0 to $(1 – 2^{1-N})$. For a 16-bit fraction, the Q15 data range is -1.0 (0x8000) to 0.999969482 (0x7FFF) including 0 and has a precision of 3.01518×10^{-5}. In Fractional mode, the 16 x 16 multiply operation generates a 1.31 product that has a precision of 4.65661×10^{-10}.

The same multiplier is used to support the MCU multiply instructions, which include integer 16-bit signed, unsigned and mixed sign multiply operations.

The MUL instruction can be directed to use byte or word-sized operands. Byte operands will direct a 16-bit result, and word operands will direct a 32-bit result to the specified register(s) in the W array.

3.6.2 DATA ACCUMULATORS AND ADDER/SUBTRACTER

The data accumulator consists of a 40-bit adder/ subtracter with automatic sign extension logic. It can select one of two accumulators (A or B) as its pre-accumulation source and post-accumulation destination. For the ADD and LAC instructions, the data to be accumulated or loaded can be optionally scaled using the barrel shifter prior to accumulation.

3.6.2.1 Adder/Subtracter, Overflow and Saturation

The adder/subtracter is a 40-bit adder with an optional zero input into one side, and either true or complement data into the other input.

- In the case of addition, the Carry/$\overline{\text{Borrow}}$ input is active-high and the other input is true data (not complemented).
- In the case of subtraction, the Carry/$\overline{\text{Borrow}}$ input is active-low and the other input is complemented.

The adder/subtracter generates Overflow Status bits, SA/SB and OA/OB, which are latched and reflected in the STATUS Register:

- Overflow from bit 39: this is a catastrophic overflow in which the sign of the accumulator is destroyed.
- Overflow into guard bits, 32 through 39: this is a recoverable overflow. This bit is set whenever all the guard bits are not identical to each other.

The adder has an additional saturation block that controls accumulator data saturation, if selected. It uses the result of the adder, the Overflow Status bits described previously and the SAT<A:B> (CORCON<7:6>) and ACCSAT (CORCON<4>) mode control bits to determine when and to what value to saturate.

Six STATUS Register bits support saturation and overflow:

- OA: ACCA overflowed into guard bits
- OB: ACCB overflowed into guard bits
- SA: ACCA saturated (bit 31 overflow and saturation)
  or
  ACCA overflowed into guard bits and saturated (bit 39 overflow and saturation)
- SB: ACCB saturated (bit 31 overflow and saturation)
  or
  ACCB overflowed into guard bits and saturated (bit 39 overflow and saturation)
- OAB: Logical OR of OA and OB
- SAB: Logical OR of SA and SB

The OA and OB bits are modified each time data passes through the adder/subtracter. When set, they indicate that the most recent operation has overflowed into the accumulator guard bits (bits 32 through 39). The OA and OB bits can also optionally generate an arithmetic warning trap when set and the corresponding Overflow Trap Flag Enable bits (OVATE, OVBTE) in the INTCON1 register are set (refer to **Section 7.0 "Interrupt Controller"**). This allows the user application to take immediate action, for example, to correct system gain.

TABLE 4-20: HIGH-SPEED PWM GENERATOR 3 REGISTER MAP FOR dsPIC33FJ16GSX02/X04 DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON3	0460	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	—	—	—	CAM	XPRES	IUE	0000
IOCON3	0462	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	0000
FCLCON3	0464	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	0000
PDC3	0466	PDC3<15:0>																0000
PHASE3	0468	PHASE3<15:0>																0000
DTR3	046C	—	—	DTR3<13:0>														0000
ALTDTR3	046C	—	—	ALTDTR3<13:0>														0000
SDC3	046E	SDC3<15:0>																0000
SPHASE3	0470	SPHASE3<15:0>																0000
TRIG3	0472	TRGCMP<15:3>													—	—	—	0000
TRGCON3	0474	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	DTM	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
STRIG3	0476	STRGCMP<15:3>													—	—	—	0000
PWMCAP3	0478	PWMCAP3<15:3>													—	—	—	0000
LEBCON3	047A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	LEB6	LEB5	LEB4	LEB3	LEB2	LEB1	LEB0	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-21: HIGH-SPEED PWM GENERATOR 4 REGISTER MAP FOR dsPIC33FJ06GS101 AND dsPIC33FJ16GS50X DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON4	0480	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	—	—	—	CAM	XPRES	IUE	0000
IOCON4	0482	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	0000
FCLCON4	0484	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	0000
PDC4	0486	PDC4<15:0>																0000
PHASE4	0488	PHASE4<15:0>																0000
DTR4	048A	—	—	DTR4<13:0>														0000
ALTDTR4	048A	—	—	ALTDTR4<13:0>														0000
SDC4	048E	SDC4<15:0>																0000
SPHASE4	0490	SPHASE4<15:0>																0000
TRIG4	0492	TRGCMP<15:3>													—	—	—	0000
TRGCON4	0494	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	DTM	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
STRIG4	0496	STRGCMP<15:3>													—	—	—	0000
PWMCAP4	0498	PWMCAP4<15:3>													—	—	—	0000
LEBCON4	049A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	LEB6	LEB5	LEB4	LEB3	LEB2	LEB1	LEB0	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.2.6 SOFTWARE STACK

In addition to its use as a Working register, the W15 register in the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices is also used as a software Stack Pointer. The Stack Pointer always points to the first available free word and grows from lower to higher addresses. It predecrements for stack pops and post-increments for stack pushes, as shown in Figure 4-6. For a PC push during any CALL instruction, the MSb of the PC is zero-extended before the push, ensuring that the MSb is always clear.

Note:	A PC push during exception processing concatenates the SRL register to the MSb of the PC prior to the push.

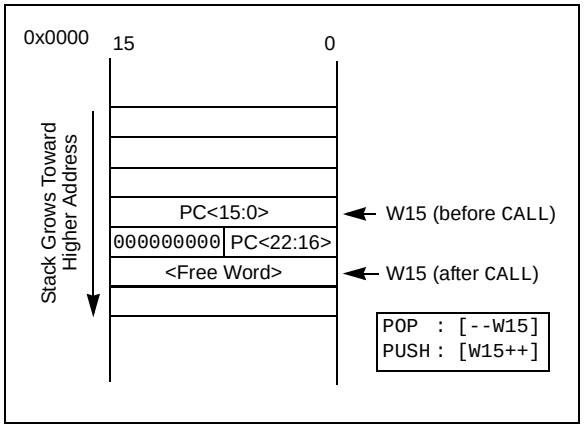
The Stack Pointer Limit register (SPLIM) associated with the Stack Pointer sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' because all stack operations must be word-aligned.

Whenever an EA is generated using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal and a push operation is performed, a stack error trap will not occur. The stack error trap will occur on a subsequent push operation. For example, to cause a stack error trap when the stack grows beyond address 0x1000 in RAM, initialize the SPLIM with the value 0x0FFE.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0x0800. This prevents the stack from interfering with the Special Function Register (SFR) space.

A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

FIGURE 4-6: CALL STACK FRAME



4.3 Instruction Addressing Modes

The addressing modes shown in Table 4-48 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.3.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a Working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire data space.

4.3.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

```
Operand 3 = Operand 1 <function> Operand 2
```

where, Operand 1 is always a Working register (that is, the addressing mode can only be register direct), which is referred to as Wb. Operand 2 can be a W register, fetched from data memory, or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-bit or 10-bit Literal

Note:	Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

5.0 FLASH PROGRAM MEMORY

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Flash Programming"** (DS70191) in the "*dsPIC33F/PIC24H Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Run-Time Self-Programming (RTSP)

ICSP allows a dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx, and three other lines for power (VDD), ground (VSS) and Master Clear ($\overline{MCLR}$). This allows customers to manufacture boards with unprogrammed devices and then program the Digital Signal Controller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data, either in blocks or 'rows' of 64 instructions (192 bytes) at a time, or a single program memory word, and erase program memory in blocks or 'pages' of 512 instructions (1536 bytes) at a time.

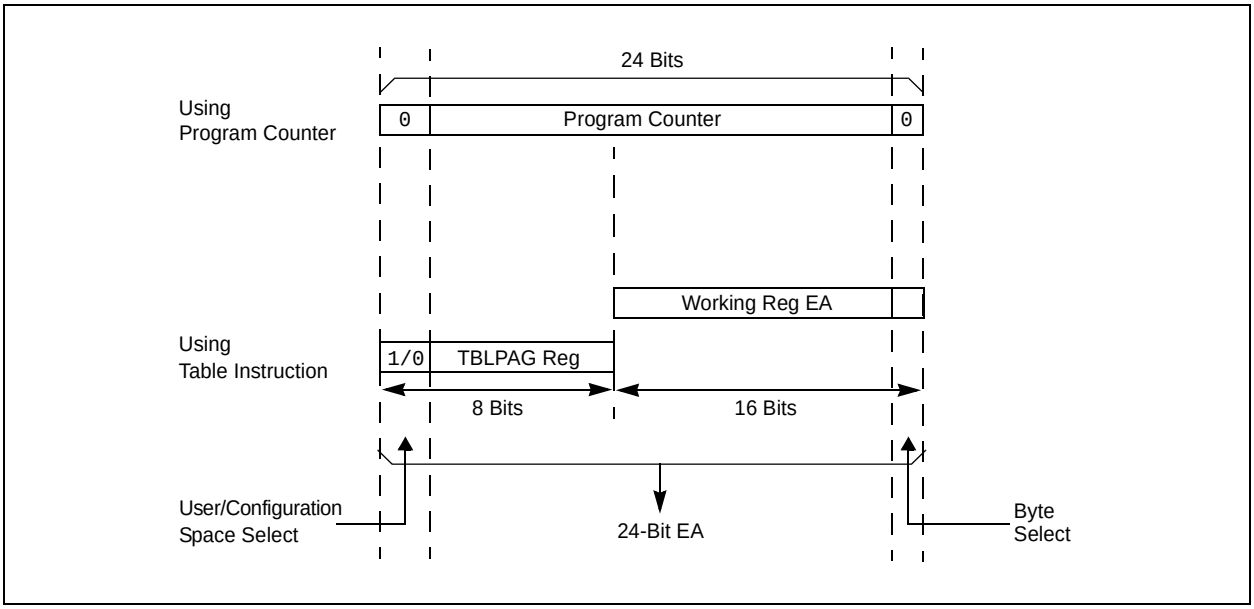
5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



REGISTER 10-9: RPINR29: PERIPHERAL PIN SELECT INPUT REGISTER 29

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	FLT1R5	FLT1R4	FLT1R3	FLT1R2	FLT1R1	FLT1R0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **FLT1R<5:0>:** Assign PWM Fault Input 1 (FLT1) to the Corresponding RPn Pin bits

111111 = Input tied to Vss
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

bit 7-0 **Unimplemented:** Read as ‘0’

12.0 TIMER2/3 FEATURES

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (DS70205) in the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available on the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

Timer2 is a Type B timer that offers the following major features:

- A Type B timer can be concatenated with a Type C timer to form a 32-bit timer
- External clock input (TxCK) is always synchronized to the internal device clock and the clock synchronization is performed after the prescaler.

Figure 12-1 shows a block diagram of the Type B timer.

Timer3 is a Type C timer that offers the following major features:

- A Type C timer can be concatenated with a Type B timer to form a 32-bit timer
- The external clock input (TxCK) is always synchronized to the internal device clock and the clock synchronization is performed before the prescaler

A block diagram of the Type C timer is shown in Figure 12-2.

Note: Timer3 is not available on all devices.

FIGURE 12-1: TYPE B TIMER BLOCK DIAGRAM (x = 2)

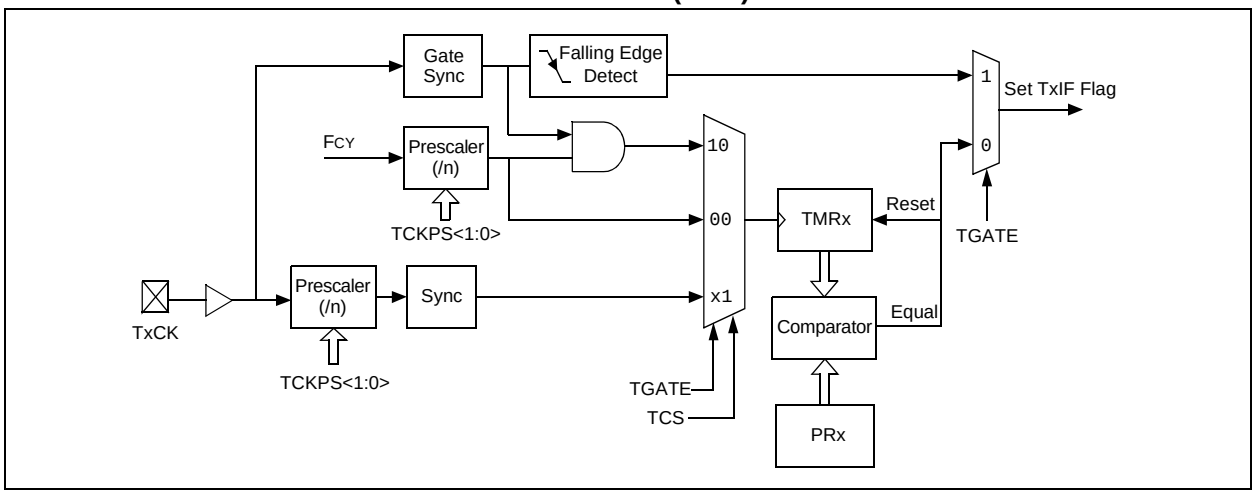
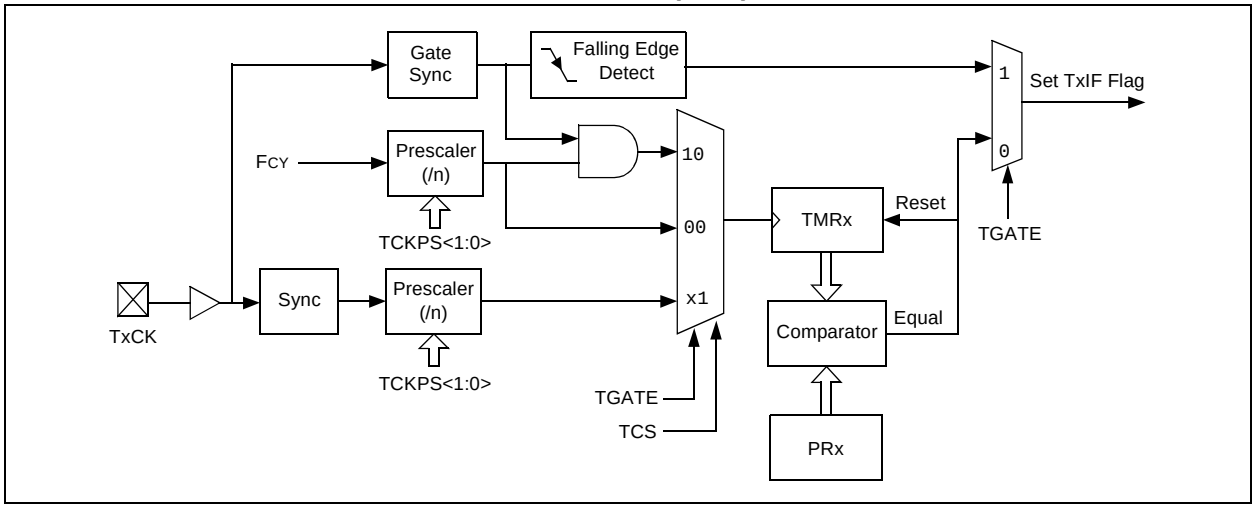


FIGURE 12-2: TYPE C TIMER BLOCK DIAGRAM (x = 3)



REGISTER 15-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER (CONTINUED)

bit 7-3 **FLTSRC<4:0>:** Fault Control Signal Source Select for PWM Generator # bits(2,3)
11111 = Reserved
•
•
•
01000 = Reserved
00111 = Fault 8
00110 = Fault 7
00101 = Fault 6
00100 = Fault 5
00011 = Fault 4
00010 = Fault 3
00001 = Fault 2
00000 = Fault 1

bit 2 **FLTPOL:** Fault Polarity for PWM Generator # bit(1)
1 = The selected Fault source is active-low
0 = The selected Fault source is active-high

bit 1-0 **FLTMOD<1:0>:** Fault Mode for PWM Generator # bits
11 = Fault input is disabled
10 = Reserved
01 = The selected Fault source forces the PWMxH and PWMxL pins to FLTDAT values (cycle)
00 = The selected Fault source forces the PWMxH and PWMxL pins to FLTDAT values (latched condition)

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

2: When Independent Fault mode is enabled (IFLTMOD = 1), and Fault 1 is used for Current-Limit mode (CLSRC<4:0> = b0000), the Fault Control Source Select bits (FLTSRC<4:0>) should be set to an unused Fault source to prevent Fault 1 from disabling both the PWMxL and PWMxH outputs.

3: When Independent Fault mode is enabled (IFLTMOD = 1) and Fault 1 is used for Fault mode (FLTSRC<4:0> = b0000), the Current-Limit Control Source Select bits (CLSRC<4:0>) should be set to an unused current-limit source to prevent the current-limit source from disabling both the PWMxH and PWMxL outputs.

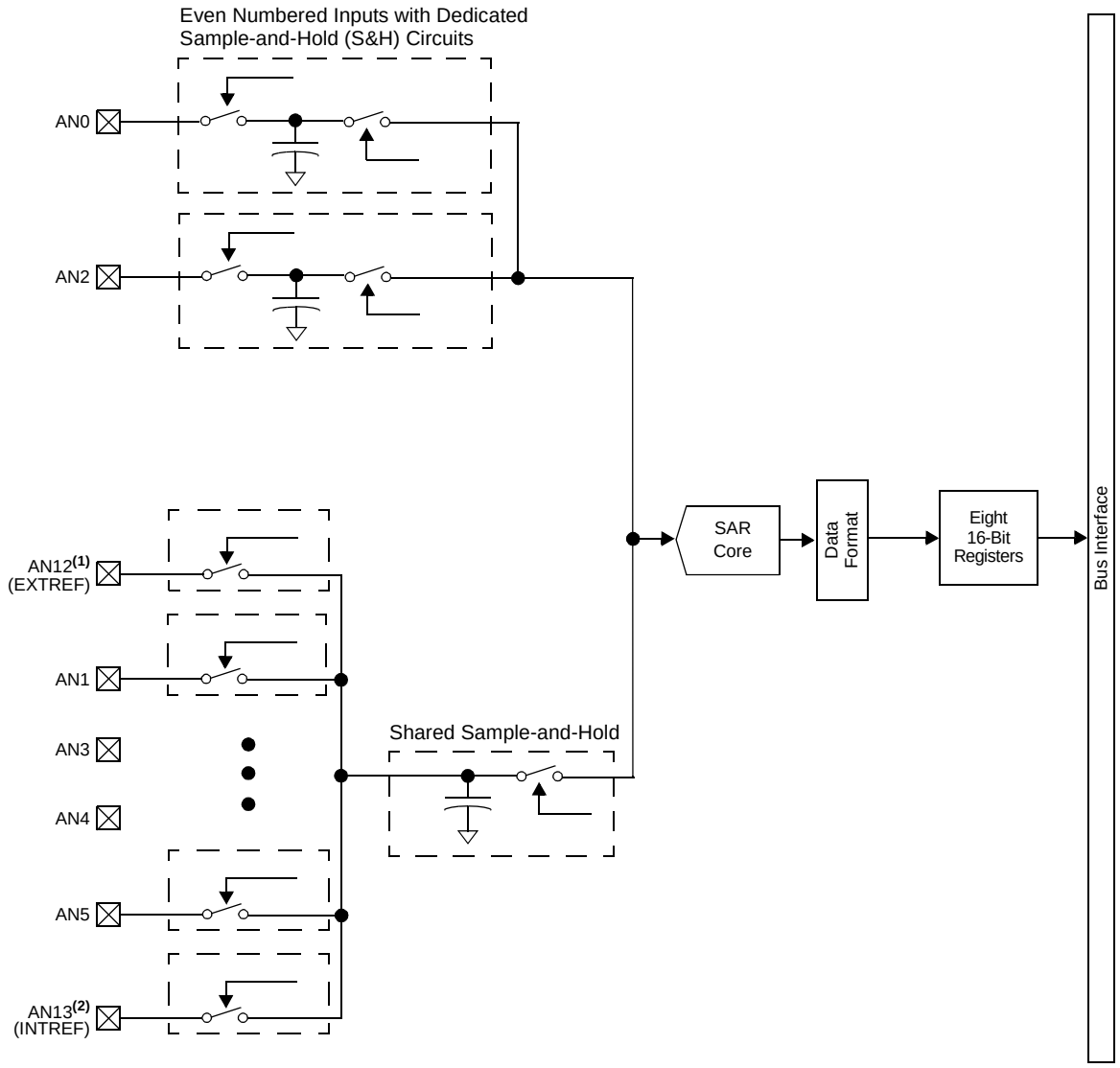
17.2 I²C Registers

I2CxCON and I2CxSTAT are control and status registers. The I2CxCON register is readable and writable. The lower six bits of I2CxSTAT are read-only. The remaining bits of the I2CxSTAT are read/write:

- I2CxRSR is the shift register used for shifting data internal to the module and the user application has no access to it
- I2CxRCV is the receive buffer and the register to which data bytes are written, or from which data bytes are read
- I2CxTRN is the transmit register to which bytes are written during a transmit operation
- The I2CxADD register holds the slave address
- A status bit, ADD10, indicates 10-Bit Addressing mode
- The I2CxBRG acts as the Baud Rate Generator (BRG) reload value

In receive operations, I2CxRSR and I2CxRCV together form a double-buffered receiver. When I2CxRSR receives a complete byte, it is transferred to I2CxRCV, and an interrupt pulse is generated.

FIGURE 19-3: ADC BLOCK DIAGRAM FOR dsPIC33FJ06GS202 DEVICES WITH ONE SAR



Note 1: AN12 (EXTREF) is an internal analog input. To measure the voltage at AN12 (EXTREF), an analog comparator must be enabled and EXTREF must be selected as the comparator reference.

2: AN13 (INTREF) is an internal analog input and is not available on a pin.

REGISTER 19-3: ADBASE: ANALOG-TO-DIGITAL BASE REGISTER(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADBASE<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
ADBASE<7:1>							—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-1 **ADBASE<15:1>:** Analog-to-Digital Base bits

This register contains the base address of the user's ADC Interrupt Service Routine jump table. This register, when read, contains the sum of the ADBASE register contents and the encoded value of the PxRDY status bits.

The encoder logic provides the bit number of the highest priority PxRDY bits, where P0RDY is the highest priority and P6RDY is the lowest priority.

bit 0 **Unimplemented:** Read as '0'

Note 1: The encoding results are shifted left two bits, so bits 1-0 of the result are always zero.

2: As an alternative to using the ADBASE register, the ADCP0-6 ADC Pair Conversion Complete interrupts can be used to invoke A to D conversion completion routines for individual ADC input pairs.

REGISTER 19-4: ADPCFG: ANALOG-TO-DIGITAL PORT CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	PCFG<11:8>(1)			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG<7:0>(1)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-0 **PCFG<11:0>:** Analog-to-Digital Port Configuration Control bits(1)

1 = Port pin in Digital mode; port read input is enabled, Analog-to-Digital input multiplexer is connected to AVSS

0 = Port pin in Analog mode; port read input is disabled, Analog-to-Digital samples the pin voltage

Note 1: Not all PCFGx bits are available on all devices. See Figure 19-1 through Figure 19-6 for the available analog pins (PCFGx = ANx, where x = 0-11).

REGISTER 19-7: ADCPC2: ANALOG-TO-DIGITAL CONVERT PAIR CONTROL REGISTER 2(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN5	PEND5	SWTRG5	TRGSRC54	TRGSRC53	TRGSRC52	TRGSRC51	TRGSRC50
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN4	PEND4	SWTRG4	TRGSRC44	TRGSRC43	TRGSRC42	TRGSRC41	TRGSRC40
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **IRQEN5:** Interrupt Request Enable 5 bit
1 = Enables IRQ generation when requested conversion of Channels AN11 and AN10 is completed
0 = IRQ is not generated

bit 14 **PEND5:** Pending Conversion Status 5 bit
1 = Conversion of Channels AN11 and AN10 is pending; set when selected trigger is asserted
0 = Conversion is complete

bit 13 **SWTRG5:** Software Trigger 5 bit
1 = Starts conversion of AN11 and AN10 (if selected by the TRGSRCx bits)(2)
This bit is automatically cleared by hardware when the PEND5 bit is set.
0 = Conversion has not started

Note 1: This register is only implemented in the dsPIC33FJ16GS504 devices.

2: The trigger source must be set as a global software trigger prior to setting this bit to '1'. If other conversions are in progress, then the conversion will be performed when the conversion resources are available.

21.5 JTAG Interface

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices implement a JTAG interface, which supports boundary scan device testing. Detailed information on this interface will be provided in future revisions of the document.

21.6 In-Circuit Serial Programming

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 family of Digital Signal Controllers can be serially programmed while in the end application circuit. This is done with two lines for clock and data and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the Digital Signal Controller just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for details about In-Circuit Serial Programming (ICSP).

Any of the three pairs of programming clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

21.7 In-Circuit Debugger

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices provide simple debugging functionality through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pin functions.

Any of the three pairs of debugging clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{MCLR}$, V_{DD}, V_{SS}, and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

TABLE 24-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
Operating Current (IDD)(2)						
DC27d	111	140	mA	-40°C	3.3V	40 MIPS See **Note 2**, except PWM is operating at 1/4 speed (PTCON2 = 0x0002)
DC27a	108	130	mA	+25°C		
DC27b	105	130	mA	+85°C		
DC27c	103	130	mA	+125°C		
DC28d	102	130	mA	-40°C	3.3V	40 MIPS See **Note 2**, except PWM is operating at 1/8 speed (PTCON2 = 0x0003)
DC28a	100	120	mA	+25°C		
DC28b	100	120	mA	+85°C		
DC28c	100	120	mA	+125°C		

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- CPU executing `while(1)` statement
- JTAG disabled

3: These parameters are characterized but not tested in manufacturing.

TABLE 24-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Conditions**		
Power-Down Current (I_{PD})(2,4)						
DC60d	125	500	µA	-40°C	3.3V	Base Power-Down Current
DC60a	135	500	µA	+25°C		
DC60b	235	500	µA	+85°C		
DC60c	565	950	µA	+125°C		
DC61d	40	50	µA	-40°C	3.3V	Watchdog Timer Current: ΔI_{WDT}(3)
DC61a	40	50	µA	+25°C		
DC61b	40	50	µA	+85°C		
DC61c	80	90	µA	+125°C		

Note 1: Data in the Typical column is at 3.3V, +25°C unless otherwise stated.

2: I_{PD} (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{MCLR}$ = V_{DD}, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all ones)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to stand-by while the device is in Sleep mode)
- JTAG disabled

3: The Δ current is the additional current consumed when the WDT module is enabled. This current should be added to the base I_{PD} current.

4: These currents are measured on the device containing the most memory in this family.

TABLE 24-12: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	10,000	—	—	E/W	-40°C to +125°C
D131	VPR	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D132B	VPEW	VDD for Self-Timed Write	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to +125°C
D135	IDDP	Supply Current during Programming	—	10	—	mA	
D136a	TRW	Row Write Time	1.477	—	1.538	ms	TRW = 11064 FRC cycles, TA = +85°C, See **Note 2**
D136b	TRW	Row Write Time	1.435	—	1.586	ms	TRW = 11064 FRC cycles, TA = +125°C, See **Note 2**
D137a	TPE	Page Erase Time	22.5	—	23.4	ms	TPE = 168517 FRC cycles, TA = +85°C, See **Note 2**
D137b	TPE	Page Erase Time	21.9	—	24.2	ms	TPE = 168517 FRC cycles, TA = +125°C, See **Note 2**
D138a	TWW	Word Write Cycle Time	47.4	—	49.3	µs	TWW = 355 FRC cycles, TA = +85°C, See **Note 2**
D138b	TWW	Word Write Cycle Time	46	—	50.9	µs	TWW = 355 FRC cycles, TA = +125°C, See **Note 2**

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

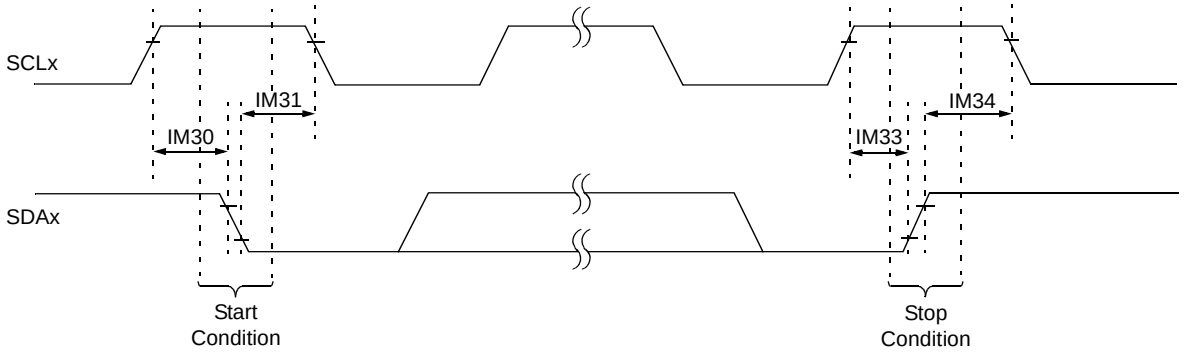
2: Other conditions: FRC = 7.37 MHz, TUN<5:0> = b'011111 (for Min), TUN<5:0> = b'100000 (for Max). This parameter depends on the FRC accuracy (see Table 24-20) and the value of the FRC Oscillator Tuning register (see Register 9-4). For complete details on calculating the Minimum and Maximum time see **Section 5.3 "Programming Operations"**.

TABLE 24-13: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions:	-40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended						
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
—	CEFC	External Filter Capacitor Value(1)	4.7	10	—	µF	Capacitor must be low series resistance (< 5 ohms)

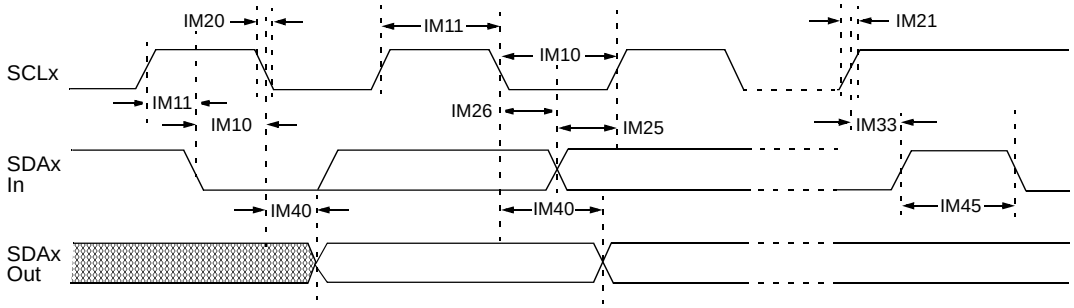
Note 1: Typical VCAP voltage = 2.5 volts when VDD ≥ VDDMIN.

FIGURE 24-19: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 24-1 for load conditions.

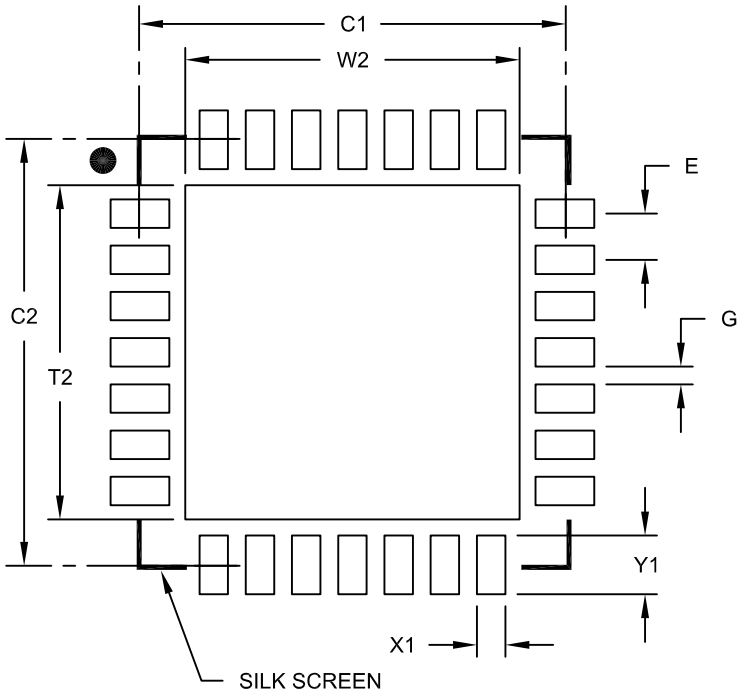
FIGURE 24-20: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 24-1 for load conditions.

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (X28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A

APPENDIX A: REVISION HISTORY

Revision A (January 2008)

This is the initial revision of this document.

Revision B (June 2008)

This revision includes minor typographical and formatting changes throughout the data sheet text. In addition, redundant information was removed that is now available in the respective chapters of the *dsPIC33F/PIC24H Family Reference Manual*, which can be obtained from the Microchip web site (www.microchip.com).

The major changes are referenced by their respective section in the following table.

TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-bit Digital Signal Controllers"	Moved location of Note 1 (RPn pin) references (see **"Pin Diagrams"**).
Section 3.0 "Memory Organization"	Updated CPU Core Register map SFR reset value for CORCON (see Table 3-1). Removed Interrupt Controller Register Map SFR IPC29 and updated reset values for IPC0, IPC1, IPC14, IPC16, IPC23, IPC24, IPC27, and IPC28 (see Table 3-5). Removed Interrupt Controller Register Map SFR IPC24 and IPC29 and updated reset values for IPC0, IPC1, IPC2, IPC14, IPC16, IPC23, IPC27, and IPC28 (see Table 3-6). Removed Interrupt Controller Register Map SFR IPC24 and updated reset values for IPC1, IPC2, IPC4, IPC14, IPC16, IPC23, IPC24, IPC27, and IPC28 (see Table 3-7). Updated Interrupt Controller Register Map SFR reset values for IPC1, IPC14, IPC16, IPC23, IPC24, IPC27, and IPC28 (see Table 3-8). Updated Interrupt Controller Register Map SFR reset values for IPC1, IPC14, IPC16, IPC23, IPC24, IPC25, IPC26, IPC27, IPC28, and IPC29 (see Table 3-9). Updated Interrupt Controller Register Map SFR reset values for IPC1, IPC4, IPC14, IPC16, IPC23, IPC24, IPC25, IPC26, IPC27, IPC28, and IPC29 (see Table 3-10). Added SFR definitions for RPOR16 and RPOR17 (see Table 3-34, Table 3-35, and Table 3-36). Updated bit definitions for PORTA, PORTB, and PORTC SFRs (ODCA, ODCB, and ODCC) (see Table 3-37, Table 3-38, Table 3-39, and Table 3-40). Updated bit definitions and reset value for System Control Register map SFR CLKDIV (see Table 3-41). Added device-specific information to title of PMD Register Map (see Table 3-47). Added device-specific PMD Register Maps (see Table 3-46, Table 3-45, and Table 3-43).

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