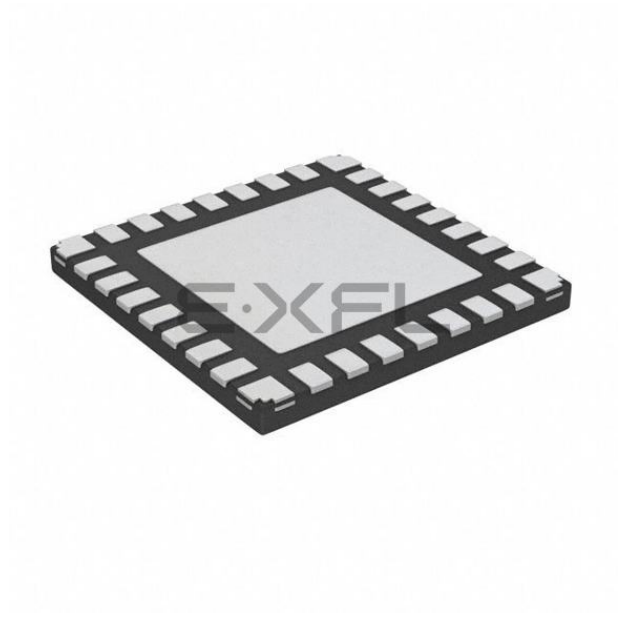

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

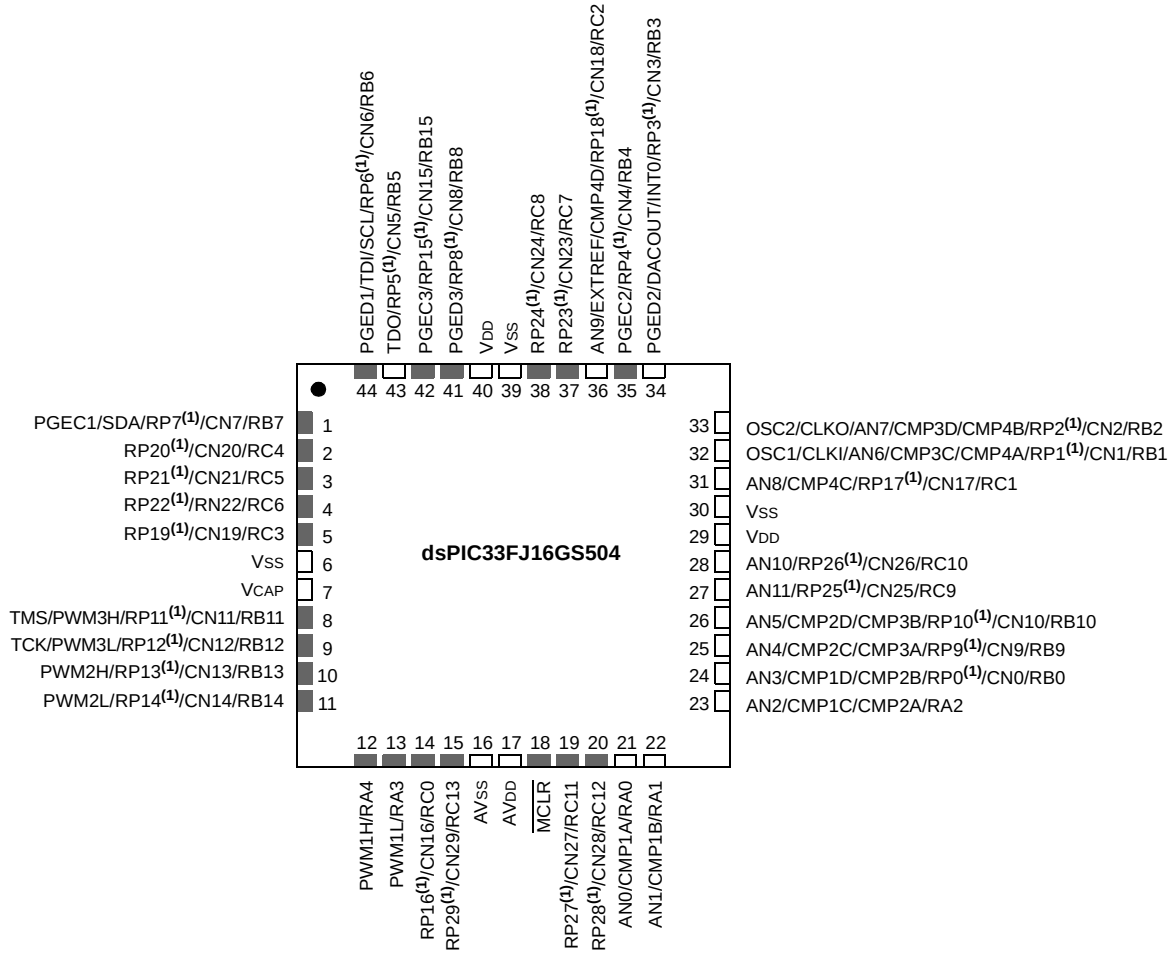
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UQFN Exposed Pad
Supplier Device Package	28-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gs502-e-mx

Pin Diagrams (Continued)

44-Pin QFN(2)

■ = Pins are up to 5V tolerant



Note 1: The RPn pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.

2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

TABLE 4-20: HIGH-SPEED PWM GENERATOR 3 REGISTER MAP FOR dsPIC33FJ16GSX02/X04 DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON3	0460	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	—	—	—	CAM	XPRES	IUE	0000
IOCON3	0462	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	0000
FCLCON3	0464	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	0000
PDC3	0466	PDC3<15:0>																0000
PHASE3	0468	PHASE3<15:0>																0000
DTR3	046C	—	—	DTR3<13:0>														0000
ALTDTR3	046C	—	—	ALTDTR3<13:0>														0000
SDC3	046E	SDC3<15:0>																0000
SPHASE3	0470	SPHASE3<15:0>																0000
TRIG3	0472	TRGCMP<15:3>													—	—	—	0000
TRGCON3	0474	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	DTM	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
STRIG3	0476	STRGCMP<15:3>													—	—	—	0000
PWMCAP3	0478	PWMCAP3<15:3>													—	—	—	0000
LEBCON3	047A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	LEB6	LEB5	LEB4	LEB3	LEB2	LEB1	LEB0	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-21: HIGH-SPEED PWM GENERATOR 4 REGISTER MAP FOR dsPIC33FJ06GS101 AND dsPIC33FJ16GS50X DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON4	0480	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	—	—	—	CAM	XPRES	IUE	0000
IOCON4	0482	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	0000
FCLCON4	0484	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	0000
PDC4	0486	PDC4<15:0>																0000
PHASE4	0488	PHASE4<15:0>																0000
DTR4	048A	—	—	DTR4<13:0>														0000
ALTDTR4	048A	—	—	ALTDTR4<13:0>														0000
SDC4	048E	SDC4<15:0>																0000
SPHASE4	0490	SPHASE4<15:0>																0000
TRIG4	0492	TRGCMP<15:3>													—	—	—	0000
TRGCON4	0494	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	DTM	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
STRIG4	0496	STRGCMP<15:3>													—	—	—	0000
PWMCAP4	0498	PWMCAP4<15:3>													—	—	—	0000
LEBCON4	049A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	LEB6	LEB5	LEB4	LEB3	LEB2	LEB1	LEB0	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-29: HIGH-SPEED 10-BIT ADC REGISTER MAP FOR dsPIC33FJ16GS502 DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADCON	0300	ADON	—	ADSIDL	SLOWCLK	—	GSWTRG	—	FORM	EIE	ORDER	SEQSAMP	ASYNCSAMP	—	ADCS2	ADCS1	ADCS0	0003
ADPCFG	0302	—	—	—	—	—	—	—	—	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
ADSTAT	0306	—	—	—	—	—	—	—	—	—	P6RDY	—	—	P3RDY	P2RDY	P1RDY	P0RDY	0000
ADBASE	0308	ADBASE<15:1>															—	0000
ADCPC0	030A	IRQEN1	PEND1	SWTRG1	TRGSRC14	TRGSRC13	TRGSRC12	TRGSRC11	TRGSRC10	IRQEN0	PEND0	SWTRG0	TRGSRC04	TRGSRC03	TRGSRC02	TRGSRC01	TRGSRC00	0000
ADCPC1	030C	IRQEN3	PEND3	SWTRG3	TRGSRC34	TRGSRC33	TRGSRC32	TRGSRC31	TRGSRC30	IRQEN2	PEND2	SWTRG2	TRGSRC24	TRGSRC23	TRGSRC22	TRGSRC21	TRGSRC20	0000
ADCPC3	0310	—	—	—	—	—	—	—	—	IRQEN6	PEND6	SWTRG6	TRGSRC64	TRGSRC63	TRGSRC62	TRGSRC61	TRGSRC60	0000
ADCBUF0	0320	ADC Data Buffer 0																xxxx
ADCBUF1	0322	ADC Data Buffer 1																xxxx
ADCBUF2	0324	ADC Data Buffer 2																xxxx
ADCBUF3	0326	ADC Data Buffer 3																xxxx
ADCBUF4	0328	ADC Data Buffer 4																xxxx
ADCBUF5	032A	ADC Data Buffer 5																xxxx
ADCBUF6	032C	ADC Data Buffer 6																xxxx
ADCBUF7	032E	ADC Data Buffer 7																xxxx
ADCBUF12	0338	ADC Data Buffer 12																xxxx
ADCBUF13	033A	ADC Data Buffer 13																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

6.2 Power-on Reset (POR)

A Power-on Reset (POR) circuit ensures the device is reset from power-on. The POR circuit is active until VDD crosses the VPOR threshold and the delay, TPOR, has elapsed. The delay, TPOR, ensures the internal device bias circuits become stable.

The device supply voltage characteristics must meet the specified starting voltage and rise rate requirements to generate the POR. Refer to **Section 24.0 "Electrical Characteristics"** for details.

The POR status (POR) bit in the Reset Control (RCON<0>) register is set to indicate the Power-on Reset.

6.2.1 Brown-out Reset (BOR) and Power-up Timer (PWRT)

The on-chip regulator has a Brown-out Reset (BOR) circuit that resets the device when the VDD is too low (VDD < VBOR) for proper device operation. The BOR circuit keeps the device in Reset until VDD crosses the VBOR threshold and the delay, TBOR, has elapsed. The delay, TBOR, ensures the voltage regulator output becomes stable.

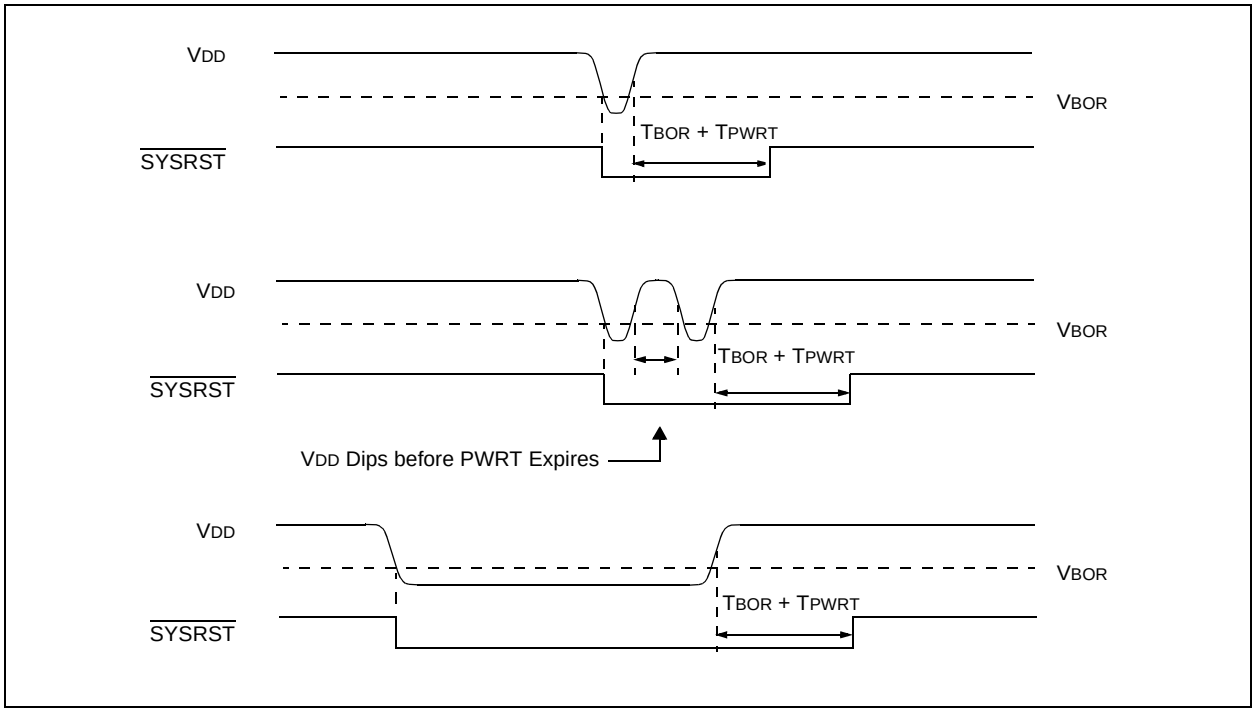
The BOR status (BOR) bit in the Reset Control (RCON<1>) register is set to indicate the Brown-out Reset.

The device will not run at full speed after a BOR as the VDD should rise to acceptable levels for full-speed operation. The PWRT provides power-up time delay (TPWRT) to ensure that the system power supplies have stabilized at the appropriate levels for full-speed operation before the $\overline{\text{SYSRST}}$ is released.

The Power-up Timer Delay (TPWRT) is programmed by the Power-on Reset Timer Value Select (FPWRT<2:0>) bits in the FPOR Configuration (FPOR<2:0>) register, which provides eight settings (from 0 ms to 128 ms). Refer to **Section 21.0 "Special Features"** for further details.

Figure 6-3 shows the typical brown-out scenarios. The Reset delay (TBOR + TPWRT) is initiated each time VDD rises above the VBOR trip point.

FIGURE 6-3: BROWN-OUT SITUATIONS



REGISTER 7-16: IEC5: INTERRUPT ENABLE CONTROL REGISTER 5

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
PWM2IE	PWM1IE	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PWM2IE:** PWM2 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 14 **PWM1IE:** PWM1 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13-0 **Unimplemented:** Read as '0'

9.2.2 IDLE MODE

The following occur in Idle mode:

- The CPU stops executing instructions
- The WDT is automatically cleared
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 9.4 "Peripheral Module Disable"**).
- If the WDT or FSCM is enabled, the LPRC also remains active

The device will wake-up from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction, or the first instruction in the ISR.

9.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

9.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this may not be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the CAN module has been configured for 500 kbps based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the CAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

9.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers will have no effect and read values will be invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC® DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note:	If a PMD bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation).

10.2 Open-Drain Configuration

In addition to the PORTx, LATx and TRISx registers for data control, some digital-only port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (for example, 5V) on any desired 5V tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

Refer to **"Pin Diagrams"** for the available pins and their functionality.

10.3 Configuring Analog Port Pins

The ADPCFG and TRISx registers control the operation of the Analog-to-Digital (A/D) port pins. The port pins that are to function as analog inputs must have their corresponding TRISx bit set (input). If the TRISx bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The ADPCFG register has a default value of 0x0000; therefore, all pins that share ANx functions are analog (not digital) by default.

When the PORTx register is read, all pins configured as analog input channels will read as cleared (a low level).

Pins configured as digital inputs will not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

10.4 I/O Port Write/Read Timing

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a NOP. An example is shown in Example 10-1.

10.5 Input Change Notification

The Input Change Notification (ICN) function of the I/O ports allows the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Depending on the device pin count, up to 30 external signals (CNx pin) can be selected (enabled) for generating an interrupt request on a Change-of-State.

Four control registers are associated with the CN module. The CNEN1 and CNEN2 registers contain the interrupt enable control bits for each of the CN input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CN pin also has a weak pull-up connected to it. The pull-ups act as a current source connected to the pin, and eliminate the need for external resistors when the push button or keypad devices are connected. The pull-ups are enabled separately using the CNPU1 and CNPU2 registers, which contain the control bits for each of the CN pins. Setting any of the control bits enables the weak pull-ups for the corresponding pins.

Note:	Pull-ups on Change Notification pins should always be disabled when the port pin is configured as a digital output.

EQUATION 10-1: PORT WRITE/READ EXAMPLE

```
MOV   0xFF00, W0          ; Configure PORTB<15:8> as inputs
MOV   W0, TRISBB          ; and PORTB<7:0> as outputs
NOP                       ; Delay 1 cycle
BTSS  PORTB, #13          ; Next Instruction
```

10.6.2.2 Output Mapping

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 6-bit fields, with each set associated with one RPn pin (see Register 10-15 through Register 10-31). The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 10-2 and Figure 10-3).

The list of peripherals for output mapping also includes a null value of '00000' because of the mapping technique. This permits any given pin to remain unconnected from the output of any of the pin selectable peripherals.

FIGURE 10-3: MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPn

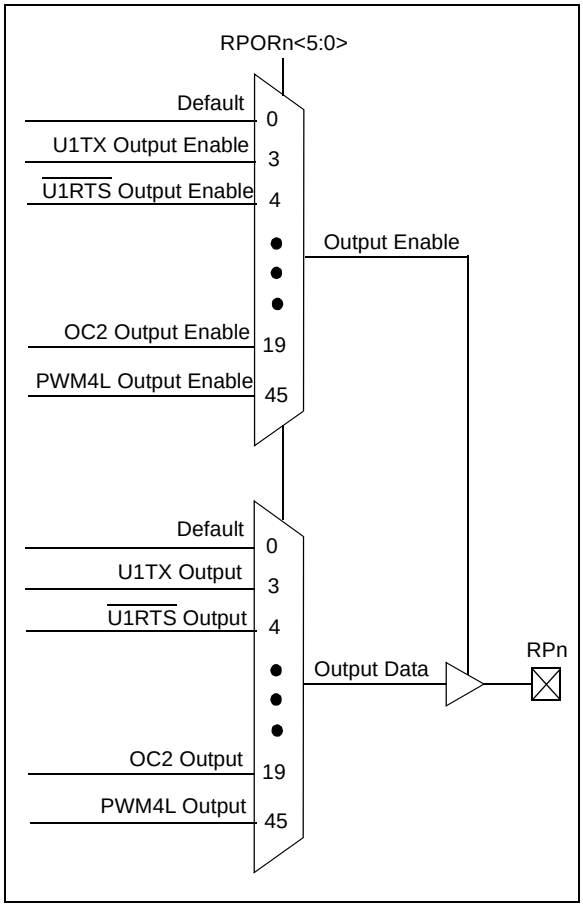


TABLE 10-2: OUTPUT SELECTION FOR REMAPPABLE PIN (RPn)

Function	RPORn<5:0>	Output Name
NULL	000000	RPn tied to default port pin
U1TX	000011	RPn tied to UART1 transmit
$\overline{\text{U1RTS}}$	000100	RPn tied to UART1 Ready-to-Send
SDO1	000111	RPn tied to SPI1 data output
SCK1	001000	RPn tied to SPI1 clock output
$\overline{\text{SS1}}$	001001	RPn tied to SPI1 slave select output
OC1	010010	RPn tied to Output Compare 1
OC2	010011	RPn tied to Output Compare 2
SYNCO1	100101	RPn tied to external device synchronization signal via PWM master time base
REFCLKO	100110	REFCLK output signal
ACMP1	100111	RPn tied to Analog Comparator Output 1
ACMP2	101000	RPn tied to Analog Comparator Output 2
ACMP3	101001	RPn tied to Analog Comparator Output 3
ACMP4	101010	RPn tied to Analog Comparator Output 4
PWM4H	101100	RPn tied to PWM output pins associated with PWM Generator 4
PWM4L	101101	RPn tied to PWM output pins associated with PWM Generator 4

REGISTER 15-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **PHASEx<15:0>:** PWM Phase-Shift Value or Independent Time Base Period for this PWM Generator bits

Note 1: If PWMCONx<ITB> = 0, the following applies based on the mode of operation:

- Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10); PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs
- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11); PHASEx<15:0> = Phase-shift value for PWMxL only

2: If PWMCONx<ITB> = 1, the following applies based on the mode of operation:

- Complementary, Redundant, and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10); PHASEx<15:0> = Independent Time Base period value for PWMxH and PWMxL
- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11); PHASEx<15:0> = Independent Time Base period value for PWMxL only
- The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0008, while the maximum pulse width generated corresponds to a value of Period – 0x0008.

REGISTER 15-18: LEBCONx: LEADING-EDGE BLANKING CONTROL REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	LEB6	LEB5
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
LEB4	LEB3	LEB2	LEB1	LEB0	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PHR:** PWMxH Rising Edge Trigger Enable bit
1 = Rising edge of PWMxH will trigger the LEB counter
0 = LEB ignores the rising edge of PWMxH

bit 14 **PHF:** PWMH Falling Edge Trigger Enable bit
1 = Falling edge of PWMxH will trigger the LEB counter
0 = LEB ignores the falling edge of PWMxH

bit 13 **PLR:** PWML Rising Edge Trigger Enable bit
1 = Rising edge of PWMxL will trigger the LEB counter
0 = LEB ignores the rising edge of PWMxL

bit 12 **PLF:** PWML Falling Edge Trigger Enable bit
1 = Falling edge of PWMxL will trigger the LEB counter
0 = LEB ignores the falling edge of PWMxL

bit 11 **FLTLEBEN:** Fault Input LEB Enable bit
1 = Leading-Edge Blanking is applied to selected Fault input
0 = Leading-Edge Blanking is not applied to selected Fault input

bit 10 **CLLEBEN:** Current-Limit LEB Enable bit
1 = Leading-Edge Blanking is applied to selected current-limit input
0 = Leading-Edge Blanking is not applied to selected current-limit input

bit 9-3 **LEB<6:0>:** Leading-Edge Blanking for Current-Limit and Fault Inputs bits
The value is 8.32 nsec increments.

bit 2-0 **Unimplemented:** Read as ‘0’

Note 1: Configure this register in word format.

REGISTER 17-1: I2CxCON: I2Cx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HC = Hardware Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **I2CEN:** I2Cx Enable bit
1 = Enables the I2Cx module, and configures the SDAx and SCLx pins as serial port pins
0 = Disables the I2Cx module; all I^2C™ pins are controlled by port functions.

bit 14 **Unimplemented:** Read as '0'

bit 13 **I2CSIDL:** I2Cx Stop in Idle Mode bit
1 = Discontinues module operation when device enters an Idle mode
0 = Continues module operation in Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I^2C slave)
1 = Releases SCLx clock
0 = Holds SCLx clock low (clock stretch)
If STREN = 1:
Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.
If STREN = 0:
Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of slave transmission.

bit 11 **IPMIEN:** Intelligent Peripheral Management Interface (IPMI) Enable bit
1 = IPMI mode is enabled; all addresses are Acknowledged
0 = IPMI mode is disabled

bit 10 **A10M:** 10-Bit Slave Address bit
1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit
1 = Slew rate control is disabled
0 = Slew rate control is enabled

bit 8 **SMEN:** SMBus Input Levels bit
1 = Enables I/O pin thresholds compliant with SMBus specification
0 = Disables SMBus input thresholds

bit 7 **GCEN:** General Call Enable bit (when operating as I^2C slave)
1 = Enables interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)
0 = General call address is disabled

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I^2C slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receive clock stretching
0 = Disables software or receive clock stretching

19.0 HIGH-SPEED 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"High-Speed 10-Bit Analog-to-Digital Converter (ADC)"** (DS70000321) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available on the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices provide high-speed, successive approximation Analog-to-Digital conversions to support applications, such as AC/DC and DC/DC power converters.

19.1 Features Overview

The ADC module comprises the following features:

- 10-bit resolution
- Unipolar inputs
- Up to two Successive Approximation Registers (SARs)
- Up to 12 external input channels
- Up to two internal analog inputs
- Dedicated result register for each analog input
- ±1 LSB accuracy at 3.3V
- Single supply operation
- 4 Msps conversion rate at 3.3V (devices with two SARs)
- 2 Msps conversion rate at 3.3V (devices with one SAR)
- Low-power CMOS technology

19.2 Module Description

This ADC module is designed for applications that require low latency between the request for conversion and the resultant output data. Typical applications include:

- AC/DC power supplies
- DC/DC Converters
- Power Factor Correction (PFC)

This ADC works with the high-speed PWM module in power control applications that require high-frequency control loops. This module can sample and convert two analog inputs in a 0.5 microsecond when two SARs are used. This small conversion delay reduces the "phase lag" between measurement and control system response.

Up to five inputs may be sampled at a time (four inputs from the dedicated Sample-and-Hold circuits and one from the shared Sample-and-Hold circuit). If multiple inputs request conversion, the ADC will convert them in a sequential manner, starting with the lowest order input.

This ADC design provides each pair of analog inputs (AN1, AN0), (AN3, AN2),..., the ability to specify its own trigger source out of a maximum of sixteen different trigger sources. This capability allows this ADC to sample and convert analog inputs that are associated with PWM generators operating on Independent Time Bases (ITBs).

The user application typically requires synchronization between analog data sampling and PWM output to the application circuit. The very high-speed operation of this ADC module allows "data on demand".

In addition, several hardware features have been added to the peripheral interface to improve real-time performance in a typical DSP-based application.

- Result alignment options
- Automated sampling
- External conversion start control
- Two internal inputs to monitor the INTREF internal reference and the EXTREF input signal

19.3 Module Functionality

The high-speed, 10-bit ADC module is designed to support power conversion applications when used with the high-speed PWM module. The ADC may have one or two SAR modules, depending on the device variant. If two SARs are present on a device, two conversions can be processed at a time, yielding 4 Msps conversion rate. If only one SAR is present on a device, only one conversion can be processed at a time, yielding 2 Msps conversion rate. The high-speed 10-bit ADC produces two 10-bit conversion results in a 0.5 microsecond.

The ADC module supports up to 12 external analog inputs and two internal analog inputs. To monitor reference voltage, two internal inputs, AN12 and AN13, are connected to the EXTREF and INTREF voltages, respectively.

The analog reference voltage is defined as the device supply voltage (AV_{DD}/AV_{SS}).

Block diagrams of the ADC module are shown in Figure 19-1 through Figure 19-6.

REGISTER 19-5: ADCPC0: ANALOG-TO-DIGITAL CONVERT PAIR CONTROL REGISTER 0 (CONTINUED)

bit 4-0 **TRGSRC0<4:0>:** Trigger 0 Source Selection bits

Selects trigger source for conversion of Analog Channels AN1 and AN0.

11111 = Timer2 period match
•
•
•
11011 = Reserved
11010 = PWM Generator 4 current-limit ADC trigger
11001 = PWM Generator 3 current-limit ADC trigger
11000 = PWM Generator 2 current-limit ADC trigger
10111 = PWM Generator 1 current-limit ADC trigger
10110 = Reserved
•
•
•
10010 = Reserved
10001 = PWM Generator 4 secondary trigger is selected
10000 = PWM Generator 3 secondary trigger is selected
01111 = PWM Generator 2 secondary trigger is selected
01110 = PWM Generator 1 secondary trigger is selected
01101 = Reserved
01100 = Timer1 period match
•
•
•
01000 = Reserved
00111 = PWM Generator 4 primary trigger is selected
00110 = PWM Generator 3 primary trigger is selected
00101 = PWM Generator 2 primary trigger is selected
00100 = PWM Generator 1 primary trigger is selected
00011 = PWM Special Event Trigger is selected
00010 = Global software trigger is selected
00001 = Individual software trigger is selected
00000 = No conversion is enabled

Note 1: The trigger source must be set as a global software trigger prior to setting this bit to '1'. If other conversions are in progress, then the conversion will be performed when the conversion resources are available.

23.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

23.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

23.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

23.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

23.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

24.1 DC Characteristics

TABLE 24-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)	Temp Range (in °C)	Max MIPS
			dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04
—	3.0-3.6V(1)	-40°C to +85°C	40
—	3.0-3.6V(1)	-40°C to +125°C	40

Note 1: Overall functional device operation at $V_{BORMIN} < V_{DD} < V_{DDMIN}$ is tested but not characterized. All device analog modules such as the ADC, etc., will function but with degraded performance below V_{DDMIN}. Refer to Parameter BO10 in Table 24-11 for BOR values.

TABLE 24-2: THERMAL OPERATING CONDITIONS

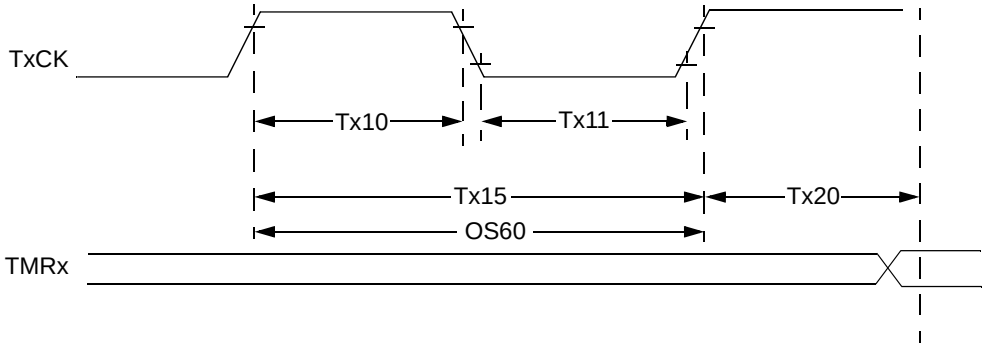
Rating	Symbol	Min	Typ	Max	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	T_J	-40	—	+125	°C
Operating Ambient Temperature Range	T_A	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	T_J	-40	—	+140	°C
Operating Ambient Temperature Range	T_A	-40	—	+125	°C
Power Dissipation: Internal chip power dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$ I/O Pin Power Dissipation: $I/O = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 24-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit	Notes
Package Thermal Resistance, 44-Pin QFN	θ_{JA}	28	—	°C/W	**1**
Package Thermal Resistance, 44-Pin TFQP	θ_{JA}	39	—	°C/W	**1**
Package Thermal Resistance, 28-Pin SPDIP	θ_{JA}	42	—	°C/W	**1**
Package Thermal Resistance, 28-Pin SOIC	θ_{JA}	47	—	°C/W	**1**
Package Thermal Resistance, 28-Pin QFN-S	θ_{JA}	34	—	°C/W	**1**
Package Thermal Resistance, 18-Pin SOIC	θ_{JA}	57	—	°C/W	**1**
Package Thermal Resistance, 44-Pin VTLA	θ_{JA}	25	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

FIGURE 24-5: TIMER1, 2 AND 3 EXTERNAL CLOCK TIMING CHARACTERISTICS



Note: Refer to Figure 24-1 for load conditions.

TABLE 24-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS(1)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TA10	TTXH	T1CK High Time	Synchronous, no prescaler	TCY + 20	—	—	ns	Must also meet Parameter TA15, N = Prescale value (1, 8, 64, 256)
			Synchronous, with prescaler	(TCY + 20)/N	—	—	ns	
			Asynchronous	20	—	—	ns	
TA11	TTXL	T1CK Low Time	Synchronous, no prescaler	TCY + 20	—	—	ns	Must also meet Parameter TA15, N = Prescale value (1, 8, 64, 256)
			Synchronous, with prescaler	(TCY + 20)/N	—	—	ns	
			Asynchronous	20	—	—	ns	
TA15	TTXP	T1CK Input Period	Synchronous, no prescaler	2 TCY + 40	—	—	ns	
			Synchronous, with prescaler	Greater of: 40 ns or (2 TCY + 40)/N	—	—	—	N = Prescale value (1, 8, 64, 256)
			Asynchronous	40	—	—	ns	
OS60	FT1	T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON<1>))		DC	—	50	kHz	
TA20	TCKEXTMRL	Delay from External T1CK Clock Edge to Timer Increment		0.75 TCY + 40	—	1.75 TCY + 40	—	

Note 1: Timer1 is a Type A timer.

TABLE 24-31: SPIx MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP10	TscP	Maximum SCKx Frequency	—	—	15	MHz	See **Note 3**
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdiV2scH, TdiV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

TABLE 24-36: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP70	TscP	Maximum SCKx Input Frequency	—	—	15	MHz	See **Note 3**
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	1.5 TCY + 40	—	—	ns	See **Note 4**

Note 1: These parameters are characterized, but are not tested in manufacturing.

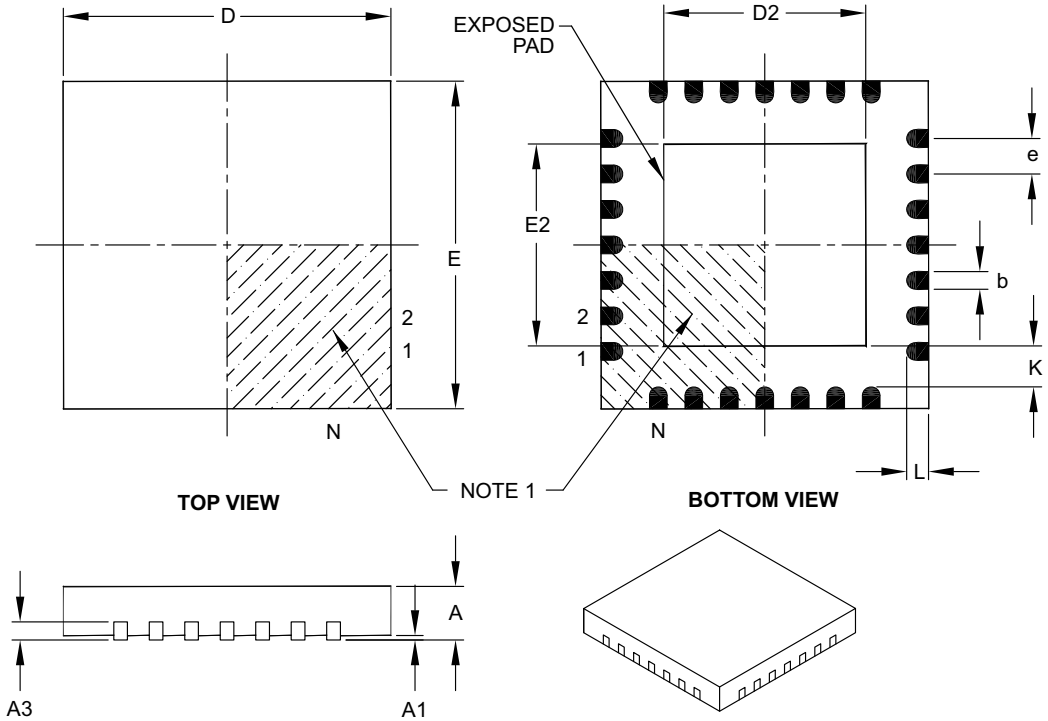
2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the Master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.70
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.70
Contact Width	b	0.23	0.38	0.43
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

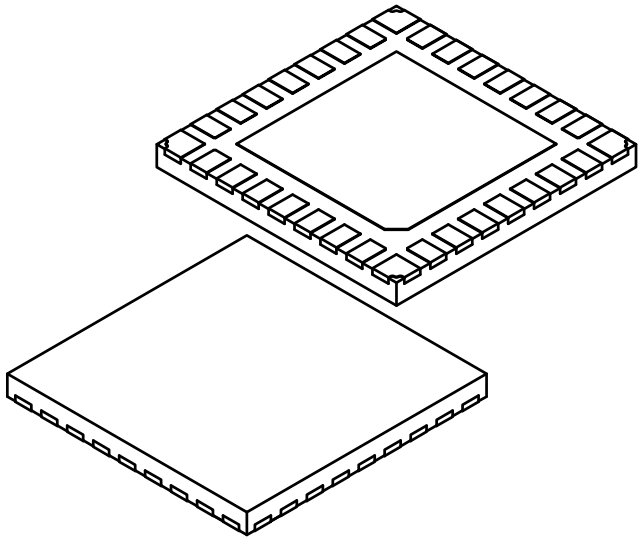
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124B

28-Lead Plastic Quad Flat, No Lead Package (MX) - 6x6x0.5mm Body [UQFN] Ultra-Thin with 0.40 x 0.60 mm Terminal Width/Length and Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.40	0.50	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	(A3)		0.127 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2		4.00	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2		4.00	
Terminal Width	b	0.35	0.40	0.45
Corner Pad	b2	0.25	0.40	0.45
Terminal Length	L	0.55	0.60	0.65
Terminal-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
4. Outermost portions of corner structures may vary slightly.

Microchip Technology Drawing C04-0209B Sheet 2 of 2