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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10b; D/A 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gs504-h-ml

TABLE 4-29: HIGH-SPEED 10-BIT ADC REGISTER MAP FOR dsPIC33FJ16GS502 DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
ADCON	0300	ADON	—	ADSIDL	SLOWCLK	—	GSWTRG	—	FORM	EIE	ORDER	SEQSAMP	ASYNCSAMP	—	ADCS2	ADCS1	ADCS0	0003	
ADPCFG	0302	—	—	—	—	—	—	—	—	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000	
ADSTAT	0306	—	—	—	—	—	—	—	—	—	P6RDY	—	—	P3RDY	P2RDY	P1RDY	P0RDY	0000	
ADBASE	0308	ADBASE<15:1>																—	0000
ADCPC0	030A	IRQEN1	PEND1	SWTRG1	TRGSRC14	TRGSRC13	TRGSRC12	TRGSRC11	TRGSRC10	IRQEN0	PEND0	SWTRG0	TRGSRC04	TRGSRC03	TRGSRC02	TRGSRC01	TRGSRC00	0000	
ADCPC1	030C	IRQEN3	PEND3	SWTRG3	TRGSRC34	TRGSRC33	TRGSRC32	TRGSRC31	TRGSRC30	IRQEN2	PEND2	SWTRG2	TRGSRC24	TRGSRC23	TRGSRC22	TRGSRC21	TRGSRC20	0000	
ADCPC3	0310	—	—	—	—	—	—	—	—	IRQEN6	PEND6	SWTRG6	TRGSRC64	TRGSRC63	TRGSRC62	TRGSRC61	TRGSRC60	0000	
ADCBUF0	0320	ADC Data Buffer 0																xxxx	
ADCBUF1	0322	ADC Data Buffer 1																xxxx	
ADCBUF2	0324	ADC Data Buffer 2																xxxx	
ADCBUF3	0326	ADC Data Buffer 3																xxxx	
ADCBUF4	0328	ADC Data Buffer 4																xxxx	
ADCBUF5	032A	ADC Data Buffer 5																xxxx	
ADCBUF6	032C	ADC Data Buffer 6																xxxx	
ADCBUF7	032E	ADC Data Buffer 7																xxxx	
ADCBUF12	0338	ADC Data Buffer 12																xxxx	
ADCBUF13	033A	ADC Data Buffer 13																xxxx	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-30: HIGH-SPEED 10-BIT ADC REGISTER MAP FOR dsPIC33FJ16GS504 DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
ADCON	0300	ADON	—	ADSIDL	SLOWCLK	—	GSWTRG	—	FORM	EIE	ORDER	SEQSAMP	ASYNCSAMP	—	ADCS2	ADCS1	ADCS0	0003	
ADPCFG	0302	—	—	—	—	PCFG11	PCFG10	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000	
ADSTAT	0306	—	—	—	—	—	—	—	—	—	P6RDY	P5RDY	P4RDY	P3RDY	P2RDY	P1RDY	P0RDY	0000	
ADBASE	0308	ADBASE<15:1>																—	0000
ADPC0	030A	IRQEN1	PEND1	SWTRG1	TRGSRC14	TRGSRC13	TRGSRC12	TRGSRC11	TRGSRC10	IRQEN0	PEND0	SWTRG0	TRGSRC04	TRGSRC03	TRGSRC02	TRGSRC01	TRGSRC00	0000	
ADPC1	030C	IRQEN3	PEND3	SWTRG3	TRGSRC34	TRGSRC33	TRGSRC32	TRGSRC31	TRGSRC30	IRQEN2	PEND2	SWTRG2	TRGSRC24	TRGSRC23	TRGSRC22	TRGSRC21	TRGSRC20	0000	
ADPC2	030E	IRQEN5	PEND5	SWTRG5	TRGSRC54	TRGSRC53	TRGSRC52	TRGSRC51	TRGSRC50	IRQEN4	PEND4	SWTRG4	TRGSRC44	TRGSRC43	TRGSRC42	TRGSRC41	TRGSRC40	0000	
ADPC3	0310	—	—	—	—	—	—	—	—	IRQEN6	PEND6	SWTRG6	TRGSRC64	TRGSRC63	TRGSRC62	TRGSRC61	TRGSRC60	0000	
ADCBUF0	0320	ADC Data Buffer 0																xxxx	
ADCBUF1	0322	ADC Data Buffer 1																xxxx	
ADCBUF2	0324	ADC Data Buffer 2																xxxx	
ADCBUF3	0326	ADC Data Buffer 3																xxxx	
ADCBUF4	0328	ADC Data Buffer 4																xxxx	
ADCBUF5	032A	ADC Data Buffer 5																xxxx	
ADCBUF6	032C	ADC Data Buffer 6																xxxx	
ADCBUF7	032E	ADC Data Buffer 7																xxxx	
ADCBUF8	0330	ADC Data Buffer 8																xxxx	
ADCBUF9	0332	ADC Data Buffer 9																xxxx	
ADCBUF10	0334	ADC Data Buffer 10																xxxx	
ADCBUF11	0336	ADC Data Buffer 11																xxxx	
ADCBUF12	0338	ADC Data Buffer 12																xxxx	
ADCBUF13	033A	ADC Data Buffer 13																xxxx	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-41: SYSTEM CONTROL REGISTER MAP

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	—	—	—	—	CM	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	xxxx ⁽¹⁾
OSCCON	0742	—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0	CLKLOCK	IOLOCK	LOCK	—	CF	—	—	OSWEN	0300 ⁽²⁾
CLKDIV	0744	ROI	DOZE2	DOZE1	DOZE0	DOZEN	FRCDIV2	FRCDIV1	FRCDIV0	PLLPOST1	PLLPOST0	—	PLLPRE4	PLLPRE3	PLLPRE2	PLLPRE1	PLLPRE0	3040
PLLFBD	0746	—	—	—	—	—	—	—	PLLDIV<8:0>									0030
REFOCON	074E	ROON	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0	—	—	—	—	—	—	—	—	0000
OSCTUN	0748	—	—	—	—	—	—	—	—	—	—	—	TUN<5:0>					0000
ACLKCON	0750	ENAPLL	APLLCK	SELACLK	—	—	APSTSCLR2	APSTSCLR1	APSTSCLR0	ASRCSEL	FRCSEL	—	—	—	—	—	—	2300

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The RCON register Reset values are dependent on the type of Reset.

2: The OSCCON register Reset values are dependent on the FOSC_x Configuration bits and on type of Reset.

TABLE 4-42: NVM REGISTER MAP

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0760	WR	WREN	WRERR	—	—	—	—	—	—	ERASE	—	—	NVMOP3	NVMOP2	NVMOP1	NVMOP0	0000 ⁽¹⁾
NVMKEY	0766	—	—	—	—	—	—	—	—	—	NVMKEY<7:0>							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset value shown is for POR only. The value on other Reset states is dependent on the state of memory write or erase operations at the time of Reset.

TABLE 4-43: PMD REGISTER MAP FOR dsPIC33FJ06GS101 DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	—	—	—	T2MD	T1MD	—	PWMMD	—	I2C1MD	—	U1MD	—	SPI1MD	—	—	ADCMD	0000
PMD2	0772	—	—	—	—	—	—	IC2MD	IC1MD	—	—	—	—	—	—	OC2MD	OC1MD	0000
PMD3	0774	—	—	—	—	—	CMPMD	—	—	—	—	—	—	—	—	—	—	0000
PMD4	0776	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—	0000
PMD6	077A	—	—	—	—	PWM4MD	—	—	PWM1MD	—	—	—	—	—	—	—	—	0000

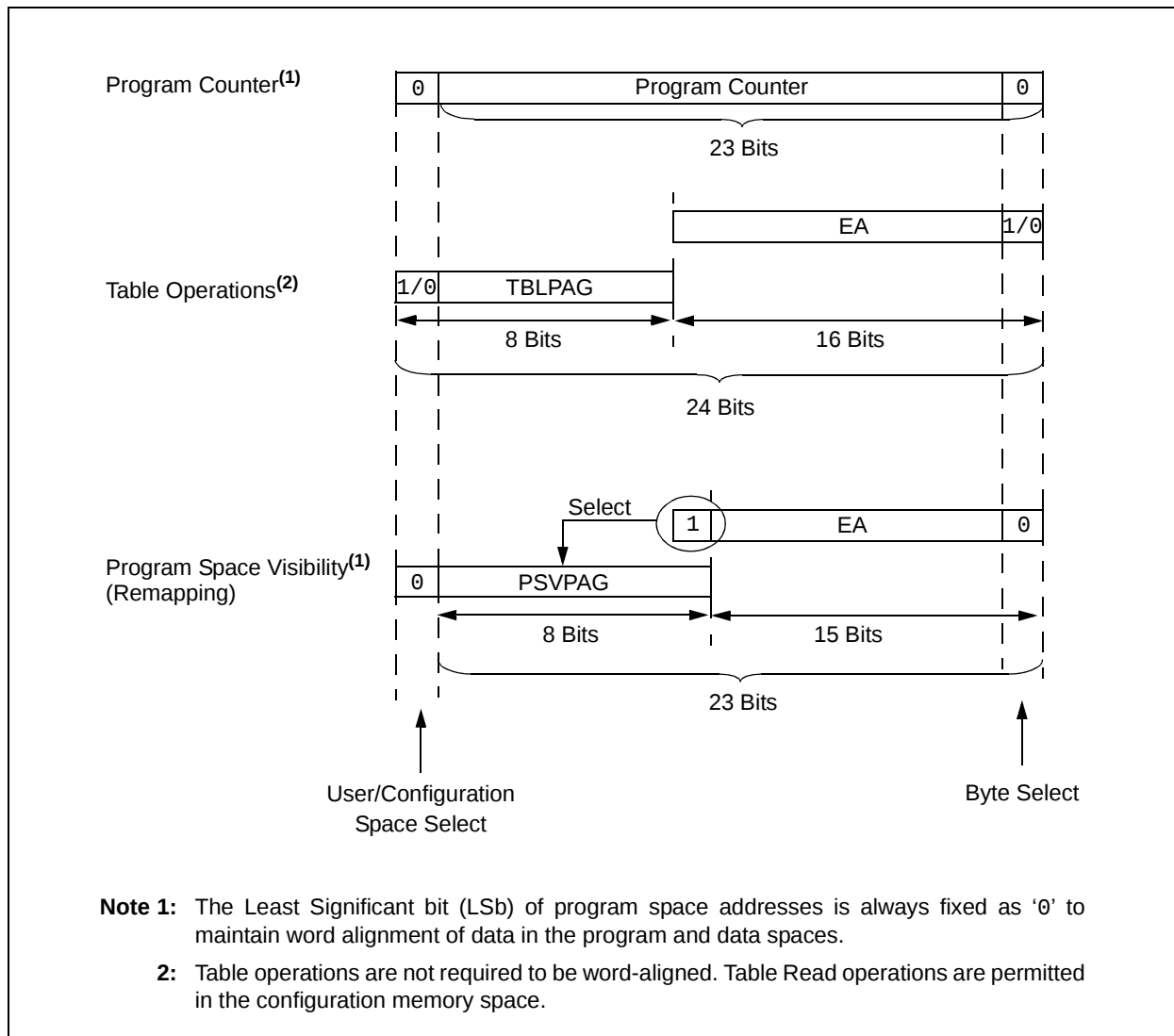
Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-44: PMD REGISTER MAP FOR dsPIC33FJ06GS102 DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	—	—	—	T2MD	T1MD	—	PWMMD	—	I2C1MD	—	U1MD	—	SPI1MD	—	—	ADCMD	0000
PMD2	0772	—	—	—	—	—	—	IC2MD	IC1MD	—	—	—	—	—	—	OC2MD	OC1MD	0000
PMD3	0774	—	—	—	—	—	CMPMD	—	—	—	—	—	—	—	—	—	—	0000
PMD4	0776	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—	0000
PMD6	077A	—	—	—	—	—	—	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

FIGURE 4-9: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



5.0 FLASH PROGRAM MEMORY

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “Flash Programming” (DS70191) in the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Run-Time Self-Programming (RTSP)

ICSP allows a dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx, and three other lines for

power (VDD), ground (VSS) and Master Clear ($\overline{\text{MCLR}}$). This allows customers to manufacture boards with unprogrammed devices and then program the Digital Signal Controller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data, either in blocks or ‘rows’ of 64 instructions (192 bytes) at a time, or a single program memory word, and erase program memory in blocks or ‘pages’ of 512 instructions (1536 bytes) at a time.

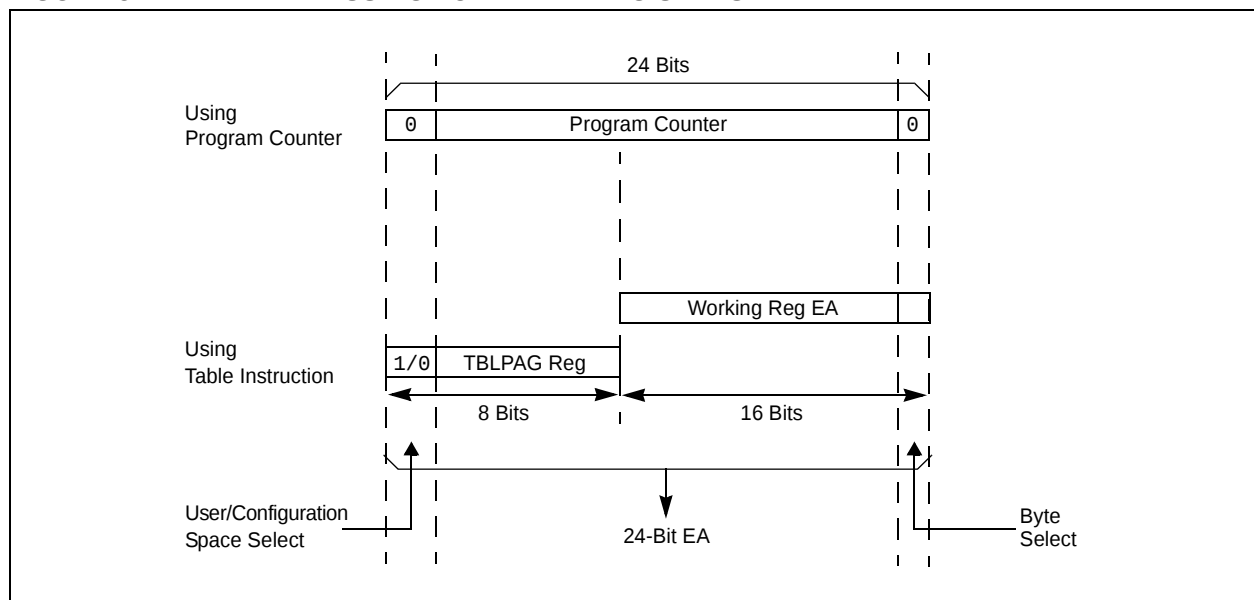
5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



7.0 INTERRUPT CONTROLLER

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Interrupts (Part IV)**” (DS70300) in the “*dsPIC33F/PIC24H Family Reference Manual*”, which is available on the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 CPU. It has the following features:

- Up to eight processor exceptions and software traps
- Seven user-selectable priority levels
- Interrupt Vector Table (IVT) with up to 118 vectors
- A unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Alternate Interrupt Vector Table (AIVT) for debug support
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The Interrupt Vector Table (IVT) is shown in Figure 7-1. The IVT resides in program memory, starting at location 000004h. The IVT contains 126 vectors, consisting of eight nonmaskable trap vectors, plus up to 118 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit-wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 will take priority over interrupts at any other vector address.

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices implement up to 35 unique interrupts and 4 non-maskable traps. These are summarized in Table 7-1.

7.1.1 ALTERNATE INTERRUPT VECTOR TABLE

The Alternate Interrupt Vector Table (AIVT) is located after the IVT, as shown in Figure 7-1. Access to the AIVT is provided by the ALTIVT control bit (INTCON2<15>). If the ALTIVT bit is set, all interrupt and exception processes use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors.

The AIVT supports debugging by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time. If the AIVT is not needed, the AIVT should be programmed with the same addresses used in the IVT.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices clear their registers in response to a Reset, which forces the PC to zero. The Digital Signal Controller then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT and AIVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 7-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0 (CONTINUED)

- bit 1 **IC1IF:** Input Capture Channel 1 Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 0 **INT0IF:** External Interrupt 0 Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

REGISTER 7-32: IPC27: INTERRUPT PRIORITY CONTROL REGISTER 27

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	ADCP1IP2	ADCP1IP1	ADCP1IP0	—	ADCP0IP2	ADCP0IP1	ADCP0IP0
bit 15				bit 8			

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **ADCP1IP<2:0>:** ADC Pair 1 Conversion Done Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **ADCP0IP<2:0>:** ADC Pair 0 Conversion Done Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 7-0 **Unimplemented:** Read as '0'

9.0 POWER-SAVING FEATURES

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Watchdog Timer and Power-Saving Modes**” (DS70196) in the “*dsPIC33F/PIC24H Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices can manage power consumption in four different ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application’s power consumption while still maintaining critical application features, such as timing-sensitive communications.

9.1 Clock Frequency and Clock Switching

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSC<2:0> bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 8.0 “Oscillator Configuration”**.

9.2 Instruction-Based Power-Saving Modes

The dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices have two special power-saving modes that are entered through the execution of a special PWSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWSAV instruction is shown in Example 9-1.

Note: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to wake-up.

9.2.1 SLEEP MODE

The following occur in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled
- The LPRC clock continues to run in Sleep mode if the WDT is enabled
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode
- Some device features or peripherals may continue to operate. This includes the items such as the Input Change Notification on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled

The device will wake-up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

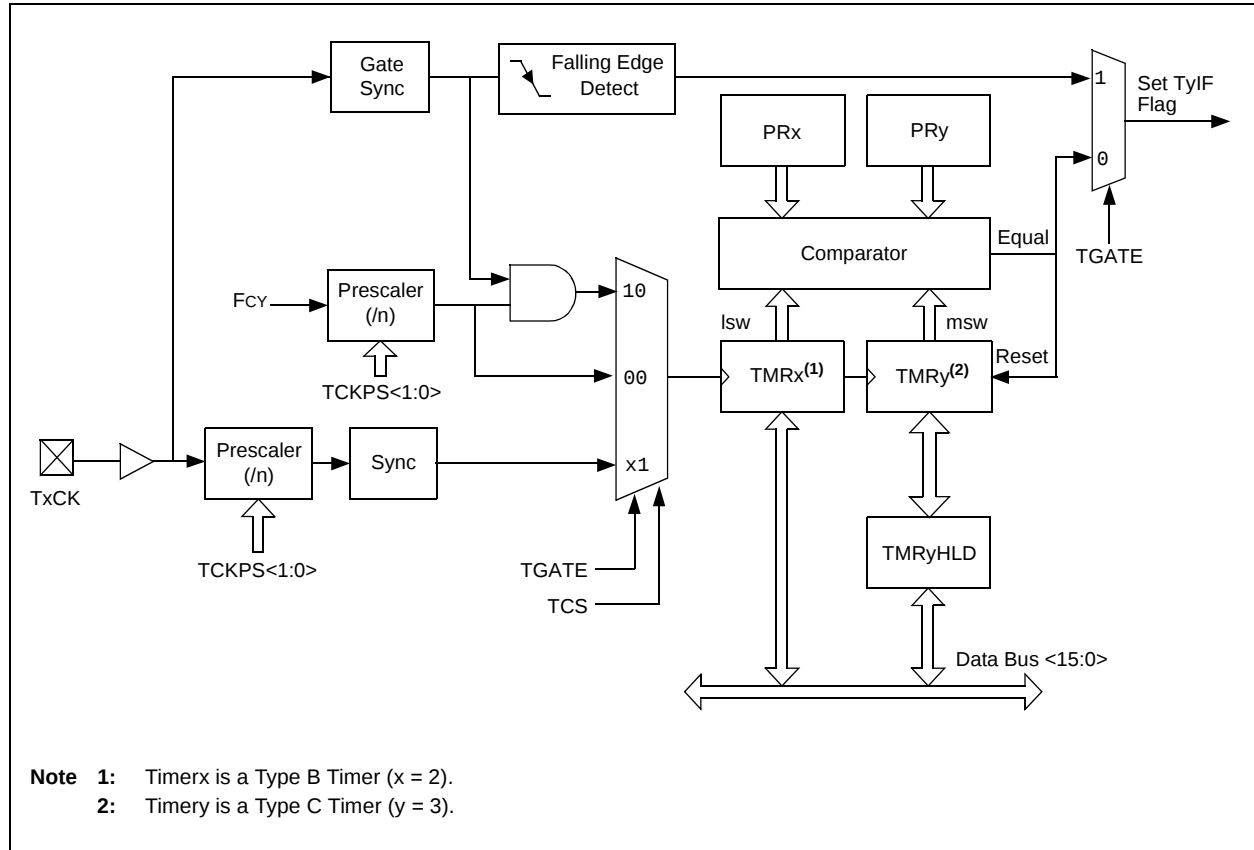
On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

EXAMPLE 9-1: PWSAV INSTRUCTION SYNTAX

```
PWSAV #SLEEP_MODE    ; Put the device into SLEEP mode
PWSAV #IDLE_MODE      ; Put the device into IDLE mode
```

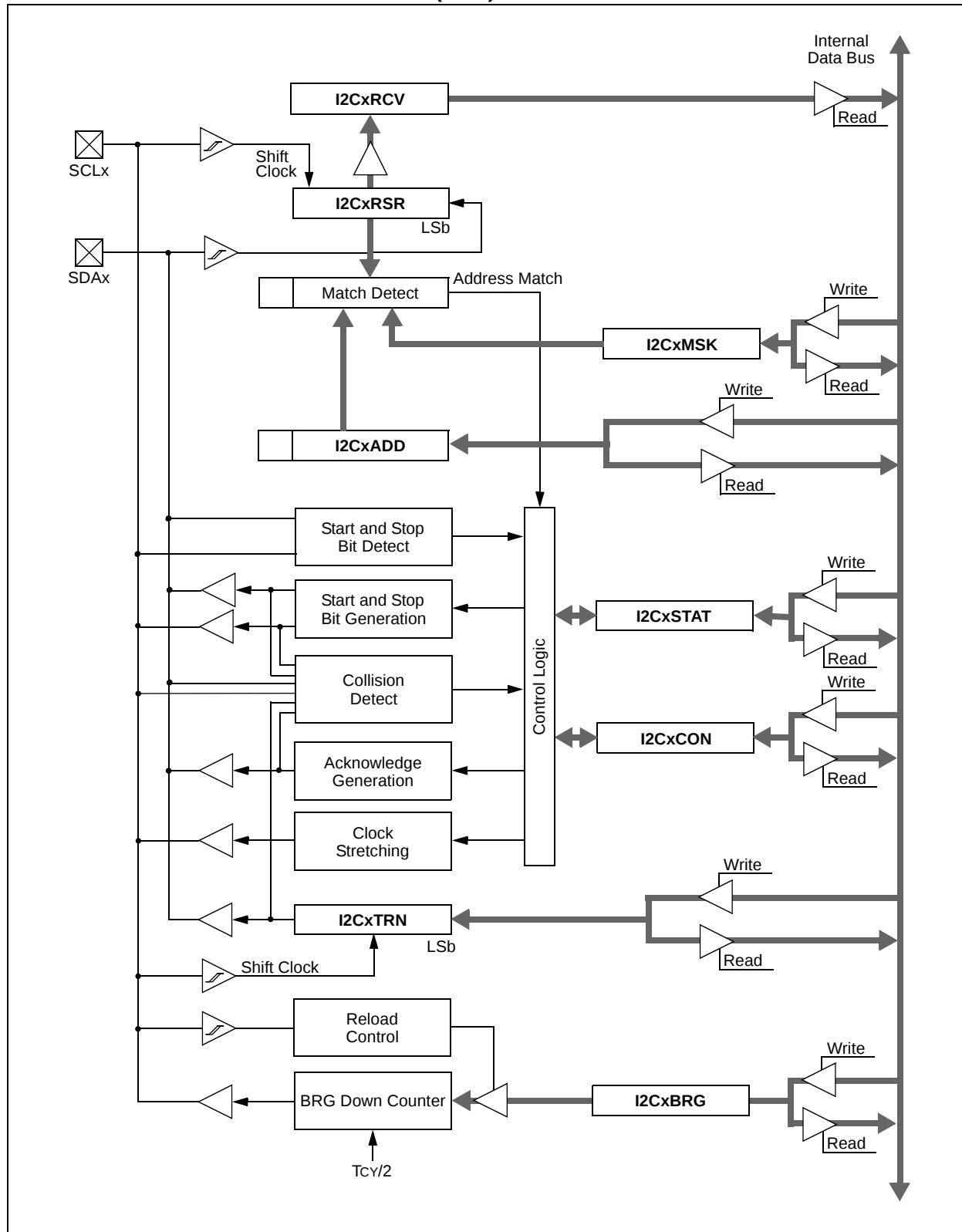
dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

FIGURE 12-3: 32-BIT TIMER BLOCK DIAGRAM



dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

FIGURE 17-1: I2Cx BLOCK DIAGRAM (x = 1)



dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

TABLE 21-2: dsPIC33F CONFIGURATION BITS DESCRIPTION

Bit Field	Register	RTSP Effect	Description
BWRP	FBS	Immediate	Boot Segment Program Flash Write Protection bit 1 = Boot segment can be written 0 = Boot segment is write-protected
BSS<2:0>	FBS	Immediate	Boot Segment Program Flash Code Protection Size bits x11 = No boot program Flash segment <u>Boot Space is 256 Instruction Words (except interrupt vectors):</u> 110 = Standard security; boot program Flash segment ends at 0x0003FE 010 = High security; boot program Flash segment ends at 0x0003FE <u>Boot Space is 768 Instruction Words (except interrupt vectors):</u> 101 = Standard security; boot program Flash segment ends at 0x0007FE 001 = High security; boot program Flash segment ends at 0x0007FE <u>Boot Space is 1792 Instruction Words (except interrupt vectors):</u> 100 = Standard security; boot program Flash segment ends at 0x000FFE 000 = High security; boot program Flash segment ends at 0x000FFE
GSS<1:0>	FGS	Immediate	General Segment Code-Protect bits 11 = User program memory is not code-protected 10 = Standard security 0x = High security
GWRP	FGS	Immediate	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
IESO	FOSCSEL	Immediate	Two-speed Oscillator Start-up Enable bit 1 = Start-up device with FRC, then automatically switch to the user-selected oscillator source when ready 0 = Start-up device with user-selected oscillator source
FNOSC<2:0>	FOSCSEL	If clock switch is enabled, RTSP effect is on any device Reset; otherwise, Immediate	Initial Oscillator Source Selection bits 111 = Internal Fast RC (FRC) Oscillator with Postscaler 110 = Internal Fast RC (FRC) Oscillator with Divide-by-16 101 = LPRC Oscillator 100 = Reserved 011 = Primary (XT, HS, EC) Oscillator with PLL 010 = Primary (XT, HS, EC) Oscillator 001 = Internal Fast RC (FRC) Oscillator with PLL 000 = FRC Oscillator
FCKSM<1:0>	FOSC	Immediate	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	FOSC	Immediate	Peripheral Pin Select Configuration bit 1 = Allows only one reconfiguration 0 = Allows multiple reconfigurations
OSCIOFNC	FOSC	Immediate	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is the general purpose digital I/O pin

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
10	BTSC	BTSC $f, \#bit4$	Bit Test f , Skip if Clear	1	1 (2 or 3)	None
		BTSC $ws, \#bit4$	Bit Test Ws , Skip if Clear	1	1 (2 or 3)	None
11	BTSS	BTSS $f, \#bit4$	Bit Test f , Skip if Set	1	1 (2 or 3)	None
		BTSS $ws, \#bit4$	Bit Test Ws , Skip if Set	1	1 (2 or 3)	None
12	BTST	BTST $f, \#bit4$	Bit Test f	1	1	Z
		BTST.C $ws, \#bit4$	Bit Test Ws to C	1	1	C
		BTST.Z $ws, \#bit4$	Bit Test Ws to Z	1	1	Z
		BTST.C ws, Wb	Bit Test $Ws < Wb >$ to C	1	1	C
		BTST.Z ws, Wb	Bit Test $Ws < Wb >$ to Z	1	1	Z
13	BTSTS	BTSTS $f, \#bit4$	Bit Test then Set f	1	1	Z
		BTSTS.C $ws, \#bit4$	Bit Test Ws to C, then Set	1	1	C
		BTSTS.Z $ws, \#bit4$	Bit Test Ws to Z, then Set	1	1	Z
14	CALL	CALL $lit23$	Call Subroutine	2	2	None
		CALL wn	Call Indirect Subroutine	1	2	None
15	CLR	CLR f	$f = 0x0000$	1	1	None
		CLR $WREG$	$WREG = 0x0000$	1	1	None
		CLR ws	$Ws = 0x0000$	1	1	None
		CLR $Acc, Wx, Wxd, Wy, Wyd, AWB$	Clear Accumulator	1	1	OA, OB, SA, SB
16	CLRWDT	CLRWDT	Clear Watchdog Timer	1	1	WDTO, Sleep
17	COM	COM f	$f = \bar{f}$	1	1	N, Z
		COM $f, WREG$	$WREG = \bar{f}$	1	1	N, Z
		COM ws, Wd	$Wd = \bar{Ws}$	1	1	N, Z
18	CP	CP f	Compare f with $WREG$	1	1	C, DC, N, OV, Z
		CP $Wb, \#lit5$	Compare Wb with $lit5$	1	1	C, DC, N, OV, Z
		CP Wb, Ws	Compare Wb with Ws ($Wb - Ws$)	1	1	C, DC, N, OV, Z
19	CP0	CP0 f	Compare f with $0x0000$	1	1	C, DC, N, OV, Z
		CP0 ws	Compare Ws with $0x0000$	1	1	C, DC, N, OV, Z
20	CPB	CPB f	Compare f with $WREG$, with Borrow	1	1	C, DC, N, OV, Z
		CPB $Wb, \#lit5$	Compare Wb with $lit5$, with Borrow	1	1	C, DC, N, OV, Z
		CPB Wb, Ws	Compare Wb with Ws , with Borrow ($Wb - Ws - C$)	1	1	C, DC, N, OV, Z
21	CPSEQ	CPSEQ Wb, Wn	Compare Wb with Wn , Skip if =	1	1 (2 or 3)	None
22	CPSGT	CPSGT Wb, Wn	Compare Wb with Wn , Skip if >	1	1 (2 or 3)	None
23	CPSLT	CPSLT Wb, Wn	Compare Wb with Wn , Skip if <	1	1 (2 or 3)	None
24	CPSNE	CPSNE Wb, Wn	Compare Wb with Wn , Skip if $\neq$	1	1 (2 or 3)	None
25	DAW	DAW Wn	$Wn = \text{Decimal Adjust } Wn$	1	1	C
26	DEC	DEC f	$f = f - 1$	1	1	C, DC, N, OV, Z
		DEC $f, WREG$	$WREG = f - 1$	1	1	C, DC, N, OV, Z
		DEC ws, Wd	$Wd = Ws - 1$	1	1	C, DC, N, OV, Z
27	DEC2	DEC2 f	$f = f - 2$	1	1	C, DC, N, OV, Z
		DEC2 $f, WREG$	$WREG = f - 2$	1	1	C, DC, N, OV, Z
		DEC2 ws, Wd	$Wd = Ws - 2$	1	1	C, DC, N, OV, Z
28	DISI	DISI $\#lit14$	Disable Interrupts for k Instruction Cycles	1	1	None

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

24.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on V _{DD} with respect to V _{SS}	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to V _{SS} ⁽³⁾	-0.3V to (V _{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V _{SS} , when V _{DD} ≥ 3.0V ⁽³⁾	-0.3V to +5.6V
Voltage on any 5V tolerant pin with respect to V _{SS} , when V _{DD} < 3.0V ⁽³⁾	-0.3V to (V _{DD} + 0.3V)
Maximum current out of V _{SS} pin	300 mA
Maximum current into V _{DD} pin ⁽²⁾	250 mA
Maximum current sourced/sunk by any 4x I/O pin	15 mA
Maximum current sourced/sunk by any 8x I/O pin	25 mA
Maximum current sourced/sunk by any 16x I/O pin	45 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports ⁽²⁾	200mA

Note 1: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 24-2).

3: See the “Pin Diagrams” section for 5V tolerant pins.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

24.1 DC Characteristics

TABLE 24-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)	Temp Range (in °C)	Max MIPS
			dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04
—	3.0-3.6V ⁽¹⁾	-40°C to +85°C	40
—	3.0-3.6V ⁽¹⁾	-40°C to +125°C	40

Note 1: Overall functional device operation at $V_{BORMIN} < V_{DD} < V_{DDMIN}$ is tested but not characterized. All device analog modules such as the ADC, etc., will function but with degraded performance below V_{DDMIN} . Refer to Parameter BO10 in Table 24-11 for BOR values.

TABLE 24-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal chip power dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$ I/O Pin Power Dissipation: $I/O = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$	PD	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	PD _{MAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 24-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit	Notes
Package Thermal Resistance, 44-Pin QFN	θ_{JA}	28	—	°C/W	1
Package Thermal Resistance, 44-Pin TFQP	θ_{JA}	39	—	°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θ_{JA}	42	—	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θ_{JA}	47	—	°C/W	1
Package Thermal Resistance, 28-Pin QFN-S	θ_{JA}	34	—	°C/W	1
Package Thermal Resistance, 18-Pin SOIC	θ_{JA}	57	—	°C/W	1
Package Thermal Resistance, 44-Pin VTLA	θ_{JA}	25	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

FIGURE 24-3: I/O TIMING CHARACTERISTICS

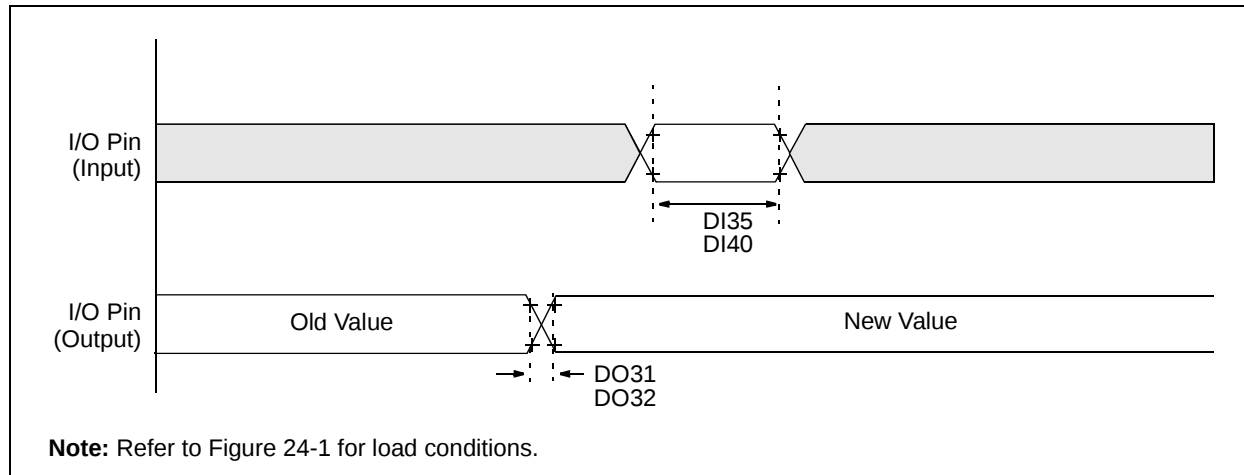


TABLE 24-21: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended					
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
DO31	TioR	Port Output Rise Time:					
		4x Source Driver Pins – RA0-RA2, RB0-RB2, RB5-RB10, RB15, RC1, RC2, RC9, RC10	—	10	25	ns	Refer to Figure 24-1 for test conditions
		8x Source Driver Pins – RC0, RC3-RC8, RC11-RC13	—	8	20	ns	
		16x Source Driver Pins – RA3, RA4, RB3, RB4, RB11-RB14	—	6	15	ns	
DO32	TioF	Port Output Fall Time:					
		4x Source Driver Pins – RA0-RA2, RB0-RB2, RB5-RB10, RB15, RC1, RC2, RC9, RC10	—	10	25	ns	Refer to Figure 24-1 for test conditions
		8x Source Driver Pins – RC0, RC3-RC8, RC11-RC13	—	8	20	ns	
		16x Source Driver Pins – RA3, RA4, RB3, RB4, RB11-RB14	—	6	15	ns	
DI35	TiNP	INTx Pin High or Low Time (input)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	Tcy	

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

TABLE 24-30: SPIx MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	CKP	SMP
15 MHz	Table 24-31	—	—	0,1	0,1	0,1
9 MHz	—	Table 24-32	—	1	0,1	1
9 MHz	—	Table 24-33	—	0	0,1	1
15 MHz	—	—	Table 24-34	1	0	0
11 MHz	—	—	Table 24-35	1	1	0
15 MHz	—	—	Table 24-36	0	1	0
11 MHz	—	—	Table 24-37	0	0	0

FIGURE 24-11: SPIx MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS

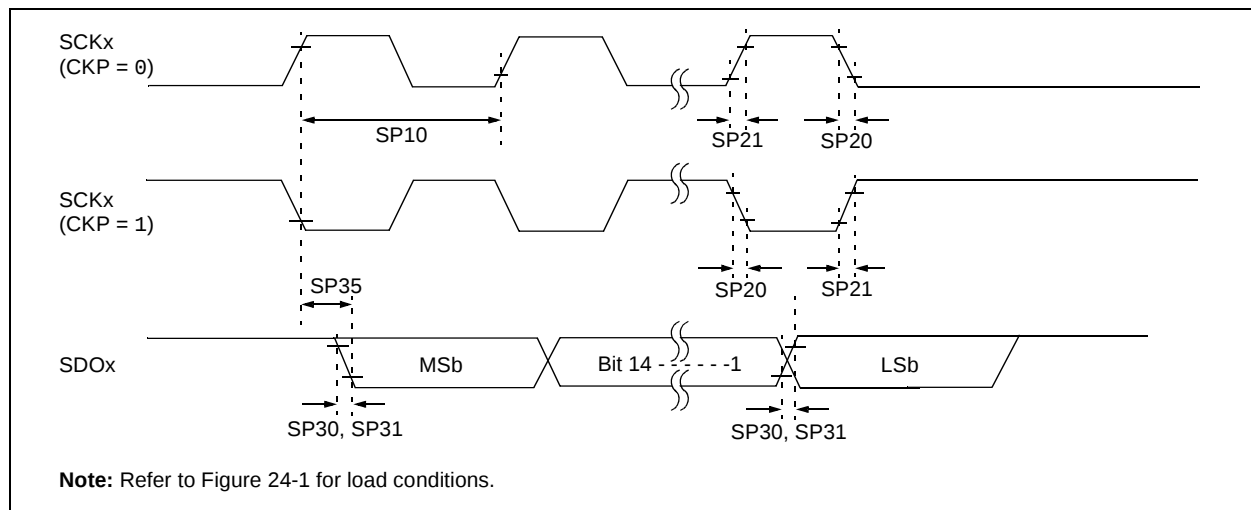
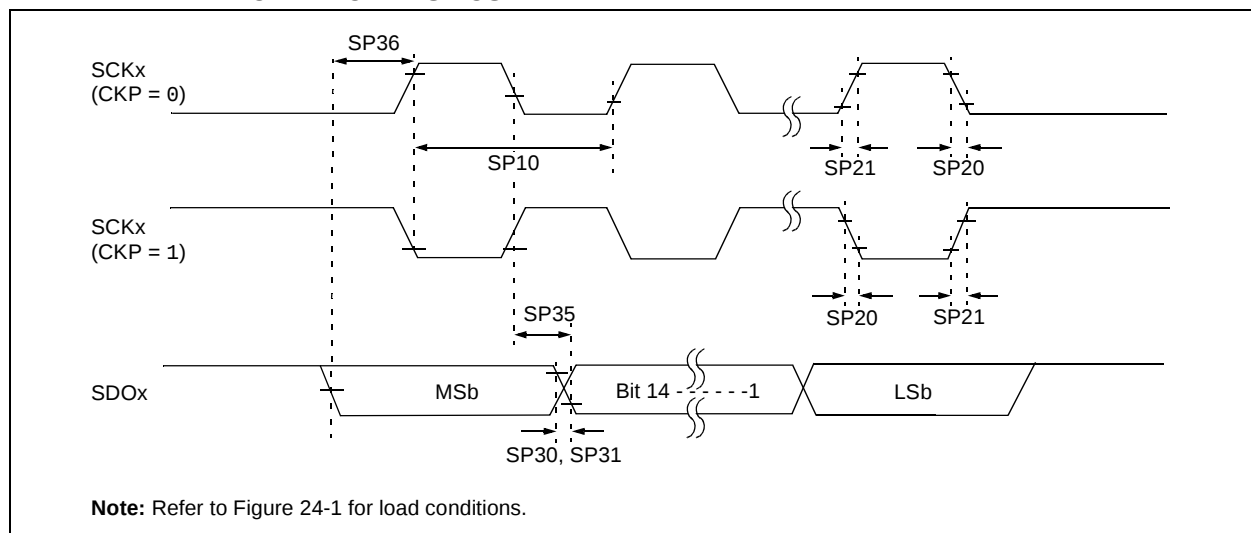


FIGURE 24-12: SPIx MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS



dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04

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