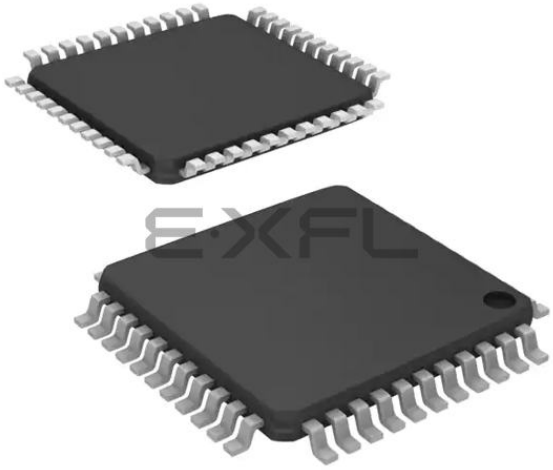

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Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
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Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
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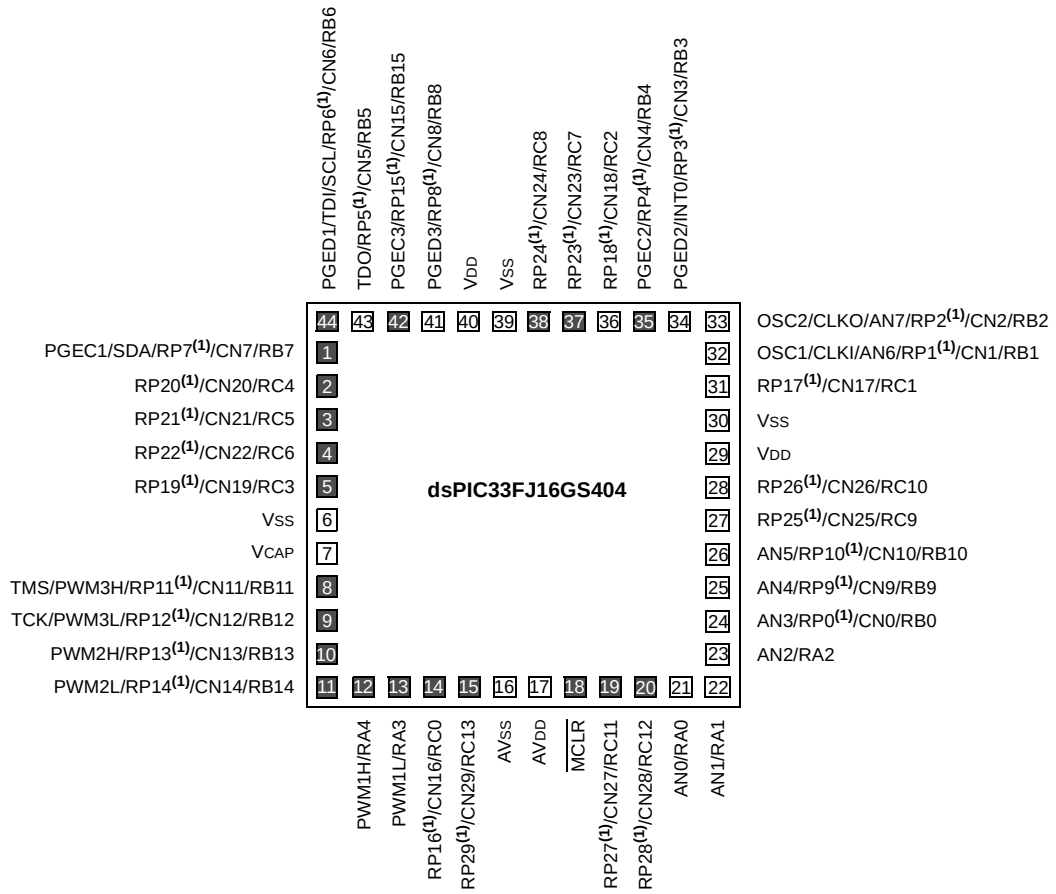
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gs504-h-pt

Pin Diagrams (Continued)

44-Pin VTLA(2)

■ = Pins are up to 5V tolerant



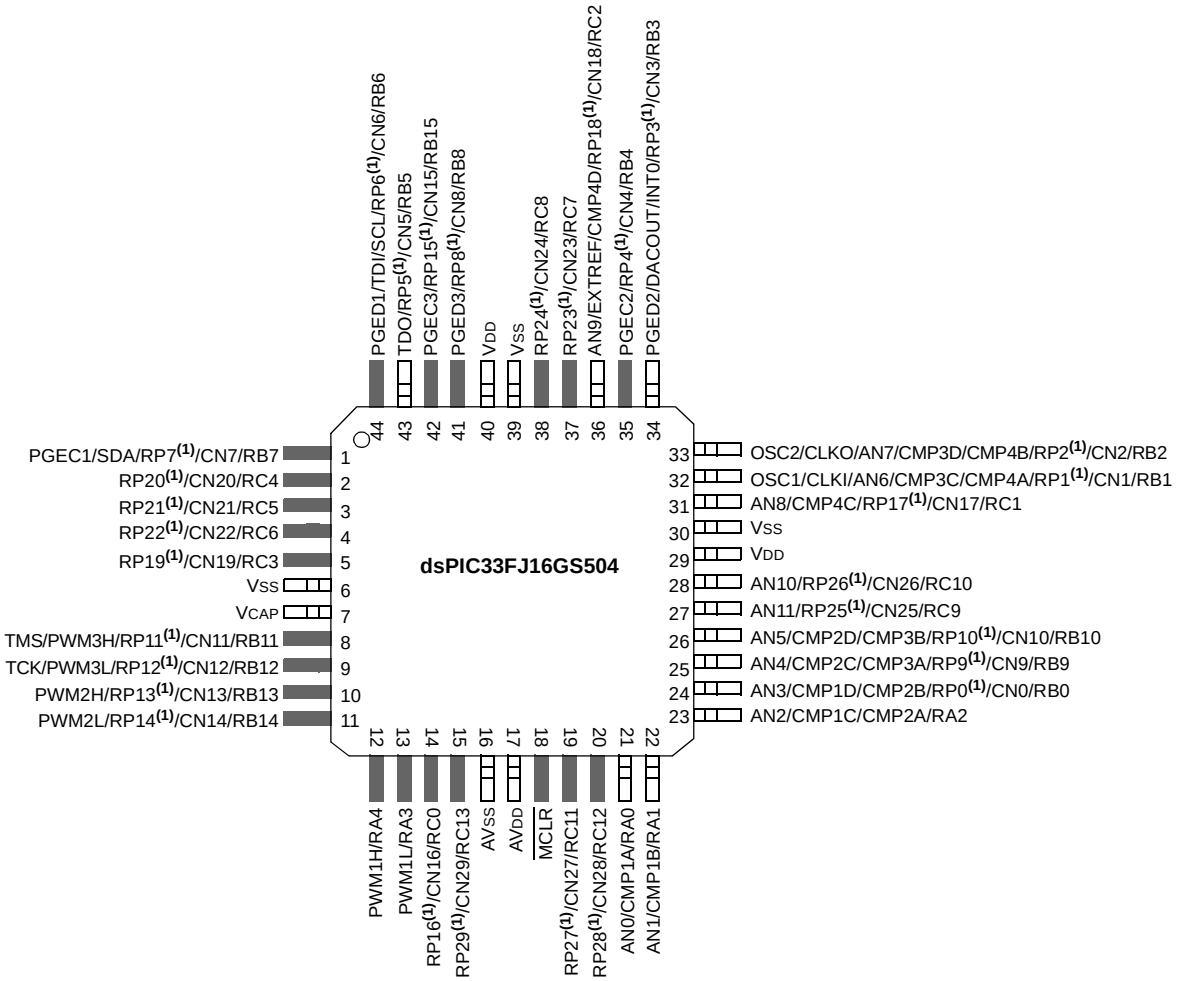
Note 1: The RPn pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.

2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

44-Pin TQFP

■ = Pins are up to 5V tolerant



Note 1: The RPn pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.

FIGURE 2-10: PHASE-SHIFTED FULL-BRIDGE CONVERTER

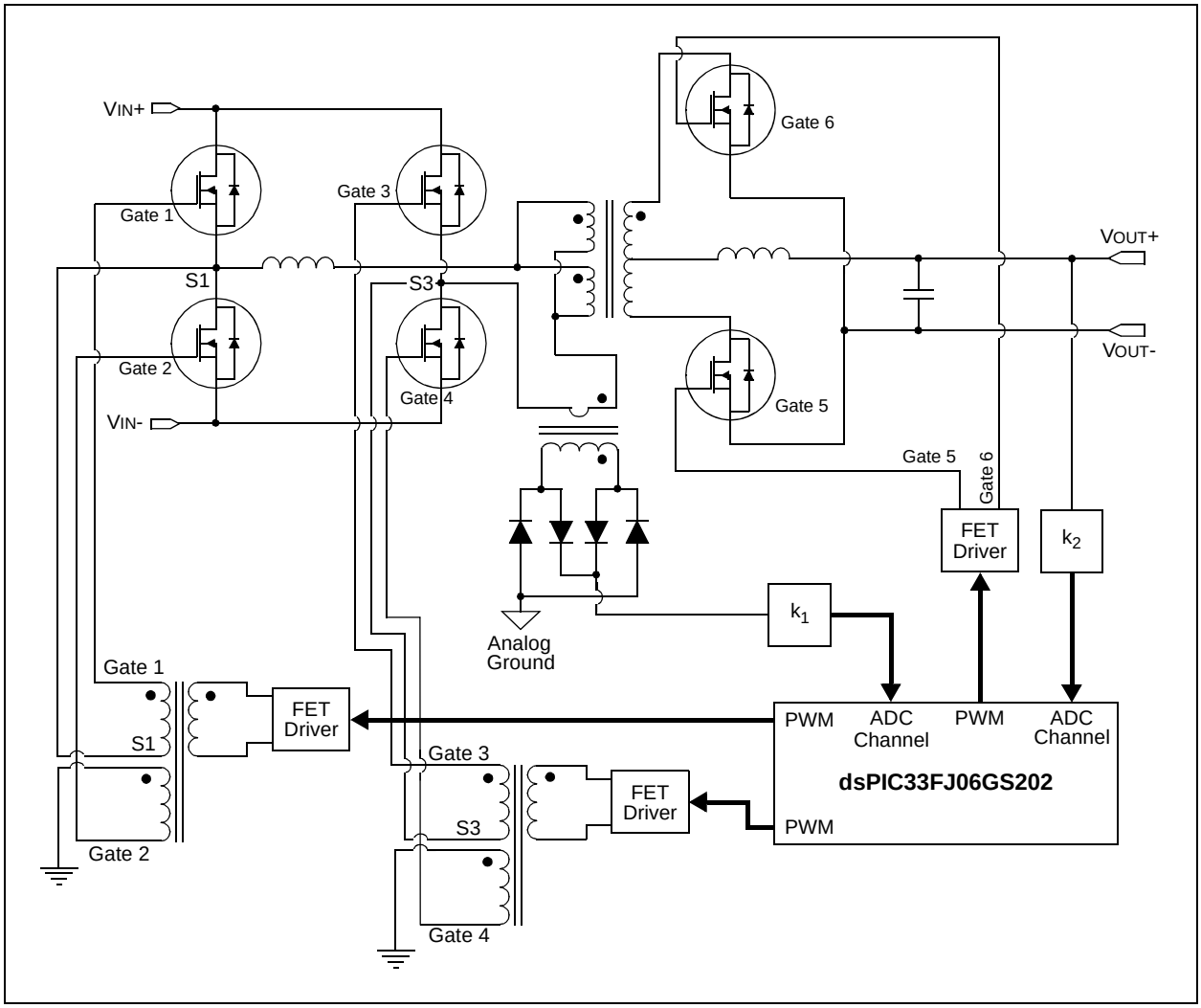


FIGURE 4-4: DATA MEMORY MAP FOR dsPIC33FJ06GS202 DEVICE WITH 1-KBYTE RAM

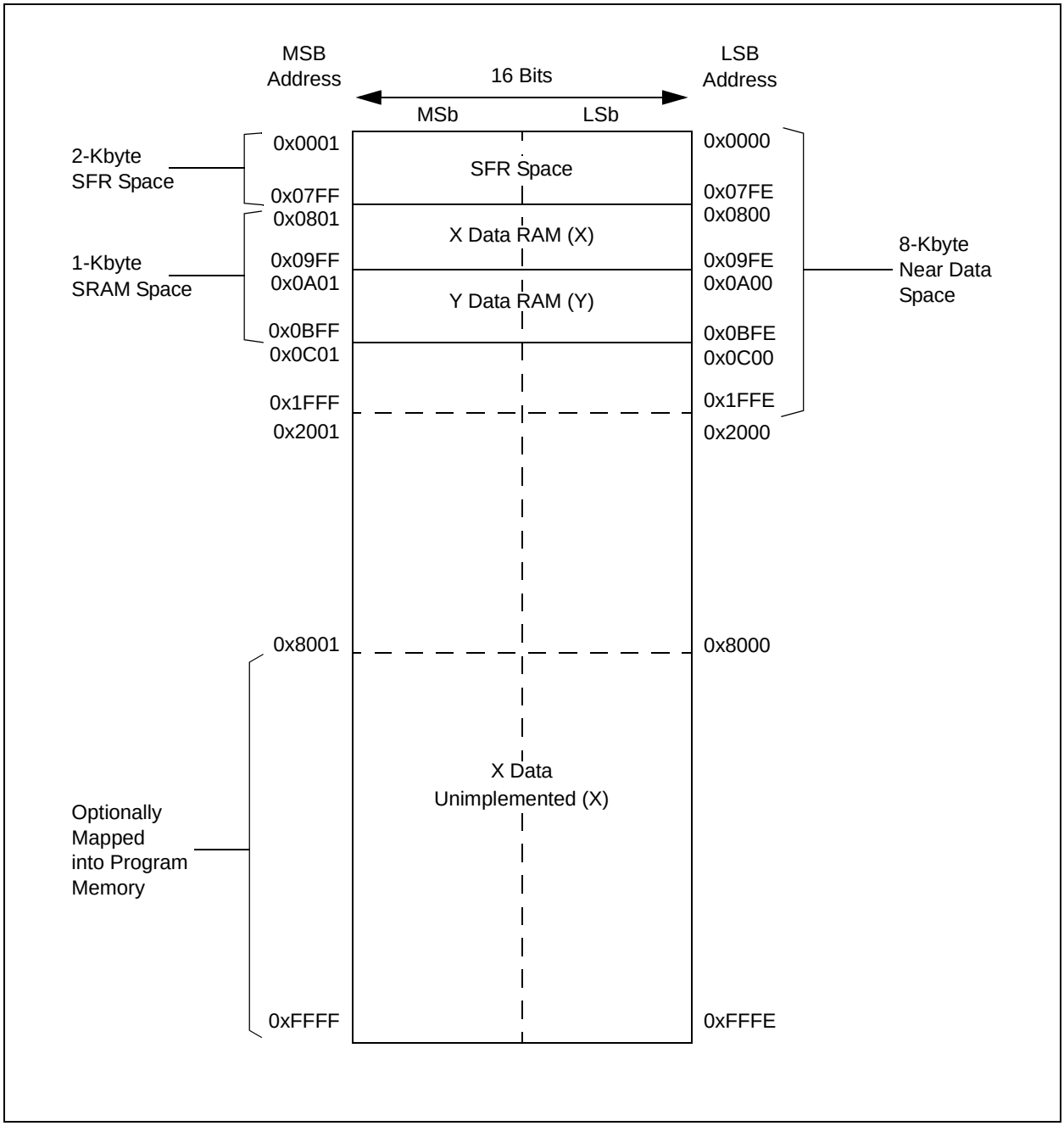


FIGURE 4-5: DATA MEMORY MAP FOR dsPIC33FJ16GS402/404/502/504 DEVICES WITH 2-KBYTE RAM

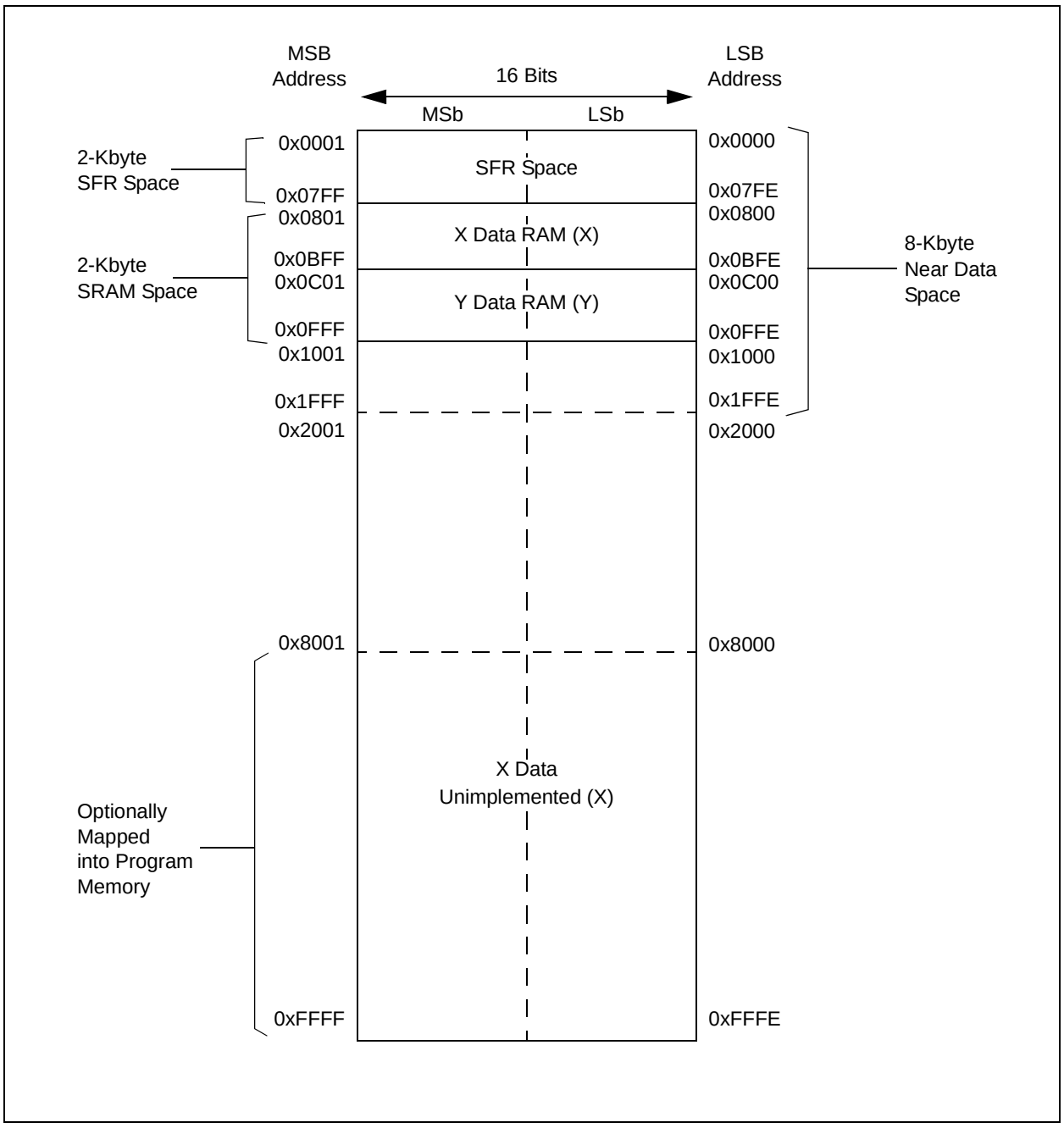


TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33FJ06GS102 DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	—	ADIF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	—	T2IF	—	—	—	T1IF	OC1IF	—	INT0IF	0000
IFS1	0086	—	—	INT2IF	—	—	—	—	—	—	—	—	INT1IF	CNIF	—	MI2C1IF	SI2C1IF	0000
IFS3	008A	—	—	—	—	—	—	PSEMIF	—	—	—	—	—	—	—	—	—	0000
IFS4	008C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIF	—	0000
IFS5	008E	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	0090	ADCP1IF	ADCP0IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS7	0092	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP2IF	0000
IEC0	0094	—	—	ADIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	—	T2IE	—	—	—	T1IE	OC1IE	—	INT0IE	0000
IEC1	0096	—	—	INT2IE	—	—	—	—	—	—	—	—	INT1IE	CNIE	—	MI2C1IE	SI2C1IE	0000
IEC3	009A	—	—	—	—	—	—	PSEMIE	—	—	—	—	—	—	—	—	—	0000
IEC4	009C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIE	—	0000
IEC5	009E	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	00A0	ADCP1IE	ADCP0IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC7	00A2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP2IE	0000
IPC0	00A4	—	T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0	—	—	—	—	—	INT0IP2	INT0IP1	INT0IP0	4404
IPC1	00A6	—	T2IP2	T2IP1	T2IP0	—	—	—	—	—	—	—	—	—	—	—	—	4000
IPC2	00A8	—	U1RXIP2	U1RXIP2	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0	—	SPI1EIP2	SPI1EIP1	SPI1EIP0	—	—	—	—	4440
IPC3	00AA	—	—	—	—	—	—	—	—	-—	ADIP2	ADIP1	ADIP0	—	U1TXIP2	U1TXIP1	U1TXIP0	0044
IPC4	00AC	—	CNIP2	CNIP1	CNIP0	—	—	—	—	—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0	4044
IPC5	00AE	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0	0004
IPC7	00B2	—	—	—	—	—	—	—	—	—	INT2IP2	INT2IP1	INT2IP0	—	—	—	—	0040
IPC14	00C0	—	—	—	—	—	—	—	—	—	PSEMIP2	PSEMIP1	PSEMIP0	—	—	—	—	0040
IPC16	00C4	—	—	—	—	—	—	—	—	—	U1EIP2	U1EIP1	U1EIP0	—	—	—	—	0040
IPC23	00D2	—	PWM2IP2	PWM2IP1	PWM2IP0	—	PWM1IP2	PWM1IP1	PWM1IP0	—	—	—	—	—	—	—	—	4400
IPC27	00DA	—	ADCP1IP2	ADCP1IP1	ADCP1IP0	—	ADCP0IP2	ADCP0IP1	ADCP0IP0	—	—	—	—	—	—	—	—	4400
IPC28	00DC	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP2IP2	ADCP2IP1	ADCP2IP0	0004
INTTREG	00E0	—	—	—	—	ILR3	ILR2	ILR1	ILR0	—	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-48: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn forms the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn forms the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

4.3.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions and the DSP accumulator class of instructions to provide a greater addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (register offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-bit Literal
- 16-bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.3.4 MAC INSTRUCTIONS

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY.N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The two-source operand prefetch registers must be members of the set {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must, therefore, be valid addresses within X data space for W8 and W9 and Y data space for W10 and W11.

Note: Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the MAC class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.3.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ADD Acc, the source of an operand or result is implied by the opcode itself. Certain operations, such as NOP, do not have any operands.

REGISTER 7-14: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	PSEMIE	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as ‘0’

bit 9 **PSEMIE:** PWM Special Event Match Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 8-0 **Unimplemented:** Read as ‘0’

REGISTER 7-15: IEC4: INTERRUPT ENABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	U1EIE	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-2 **Unimplemented:** Read as ‘0’

bit 1 **U1EIE:** UART1 Error Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 0 **Unimplemented:** Read as ‘0’

REGISTER 7-28: IPC23: INTERRUPT PRIORITY CONTROL REGISTER 23

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	PWM2IP2	PWM2IP1	PWM2IP0	—	PWM1IP2	PWM1IP1	PWM1IP0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **PWM2IP<2:0>:** PWM2 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **PWM1IP<2:0>:** PWM1 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 7-30: IPC25: INTERRUPT PRIORITY CONTROL REGISTER 25

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	AC2IP2	AC2IP1	AC2IP0	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **AC2IP<2:0>:** Analog Comparator 2 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11-01 **Unimplemented:** Read as '0'

REGISTER 15-7: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PDCx<15:0>:** PWM Generator # Duty Cycle Value bits

Note 1: In Independent PWM mode, the PDCx register controls the PWMxH duty cycle only. In Complementary, Redundant and Push-Pull PWM modes, the PDCx register controls the duty cycle of both the PWMxH and PWMxL. The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0009, while the maximum pulse width generated corresponds to a value of Period-0x0008.

2: As the duty cycle gets closer to 0% or 100% of the PWM period (0 ns-40 ns, depending on the mode of operation), the PWM duty cycle resolution will degrade from 1 LSB to 3 LSBs.

REGISTER 15-8: SDCx: PWMx SECONDARY DUTY CYCLE REGISTER(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDCx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDCx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **SDCx<15:0>:** Secondary Duty Cycle for PWMxL Output Pin bits

Note 1: The SDCx register is used in Independent PWM mode only. When used in Independent PWM mode, the SDCx register controls the PWMxL duty cycle. The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0009, while the maximum pulse width generated corresponds to a value of Period-0x0008.

2: As the duty cycle gets closer to 0% or 100% of the PWM period (0 ns-40 ns, depending on the mode of operation), the PWM duty cycle resolution will degrade from 1 LSB to 3 LSBs.

REGISTER 15-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **PHASEx<15:0>:** PWM Phase-Shift Value or Independent Time Base Period for this PWM Generator bits

Note 1: If PWMCONx<ITB> = 0, the following applies based on the mode of operation:

- Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10); PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs
- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11); PHASEx<15:0> = Phase-shift value for PWMxL only

2: If PWMCONx<ITB> = 1, the following applies based on the mode of operation:

- Complementary, Redundant, and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10); PHASEx<15:0> = Independent Time Base period value for PWMxH and PWMxL
- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11); PHASEx<15:0> = Independent Time Base period value for PWMxL only
- The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0008, while the maximum pulse width generated corresponds to a value of Period – 0x0008.

REGISTER 19-8: ADCPC3: ANALOG-TO-DIGITAL CONVERT PAIR CONTROL REGISTER 3(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN6	PEND6	SWTRG6	TRGSRC6<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **IRQEN6:** Interrupt Request Enable 6 bit
1 = Enables IRQ generation when requested conversion of Channels AN13 and AN12 is completed
0 = IRQ is not generated

bit 6 **PEND6:** Pending Conversion Status 6 bit
1 = Conversion of Channels AN13 and AN 12 is pending; set when selected trigger is asserted
0 = Conversion is complete

bit 5 **SWTRG6:** Software Trigger 6 bit
1 = Starts conversion of AN13 (INTREF) and AN12 (EXTREF) (if selected by the TRGSRCx bits)(2)
This bit is automatically cleared by hardware when the PEND6 bit is set.
0 = Conversion has not started

Note 1: This register is only implemented on the dsPIC33FJ16GS502 and dsPIC33FJ16GS504 devices.

2: The trigger source must be set as global software trigger prior to setting this bit to '1'. If other conversions are in progress, conversion will be performed when the conversion resources are available.

REGISTER 19-8: ADCPC3: ANALOG-TO-DIGITAL CONVERT PAIR CONTROL REGISTER 3(1)

bit 4-0 **TRGSRC6<4:0>:** Trigger 6 Source Selection bits

Selects trigger source for conversion of Analog Channels AN13 and AN12.
11111 = Timer2 period match
•
•
•
11011 = Reserved
11010 = PWM Generator 4 current-limit ADC trigger
11001 = PWM Generator 3 current-limit ADC trigger
11000 = PWM Generator 2 current-limit ADC trigger
10111 = PWM Generator 1 current-limit ADC trigger
10110 = Reserved
•
•
•
10010 = Reserved
10001 = PWM Generator 4 secondary trigger is selected
10000 = PWM Generator 3 secondary trigger is selected
01111 = PWM Generator 2 secondary trigger is selected
01110 = PWM Generator 1 secondary trigger is selected
01101 = Reserved
01100 = Timer1 period match
•
•
•
01000 = Reserved
00111 = PWM Generator 4 primary trigger is selected
00110 = PWM Generator 3 primary trigger is selected
00101 = PWM Generator 2 primary trigger is selected
00100 = PWM Generator 1 primary trigger is selected
00011 = PWM Special Event Trigger is selected
00010 = Global software trigger is selected
00001 = Individual software trigger is selected
00000 = No conversion is enabled

Note 1: This register is only implemented on the dsPIC33FJ16GS502 and dsPIC33FJ16GS504 devices.

2: The trigger source must be set as global software trigger prior to setting this bit to '1'. If other conversions are in progress, conversion will be performed when the conversion resources are available.

20.0 HIGH-SPEED ANALOG COMPARATOR

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"High-Speed Analog Comparator"** (DS70296) in the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available on the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33F SMPS comparator module monitors current and/or voltage transients that may be too fast for the CPU and ADC to capture.

20.1 Features Overview

The SMPS comparator module contains the following major features:

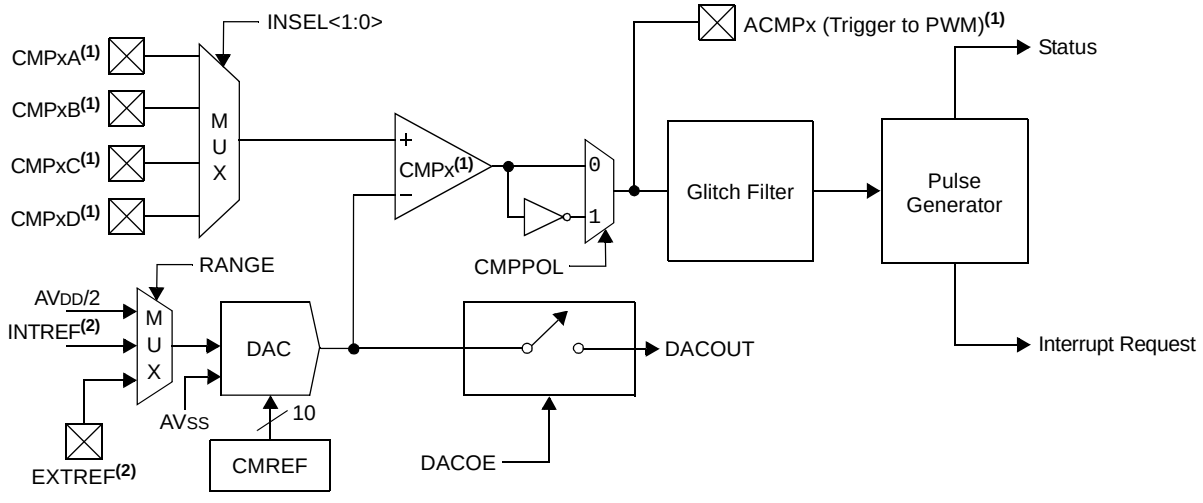
- 16 selectable comparator inputs
- Up to four analog comparators
- 10-bit DAC for each analog comparator
- Programmable output polarity
- Interrupt generation capability
- DACOUT pin to provide DAC output
- DAC has three ranges of operation:
  - $AV_{DD}/2$
  - Internal Reference (INTREF)
  - External Reference (EXTREF)
- ADC sample and convert trigger capability
- Disable capability reduces power consumption
- Functional support for PWM module:
  - PWM duty cycle control
  - PWM period control
  - PWM Fault detect

20.2 Module Description

Figure 20-1 shows a functional block diagram of one analog comparator from the SMPS comparator module. The analog comparator provides high-speed operation with a typical delay of 20 ns. The comparator has a typical offset voltage of ±5 mV. The negative input of the comparator is always connected to the DAC circuit. The positive input of the comparator is connected to an analog multiplexer that selects the desired source pin.

The analog comparator input pins are typically shared with pins used by the Analog-to-Digital Converter (ADC) module. Both the comparator and the ADC can use the same pins at the same time. This capability enables a user to measure an input voltage with the ADC and detect voltage transients with the comparator.

FIGURE 20-1: HIGH-SPEED ANALOG COMPARATOR MODULE BLOCK DIAGRAM



Note 1: x = 1, 2, 3 and 4.

2: For the INTREF and EXTREF values, refer to the DAC Module Specifications (Table 24-43) in **Section 24.0 "Electrical Characteristics"**.

21.0 SPECIAL FEATURES

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F/PIC24H Family Reference Manual"*. Please see the Microchip web site (www.microchip.com) for the latest *"dsPIC33F/PIC24H Family Reference Manual"* sections.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation
- Brown-out Reset (BOR)

21.1 Configuration Bits

dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 devices provide nonvolatile memory implementations for device Configuration bits. Refer to **"Device Configuration"** (DS70194) in the *"dsPIC33F/PIC24H Family Reference Manual"* for more information on this implementation.

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped starting at program memory location 0xF80000.

The individual Configuration bit descriptions for the Configuration registers are shown in Table 21-2.

Note that address, 0xF80000, is beyond the user program memory space. It belongs to the configuration memory space (0x800000-0xFFFFFF), which can only be accessed using Table Reads and Table Writes.

The device Configuration register map is shown in Table 21-1.

TABLE 21-1: DEVICE CONFIGURATION REGISTER MAP

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xF80000	FBS	—	—	—	—	BSS2	BSS1	BSS0	BWRP
0xF80002	Reserved	—	—	—	—	—	—	—	—
0xF80004	FGS	—	—	—	—	—	GSS1	GSS0	GWRP
0xF80006	FOSCSEL	IESO	—	—	—		FNOSC2	FNOSC1	FNOSC0
0xF80008	FOSC	FCKSM1	FCKSM0	IOL1WAY	—	—	OSCIOFNC	POSCMD1	POSCMD0
0xF8000A	FWDT	FWDTEN	WINDIS	—	WDTPRE	WDTPOST3	WDTPOST2	WDTPOST1	WDTPOST0
0xF8000C	FPOR	—	—	—	—	Reserved(2)	FPWRT2	FPWRT1	FPWRT0
0xF8000E	FICD	Reserved(1)		JTAGEN	—	—	—	ICS1	ICS0
0xF80010	FUID0	User Unit ID Byte 0							
0xF80012	FUID1	User Unit ID Byte 1							

Legend: — = unimplemented bit, read as '0'.

Note 1: These bits are reserved for use by development tools and must be programmed to '1'.

2: This bit reads the current programmed value.

NOTES:

25.0 HIGH-TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

Note:	Programming of the Flash memory is not allowed above +125°C.

The specifications between -40°C to +150°C are identical to those shown in **Section 24.0 "Electrical Characteristics"** for operation between -40°C to +125°C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter DC10 in **Section 24.0 "Electrical Characteristics"** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 high-temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings(1)

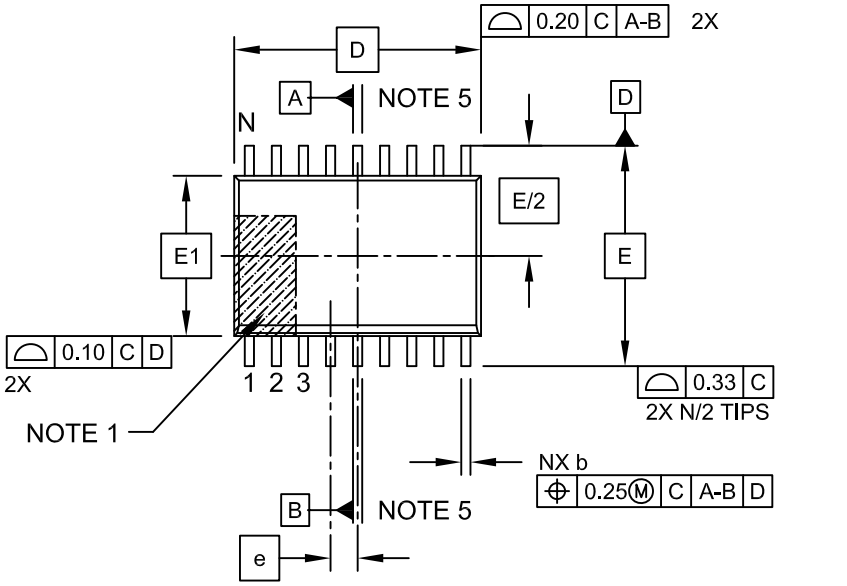
Ambient temperature under bias(3) ..... -40°C to +150°C
Storage temperature ..... -65°C to +160°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to V_{SS}(4) ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when V_{DD} < 3.0V(4) ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq$ 3.0V(4) ..... -0.3V to 5.6V
Maximum current out of V_{SS} pin ..... 60 mA
Maximum current into V_{DD} pin(2) ..... 60 mA
Maximum junction temperature ..... +155°C
Maximum current sourced/sunk by any 4x I/O pin ..... 4 mA
Maximum current sourced/sunk by any 8x I/O pin ..... 8 mA
Maximum current sourced/sunk by any 16x I/O pin ..... 16 mA
Maximum current sunk by all ports combined ..... 180 mA
Maximum current sourced by all ports combined(2) ..... 180 mA

Note 1:	Stresses above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.
2:	Maximum allowable current is a function of device maximum power dissipation (see Table 25-2).
3:	AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.
4:	Refer to the **"Pin Diagrams"** section for 5V tolerant pins.

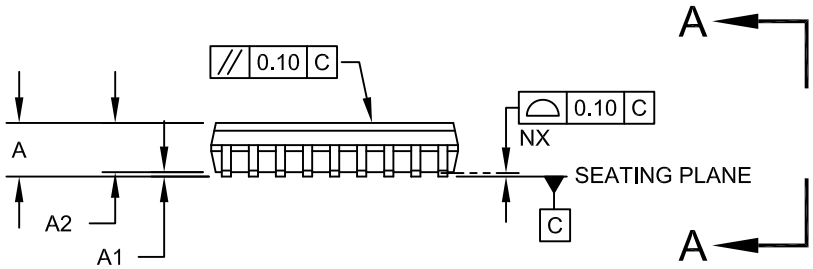
28.2 Package Details

18-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

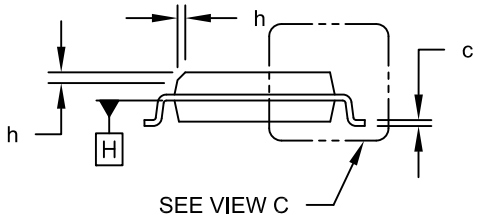
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

Microchip Technology Drawing C04-051C Sheet 1 of 2

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 24.0 "Electrical Characteristics"	Updated Typical values for Thermal Packaging Characteristics (see Table 24-3). Updated Min and Max values for Parameter DC12 (RAM Data Retention Voltage) and added Note 4 (see Table 24-4). Updated Characteristics for I/O Pin Input Specifications (see Table 24-9). Added ISOURCE to I/O Pin Output Specifications (see Table 24-10). Updated Program Memory values for Parameters 136, 137, and 138 (renamed to 136a, 137a, and 138a), added Parameters 136b, 137b, and 138b, and added Note 2 (see Table 24-12). Added Parameter OS42 (GM) to the External Clock Timing Requirements (see Table 24-16). Updated Conditions for symbol TPDLY (Tap Delay) and added symbol ACLK (PWM Input Clock) to the High-Speed PWM Module Timing Requirements (see Table 24-29). Updated Parameters AD01 and AD02 in the 10-bit High-Speed Analog-to-Digital Module Specifications (see Table 24-36). Updated Parameters AD50b, AD55b, and AD56b, and removed Parameters AD57b and AD60b from the 10-bit High-Speed Analog-to-Digital Module Timing Requirements (see Table 24-37).