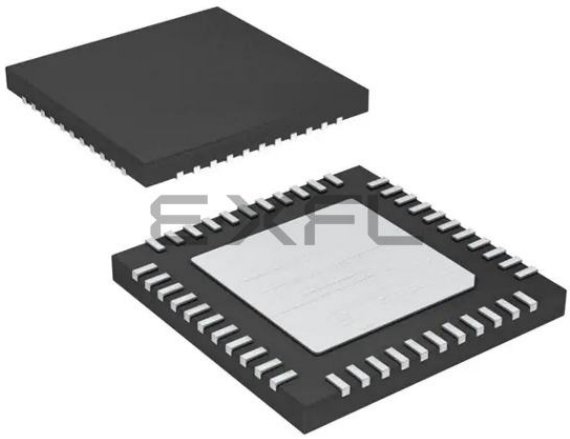
# Microchip Technology - DSPIC33FJ16GS504T-50I/ML Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

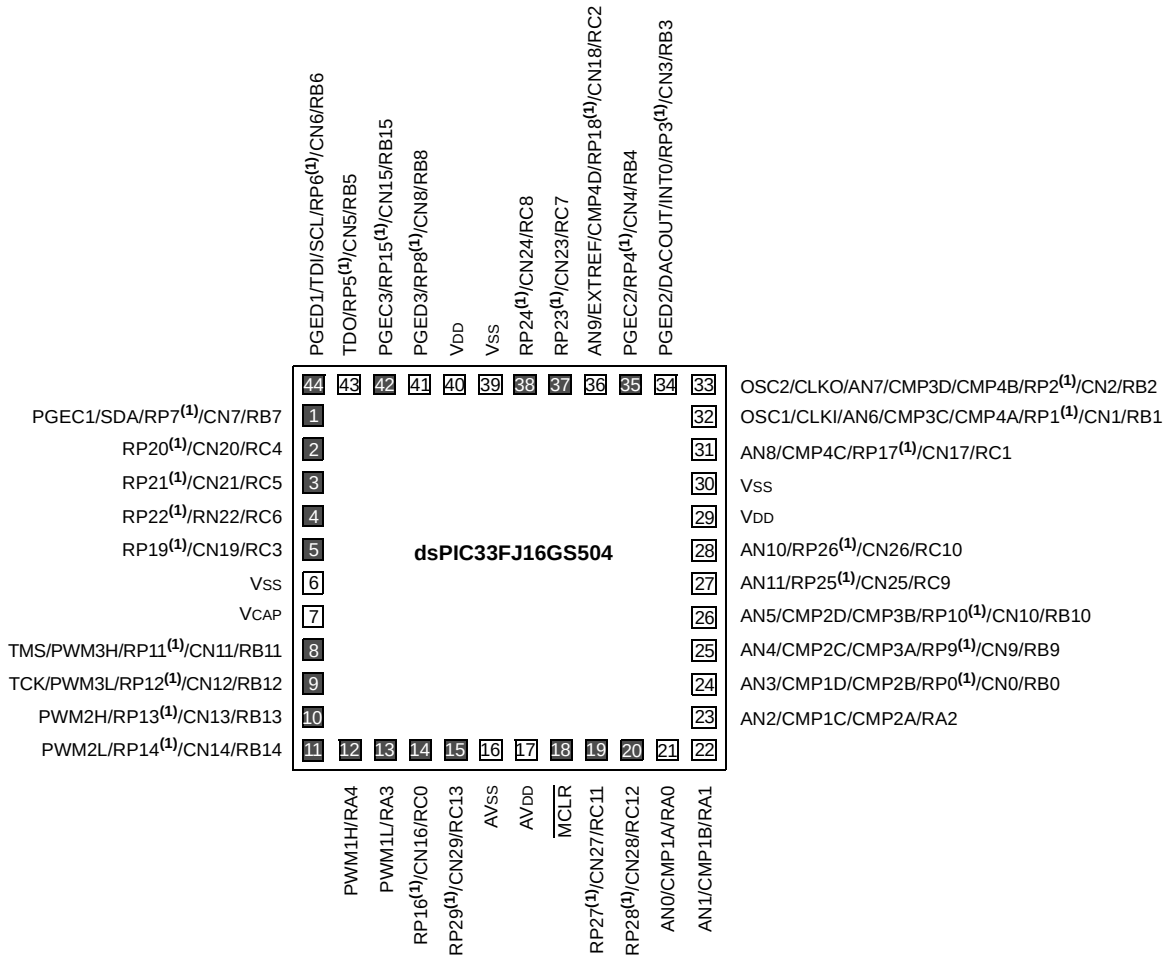
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 50 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 24x10b; D/A 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VQFN Exposed Pad |
| Supplier Device Package | 44-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj16gs504t-50i-ml |

## Pin Diagrams (Continued)

**44-Pin VTLA(2)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.

**2:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**TABLE 4-33: PERIPHERAL PIN SELECT INPUT REGISTER MAP**

| File Name | SFR Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 0680 | — | — | INT1R5 | INT1R4 | INT1R3 | INT1R2 | INT1R1 | INT1R0 | — | — | — | — | — | — | — | — | 3F00 |
| RPINR1 | 0682 | — | — | — | — | — | — | — | — | — | — | INT2R5 | INT2R4 | INT2R3 | INT2R2 | INT2R1 | INT2R0 | 003F |
| RPINR2 | 0684 | — | — | T1CKR5 | T1CKR4 | T1CKR3 | T1CKR2 | T1CKR1 | T1CKR0 | — | — | — | — | — | — | — | — | 0000 |
| RPINR3 | 0686 | — | — | T3CKR5 | T3CKR4 | T3CKR3 | T3CKR2 | T3CKR1 | T3CKR0 | — | — | T2CKR5 | T2CKR4 | T2CKR3 | T2CKR2 | T2CKR1 | T2CKR0 | 3F3F |
| RPINR7 | 068E | — | — | IC2R5 | IC2R4 | IC2R3 | IC2R2 | IC2R1 | IC2R0 | — | — | IC1R5 | IC1R4 | IC1R3 | IC1R2 | IC1R1 | IC1R0 | 3F3F |
| RPINR11 | 0696 | — | — | — | — | — | — | — | — | — | — | OCFAR5 | OCFAR4 | OCFAR3 | OCFAR2 | OCFAR1 | OCFAR0 | 3F3F |
| RPINR18 | 06A4 | — | — | U1CTSR5 | U1CTSR4 | U1CTSR3 | U1CTSR2 | U1CTSR1 | U1CTSR0 | — | — | U1RXR5 | U1RXR4 | U1RXR3 | U1RXR2 | U1RXR1 | U1RXR0 | 003F |
| RPINR20 | 06A8 | — | — | SCK1R5 | SCK1R4 | SCK1R3 | SCK1R2 | SCK1R1 | SCK1R0 | — | — | SDI1R5 | SDI1R4 | SDI1R3 | SDI1R2 | SDI1R1 | SDI1R0 | 3F3F |
| RPINR21 | 06AA | — | — | — | — | — | — | — | — | — | — | SS1R5 | SS1R54 | SS1R3 | SS1R2 | SS1R1 | SS1R0 | 0000 |
| RPINR29 | 06BA | — | — | FLT1R5 | FLT1R4 | FLT1R3 | FLT1R2 | FLT1R1 | FLT1R0 | — | — | — | — | — | — | — | — | 3F00 |
| RPINR30 | 06BC | — | — | FLT3R5 | FLT3R4 | FLT3R3 | FLT3R2 | FLT3R1 | FLT3R0 | — | — | FLT2R5 | FLT2R4 | FLT2R3 | FLT2R2 | FLT2R1 | FLT2R0 | 3F3F |
| RPINR31 | 06BE | — | — | FLT5R5 | FLT5R4 | FLT5R3 | FLT5R2 | FLT5R1 | FLT5R0 | — | — | FLT4R5 | FLT4R4 | FLT4R3 | FLT4R2 | FLT4R1 | FLT4R0 | 3F3F |
| RPINR32 | 06C0 | — | — | FLT7R5 | FLT7R4 | FLT7R3 | FLT7R2 | FLT7R1 | FLT7R0 | — | — | FLT6R5 | FLT6R4 | FLT6R3 | FLT6R2 | FLT6R1 | FLT6R0 | 3F3F |
| RPINR33 | 06C2 | — | — | SYNCI1R5 | SYNCI1R4 | SYNCI1R3 | SYNCI1R2 | SYNCI1R1 | SYNCI1R0 | — | — | FLT8R5 | FLT8R4 | FLT8R3 | FLT8R2 | FLT8R1 | FLT8R0 | 3F3F |
| RPINR34 | 06C4 | — | — | — | — | — | — | — | — | — | — | SYNCI2R5 | SYNCI2R4 | SYNCI2R3 | SYNCI2R2 | SYNCI2R1 | SYNCI2R0 | 3F3F |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-34: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33FJ06GS101**

| File Name | SFR Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPOR0 | 06D0 | — | — | RP1R5 | RP1R4 | RP1R3 | RP1R2 | RP1R1 | RP1R0 | — | — | RP0R5 | RP0R4 | RP0R3 | RP0R2 | RP0R1 | RP0R0 | 0000 |
| RPOR1 | 06D2 | — | — | RP3R5 | RP3R4 | RP3R3 | RP3R2 | RP3R1 | RP3R0 | — | — | RP2R5 | RP2R4 | RP2R3 | RP2R2 | RP2R1 | RP2R0 | 0000 |
| RPOR2 | 06D4 | — | — | RP5R5 | RP5R4 | RP5R3 | RP5R2 | RP5R1 | RP5R0 | — | — | RP4R5 | RP4R4 | RP4R3 | RP4R2 | RP4R1 | RP4R0 | 0000 |
| RPOR3 | 06D6 | — | — | RP7R5 | RP7R4 | RP7R3 | RP7R2 | RP7R1 | RP7R0 | — | — | RP6R5 | RP6R4 | RP6R3 | RP6R2 | RP6R1 | RP6R0 | 0000 |
| RPOR16 | 06F0 | — | — | RP33R5 | RP33R4 | RP33R3 | RP33R2 | RP33R1 | RP33R0 | — | — | RP32R5 | RP32R4 | RP32R3 | RP32R2 | RP32R1 | RP32R0 | 0000 |
| RPOR17 | 06F2 | — | — | RP35R5 | RP35R4 | RP35R3 | RP35R2 | RP35R1 | RP35R0 | — | — | RP34R5 | RP34R4 | RP34R3 | RP34R2 | RP34R1 | RP34R0 | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 5-2: NVMKEY: NONVOLATILE MEMORY KEY REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
|---|---|---|---|---|---|---|---|
| NVMKEY<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **NVMKEY<7:0>:** Nonvolatile Memory Key bits (write-only)

**REGISTER 7-9: IFS5: INTERRUPT FLAG STATUS REGISTER 5**

| R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| PWM2IF | PWM1IF | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **PWM2IF:** PWM2 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 14 **PWM1IF:** PWM1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13-0 **Unimplemented:** Read as ‘0’

**REGISTER 7-11: IFS7: INTERRUPT FLAG STATUS REGISTER 7**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | ADCP6IF | ADCP5IF | ADCP4IF | ADCP3IF | ADCP2IF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4 **ADCP6IF:** ADC Pair 6 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **ADCP5IF:** ADC Pair 5 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **ADCP4IF:** ADC Pair 4 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **ADCP3IF:** ADC Pair 3 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **ADCP2IF:** ADC Pair 2 Conversion Done Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

**REGISTER 8-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER(1)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | TUN<5:0>(2) | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits(2)

011111 = Center frequency + 11.6% (8.2268 MHz)
011110 = Center frequency + 11.2% (8.1992 MHz)
•
•
•
000001 = Center frequency + 0.375% (7.3976 MHz)
000000 = Center frequency (7.37 MHz nominal)
111111 = Center frequency – 0.375% (7.2594 MHz)
•
•
•
100001 = Center frequency – 11.6% (6.5132 MHz)
000000 = Center frequency – 12% (6.4856 MHz)

**Note 1:** This register is reset only on a Power-on Reset (POR).

**2:** OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step-size is an approximation and is neither characterized nor tested.

**REGISTER 9-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | IC2MD | IC1MD |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | OC2MD | OC1MD |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-10 **Unimplemented:** Read as ‘0’

bit 9 **IC2MD**: Input Capture 2 Module Disable bit
1 = Input Capture 2 module is disabled
0 = Input Capture 2 module is enabled

bit 8 **IC1MD**: Input Capture 1 Module Disable bit
1 = Input Capture 1 module is disabled
0 = Input Capture 1 module is enabled

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **OC2MD**: Output Compare 2 Module Disable bit
1 = Output Compare 2 module is disabled
0 = Output Compare 2 module is enabled

bit 0 **OC1MD**: Output Compare 1 Module Disable bit
1 = Output Compare 1 module is disabled
0 = Output Compare 1 module is enabled

**REGISTER 9-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | PWM4MD | PWM3MD | PWM2MD | PWM1MD |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11 **PWM4MD**: PWM Generator 4 Module Disable bit
1 = PWM Generator 4 module is disabled
0 = PWM Generator 4 module is enabled

bit 10 **PWM3MD**: PWM Generator 3 Module Disable bit
1 = PWM Generator 3 module is disabled
0 = PWM Generator 3 module is enabled

bit 9 **PWM2MD**: PWM Generator 2 Module Disable bit
1 = PWM Generator 2 module is disabled
0 = PWM Generator 2 module is enabled

bit 8 **PWM1MD**: PWM Generator 1 Module Disable bit
1 = PWM Generator 1 module is disabled
0 = PWM Generator 1 module is enabled

bit 7-0 **Unimplemented:** Read as ‘0’

**REGISTER 10-9: RPINR29: PERIPHERAL PIN SELECT INPUT REGISTER 29**

| U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | FLT1R5 | FLT1R4 | FLT1R3 | FLT1R2 | FLT1R1 | FLT1R0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **FLT1R<5:0>:** Assign PWM Fault Input 1 (FLT1) to the Corresponding RPn Pin bits

111111 = Input tied to Vss
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

bit 7-0 **Unimplemented:** Read as ‘0’

**REGISTER 12-2: TyCON: TIMERy CONTROL REGISTER (y = 3)**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TON(2) | — | TSIDL(1) | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE(2) | TCKPS1(2) | TCKPS0(2) | — | — | TCS(2) | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timery On bit(2)
1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **TSIDL:** Timery Stop in Idle Mode bit(1)
1 = Discontinues timer operation when device enters Idle mode
0 = Continues timer operation in Idle mode

bit 12-7 **Unimplemented:** Read as ‘0’

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit(2)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timery Input Clock Prescale Select bits(2)
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1 **TCS:** Timery Clock Source Select bit(2)
1 = External clock from TxCK pin
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as ‘0’

**Note 1:** When 32-bit timer operation is enabled (T32 = 1) in the Timerx Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

**2:** When the 32-bit timer operation is enabled (T32 = 1) in the Timerx Control (TxCON<3>) register, these bits have no effect.

## 14.1 Output Compare Modes

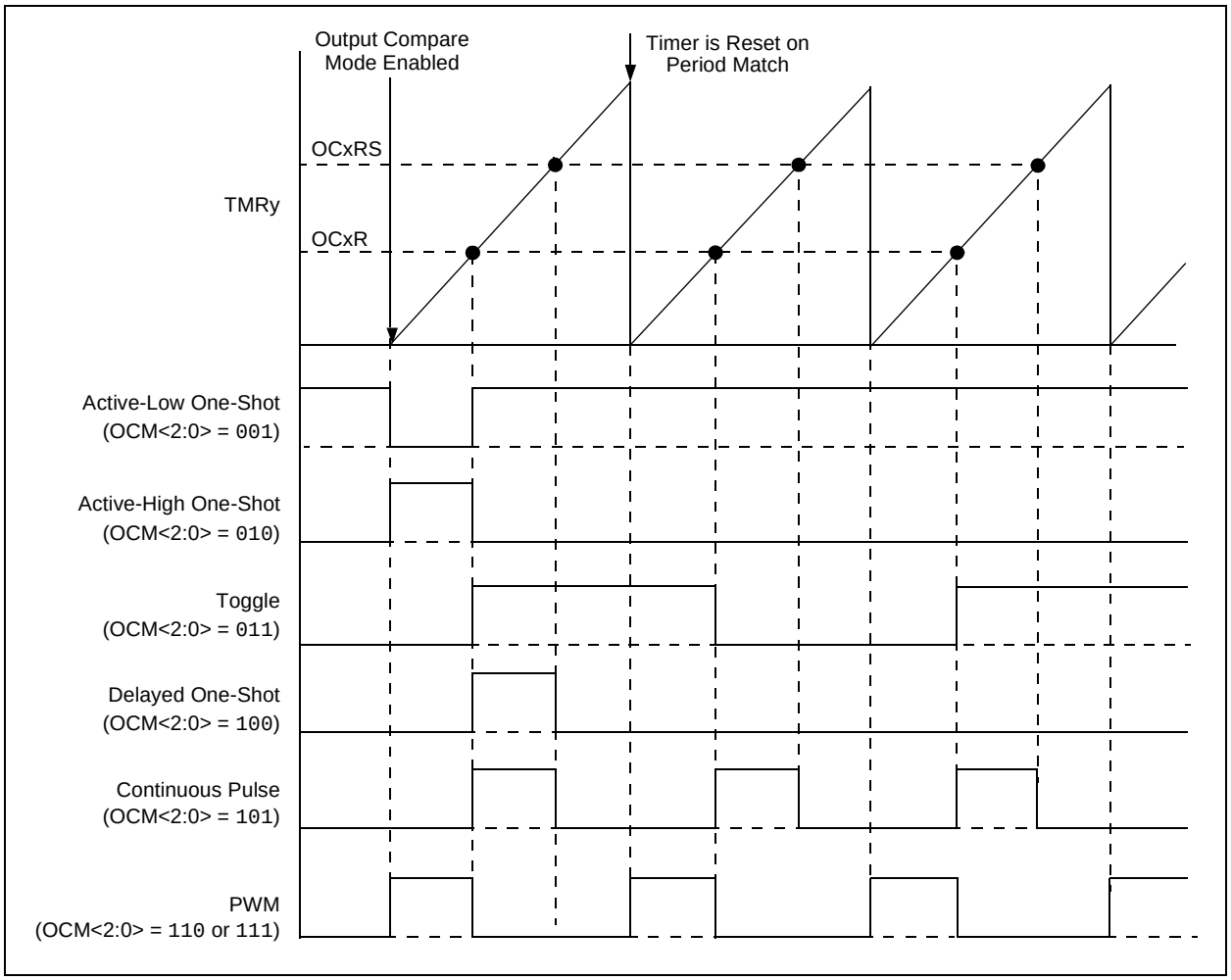
Configure the Output Compare modes by setting the appropriate Output Compare Mode (OCM<2:0>) bits in the Output Compare Control (OCxCON<2:0>) register. Table 14-1 lists the different bit settings for the Output Compare modes. Figure 14-2 illustrates the output compare operation for various modes. The user application must disable the associated timer when writing to the Output Compare Control registers to avoid malfunctions.

| **Note:** | Refer to **"Output Compare"** (DS70209) in the *"dsPIC33F/PIC24H Family Reference Manual"* for OCxR and OCxRS register restrictions. |
|---|---|

**TABLE 14-1: OUTPUT COMPARE MODES**

| OCM<2:0> | Mode | OCx Pin Initial State | OCx Interrupt Generation |
|---|---|---|---|
| 111 | PWM with Fault Protection | '0', if OCxR is zero<br>'1', if OCxR is non-zero | OCFA falling edge for OC1 to OC4 |
| 110 | PWM without Fault Protection | '0', if OCxR is zero<br>'1', if OCxR is non-zero | No interrupt |
| 101 | Continuous Pulse | 0 | OCx falling edge |
| 100 | Delayed One-Shot | 0 | OCx falling edge |
| 011 | Toggle | Current output is maintained | OCx rising and falling edge |
| 010 | Active-High One-Shot | 1 | OCx falling edge |
| 001 | Active-Low One-Shot | 0 | OCx rising edge |
| 000 | Module Disabled | Controlled by GPIO register | — |

**FIGURE 14-2: OUTPUT COMPARE OPERATION**



**REGISTER 15-2: PTCON2: PWM CLOCK DIVIDER SELECT REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | PCLKDIV<2:0>(1) | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **PCLKDIV<2:0>:** PWM Input Clock Prescaler (Divider) Select bits(1)

111 = Reserved
110 = Divide-by-64, maximum PWM timing resolution
101 = Divide-by-32, maximum PWM timing resolution
100 = Divide-by-16, maximum PWM timing resolution
011 = Divide-by-8, maximum PWM timing resolution
010 = Divide-by-4, maximum PWM timing resolution
001 = Divide-by-2, maximum PWM timing resolution
000 = Divide-by-1, maximum PWM timing resolution (power-on default)

**Note 1:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

**REGISTER 15-3: PTPER: PWM MASTER TIME BASE REGISTER(1)**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| PTPER <15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTPER <7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **PTPER<15:0>:** PWM Master Time Base (PMTMR) Period Value bits

**Note 1:** The minimum value that can be loaded into the PTPER register is 0x0010 and the maximum value is 0xFFF8.

**REGISTER 15-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER(1,2)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PHASEx<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PHASEx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **PHASEx<15:0>:** PWM Phase-Shift Value or Independent Time Base Period for this PWM Generator bits

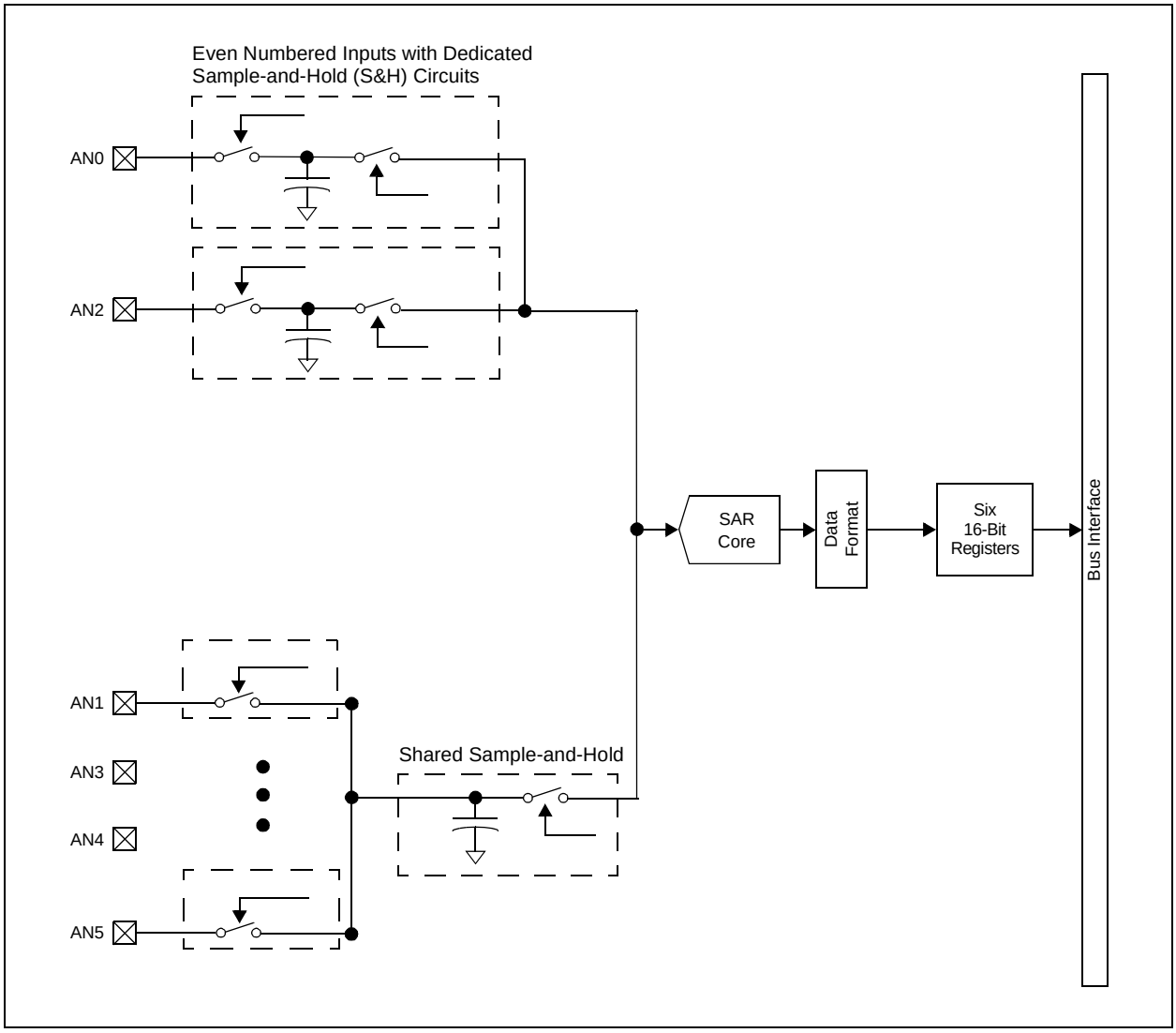
**Note 1:** If PWMCONx<ITB> = 0, the following applies based on the mode of operation:

- Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10); PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs
- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11); PHASEx<15:0> = Phase-shift value for PWMxL only

**2:** If PWMCONx<ITB> = 1, the following applies based on the mode of operation:

- Complementary, Redundant, and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10); PHASEx<15:0> = Independent Time Base period value for PWMxH and PWMxL
- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11); PHASEx<15:0> = Independent Time Base period value for PWMxL only
- The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0008, while the maximum pulse width generated corresponds to a value of Period – 0x0008.

**FIGURE 19-2: ADC BLOCK DIAGRAM FOR dsPIC33FJ06GS102 DEVICES WITH ONE SAR**



**NOTES:**

**TABLE 24-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| DI60a | IICL | **Input Low Injection Current** | 0 | — | -5(5,8) | mA | All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP and RB5 |
| DI60b | IICH | **Input High Injection Current** | 0 | — | +5(6,7,8) | mA | All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB5 and digital 5V-tolerant designated pins |
| DI60c | ∑ IICT | **Total Input Injection Current (sum of all I/O and control pins)** | -20(9) | — | +20(9) | mA | Absolute instantaneous sum of all ± input injection currents from all I/O pins ( \| IICL + \| IICH \| ) ≤ ∑ IICT |

**Note 1:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as current sourced by the pin.

**4:** See **"Pin Diagrams"** for the list of 5V tolerant I/O pins.

**5:** VIL source < (VSS – 0.3). Characterized but not tested.

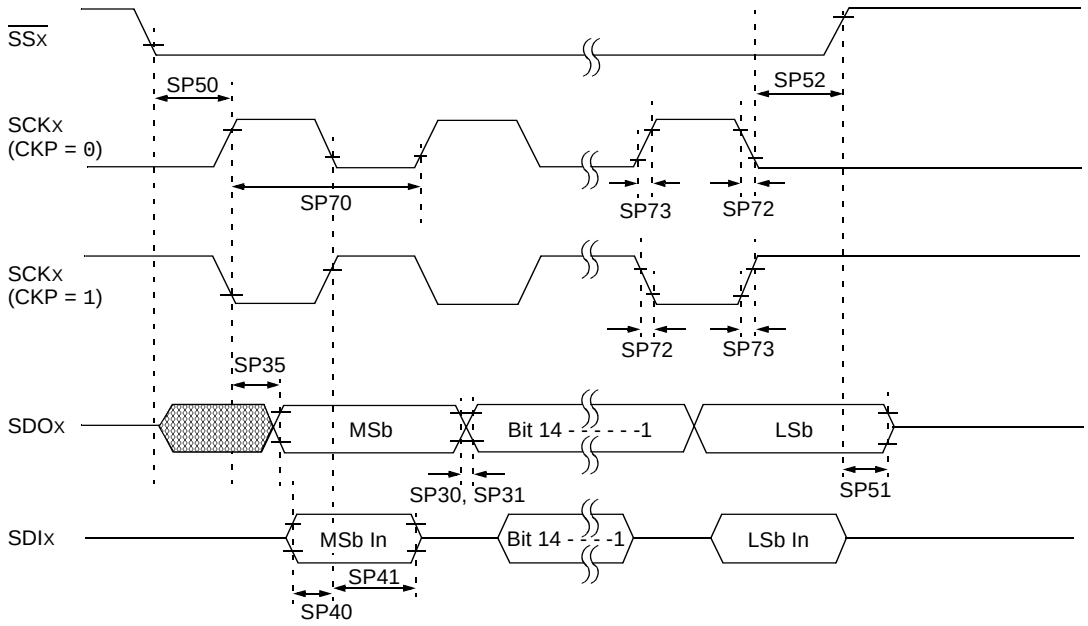
**6:** Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

**7:** Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

**8:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

**9:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

**FIGURE 24-17: SPIx SLAVE MODE (FULL-DUPLEX CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 24-1 for load conditions.

**TABLE 24-40: 10-BIT HIGH-SPEED ADC MODULE SPECIFICATIONS**

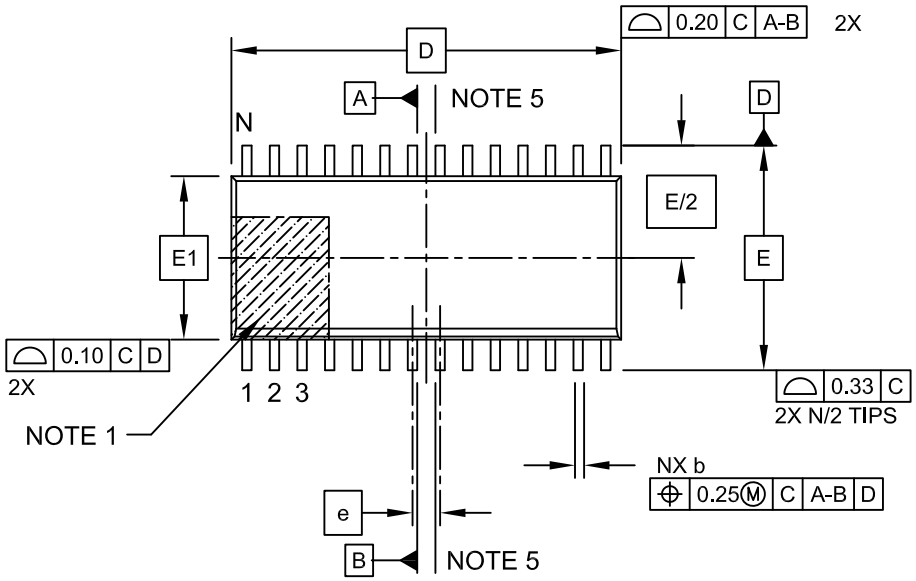
| AC CHARACTERISTICS | | | Standard Operating Conditions (see Note 2): 3.0V and 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Device Supply** | | | | | | | |
| AD01 | AVDD | Module VDD Supply | — | — | — | — | AVDD is internally connected to VDD; see Parameter DC10 in Table 24-4 |
| AD02 | AVSS | Module VSS Supply | — | — | — | — | AVSS is internally connected to VSS |
| **Analog Input** | | | | | | | |
| AD10 | VINH-VINL | Full-Scale Input Span | VSS | — | VDD | V | |
| AD11 | VIN | Absolute Input Voltage | AVSS | — | AVDD | V | |
| AD12 | IAD | Operating Current | — | 8 | — | mA | |
| AD13 | — | Leakage Current | — | ±0.6 | — | μA | VINL = AVSS = 0V, AVDD = 3.3V, Source Impedance = 100Ω |
| AD17 | RIN | Recommended Impedance Of Analog Voltage Source | — | — | 100 | Ω | |
| **DC Accuracy @ 1.5 Msps** | | | | | | | |
| AD20A | Nr | Resolution | 10 Data Bits | | | | |
| AD21A | INL | Integral Nonlinearity | -0.5 | -0.3/+0.5 | +1.2 | LSb | |
| AD22A | DNL | Differential Nonlinearity | -0.9 | ±0.6 | +0.9 | LSb | |
| AD23A | GERR | Gain Error | 13 | 15 | 22 | LSb | |
| AD24A | EOFF | Offset Error | 6 | 7 | 8 | LSb | |
| AD25A | — | Monotonicity(1) | — | — | — | — | Guaranteed |
| **DC Accuracy @ 1.7 Msps** | | | | | | | |
| AD20B | Nr | Resolution | 10 Data Bits | | | | |
| AD21B | INL | Integral Nonlinearity | -0.5 | -0.4/+1.1 | +1.8 | LSb | |
| AD22B | DNL | Differential Nonlinearity | -1.0 | ±1.0 | +1.5 | LSb | |
| AD23B | GERR | Gain Error | 13 | 15 | 22 | LSb | |
| AD24B | EOFF | Offset Error | 6 | 7 | 8 | LSb | |
| AD25B | — | Monotonicity(1) | — | — | — | — | Guaranteed |
| **DC Accuracy @ 2.0 Msps** | | | | | | | |
| AD20C | Nr | Resolution | 10 Data Bits | | | | |
| AD21C | INL | Integral Nonlinearity | -0.8 | -0.5/+1.8 | +2.8 | LSb | |
| AD22C | DNL | Differential Nonlinearity | -1.0 | -1.0/+1.8 | +2.8 | LSb | |
| AD23C | GERR | Gain Error | 14 | 16 | 23 | LSb | |
| AD24C | EOFF | Offset Error | 6 | 7 | 8 | LSb | |
| AD25C | — | Monotonicity(1) | — | — | — | — | Guaranteed |
| **Dynamic Performance** | | | | | | | |
| AD30 | THD | Total Harmonic Distortion | — | -73 | — | dB | |
| AD31 | SINAD | Signal to Noise and Distortion | — | 58 | — | dB | |
| AD32 | SFDR | Spurious Free Dynamic Range | — | -73 | — | dB | |
| AD33 | FNYQ | Input Signal Bandwidth | — | — | 1 | MHz | |
| AD34 | ENOB | Effective Number of Bits | — | 9.4 | — | bits | |

**Note 1:** The Analog-to-Digital conversion result never decreases with an increase in input voltage, and has no missing codes.

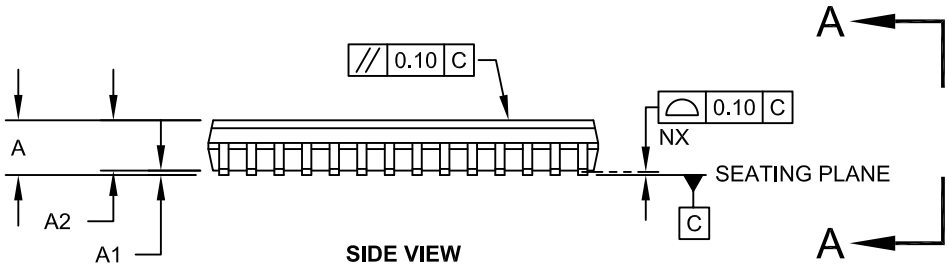
**2:** Module is functional at VBOR < VDD < VDDMIN, but with degraded performance. Module functionality is tested but not characterized.

### 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

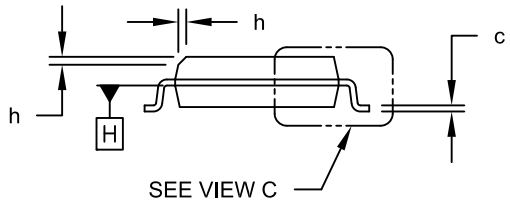
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**TOP VIEW**




**SIDE VIEW**

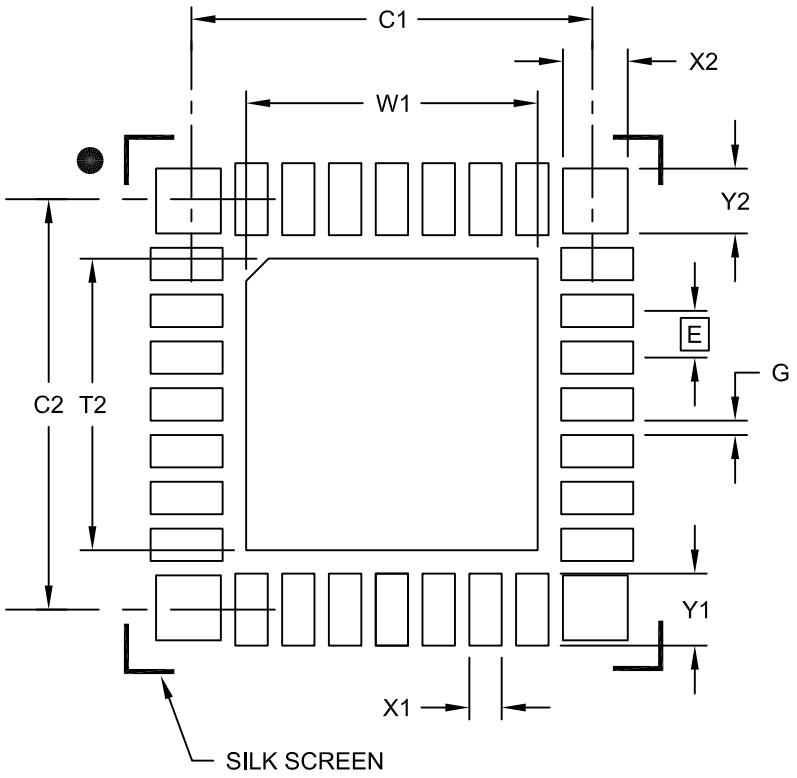



**VIEW A-A**

Microchip Technology Drawing C04-052C Sheet 1 of 2

### 28-Lead Plastic Quad Flat, No Lead Package (MX) - 6x6 mm Body [UQFN] With 0.60mm Contact Length And Corner Anchors

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Optional Center Pad Width | W1 | | | 4.05 |
| Optional Center Pad Length | T2 | | | 4.05 |
| Contact Pad Spacing | C1 | | 5.70 | |
| Contact Pad Spacing | C2 | | 5.70 | |
| Contact Pad Width (X28) | X1 | | | 0.45 |
| Contact Pad Length (X28) | Y1 | | | 1.00 |
| Corner Pad Width (X4) | X2 | | | 0.90 |
| Corner Pad Length (X4) | Y2 | | | 0.90 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2209B