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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9bf166npmc-g-jne2

[UART]

- Full-duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control : Automatically control the transmission by CTS/RTS (only ch.4)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[CSIO]

- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detect function available
- Serial chip select function (ch.6 and ch.7 only)
- Supports high-speed SPI (ch.4 and ch.6 only)
- Data length 5 to 16-bit

[LIN]

- LIN protocol Rev.2.1 supported
- Full-duplex double buffer
- Master/Slave mode supported
- LIN break field generation (can change to 13 to 16-bit length)
- LIN break delimiter generation (can change to 1 to 4-bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[I^2C]

- Standard-mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported
- Fast-mode Plus (Fm+) (Max 1000 kbps, only for ch.3 = ch.A and ch.7 = ch.B) supported

DMA Controller (8 channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System data Transfer Controller) (128 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor system and, following the specified contents of the Descriptor which has already been constructed on the memory, can access directly the memory /peripheral device and performs the data transfer operation.

It supports the software activation, the hardware activation and the chain activation functions.

A/D Converter (Max 24 channels)

[12-bit A/D Converter]

- Successive Approximation type
- Built-in 3 units
- Conversion time: 0.5µs @ 5V
- Priority conversion available (priority at 2levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16steps, for Priority conversion: 4steps)

DA converter (Max 2 channels)

- R-2R type
- 12-bit resolution

Base Timer (Max 8 channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 100 high-speed general-purpose I/O ports @ 120pin Package
- Some pin is 5V tolerant I/O.
- See “Pin Description” and “I/O Circuit Type” for the corresponding pins.

Multi-function Timer (Max 2 units)

The Multi-function timer is composed of the following blocks.

Minimum resolution : 6.25 ns

- 16-bit free-run timer × 3ch./unit
- Input capture × 4ch./unit
- Output compare × 6ch./unit
- A/D activation compare × 6ch./unit
- Waveform generator × 3ch./unit
- 16-bit PPG timer × 3ch./unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Real-time clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- Interrupt function with specifying date and time (Year/Month/Day/Hour/Minute) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Quadrature Position/Revolution Counter (QPRC) (Max 2 channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (= Reload)
- One-shot

Watch Counter

The Watch counter is used for wake up from the low-power consumption mode. It is possible to select the main clock, sub clock, built-in high-speed CR clock or built-in low-speed CR clock as the clock source.

Interval timer: up to 64s (Max) @ Sub Clock : 32.768 kHz

External Interrupt Controller Unit

- External interrupt input pin: Max 16 pins
- Include one non-maskable interrupt (NMI)

Watchdog Timer (2 channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

"Hardware" watchdog timer is clocked by low-speed internal CR oscillator. Therefore, "Hardware" watchdog is active in any power saving mode except STOP.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

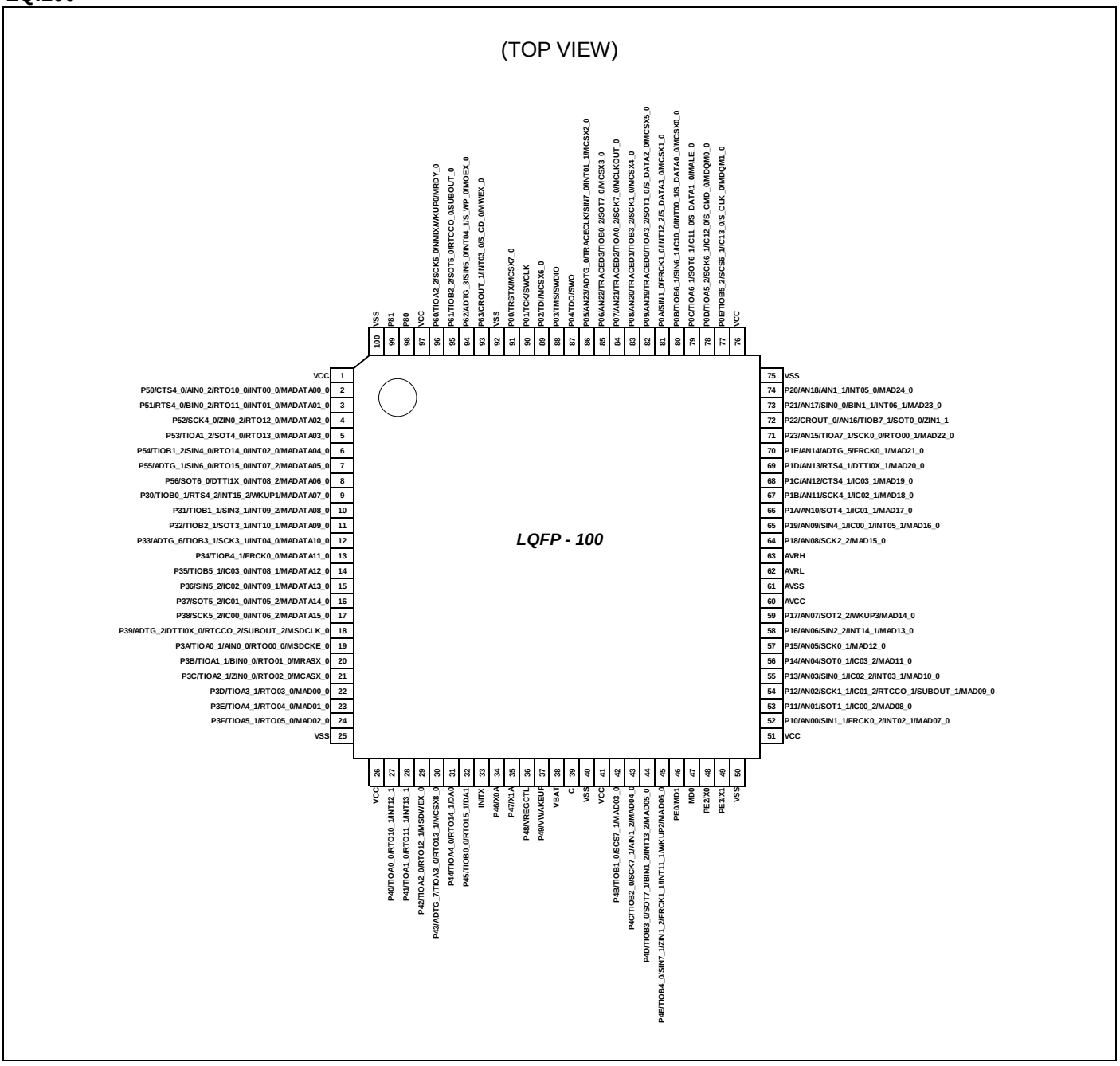
- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

SD Card Interface

It is possible to use the SD card that conforms to the following standards.

- Part 1 Physical Layer Specification version 3.01
- Part E1 SDIO Specification version 3.00
- Part A2 SD Host Controller Standard Specification version 3.00
- 1-bit or 4-bit data bus

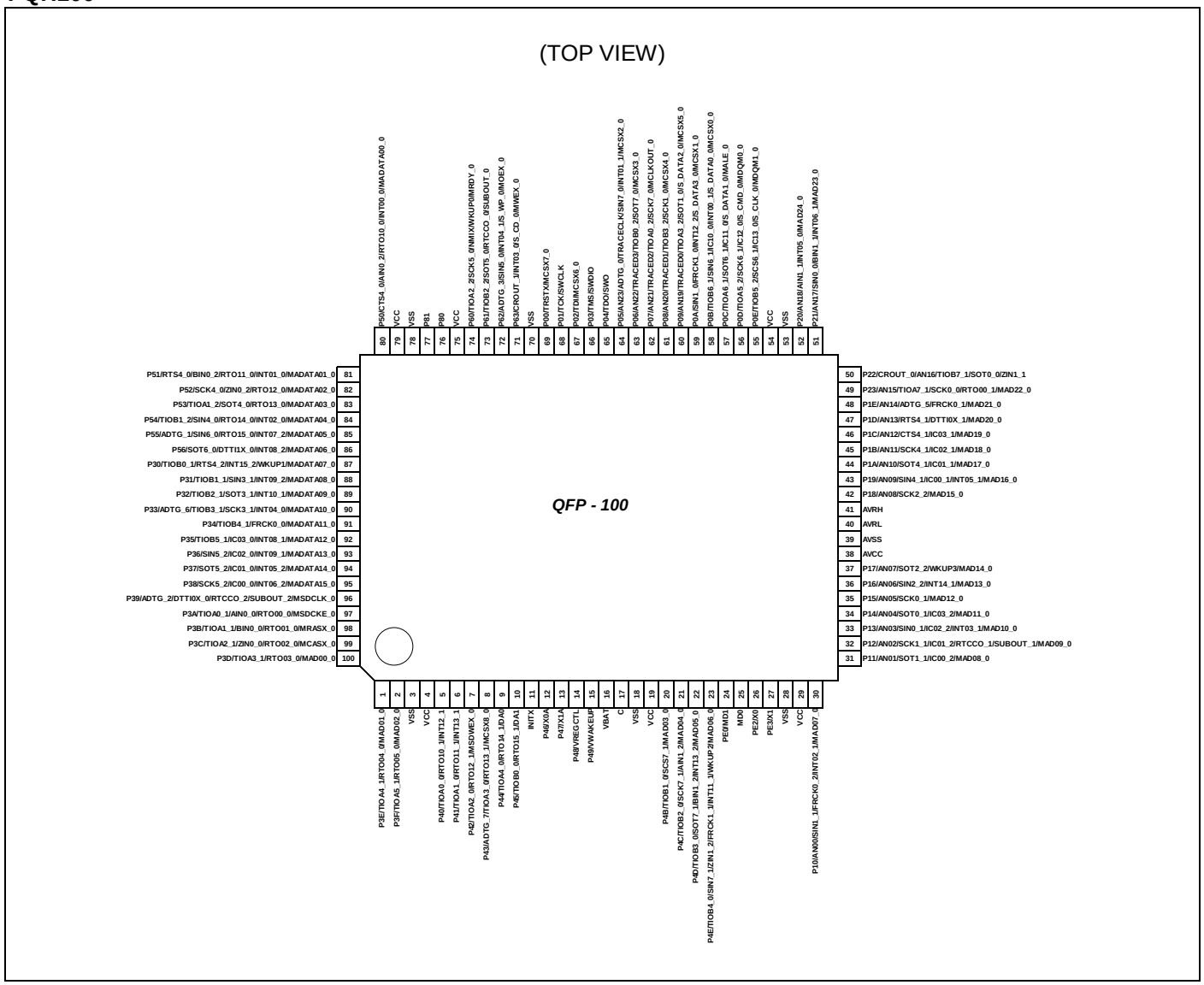
LQI100



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

PQH100



Note:

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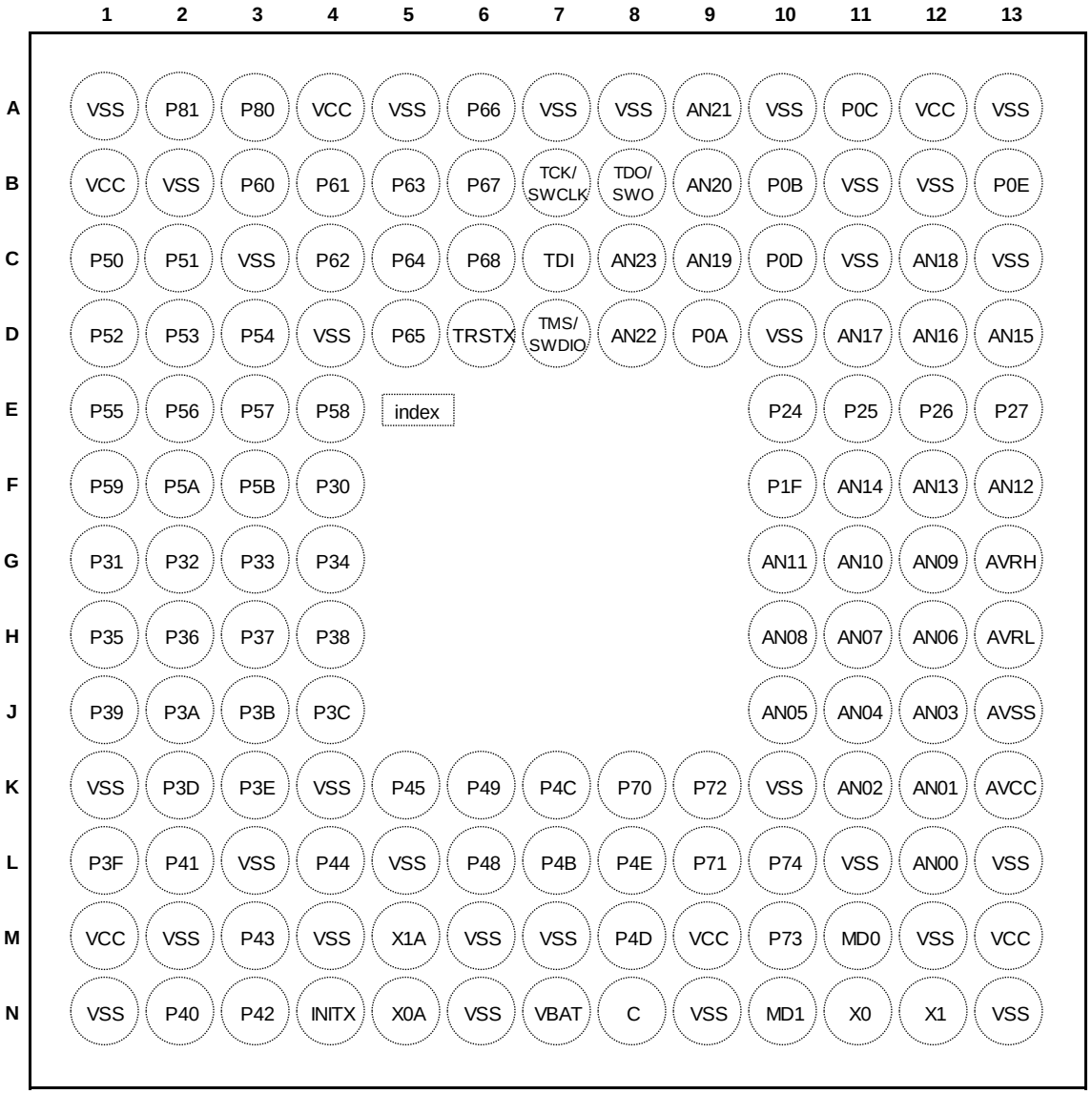
LDC144

(TOP VIEW)



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

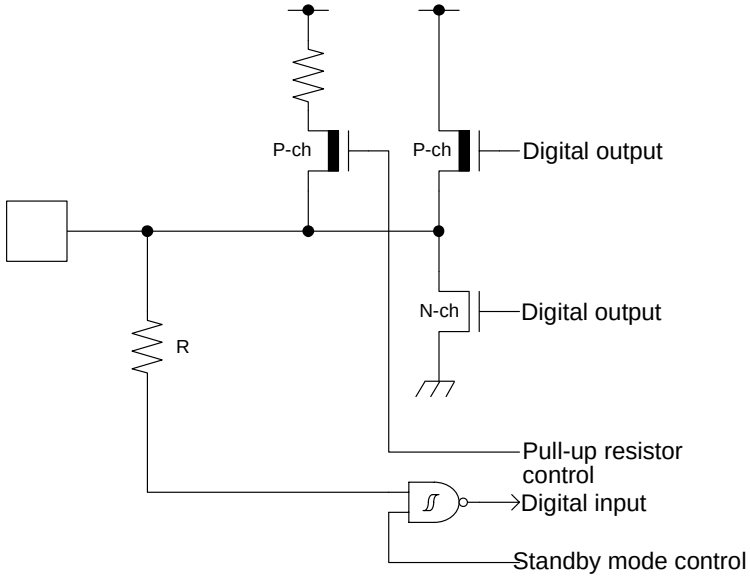
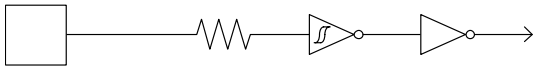
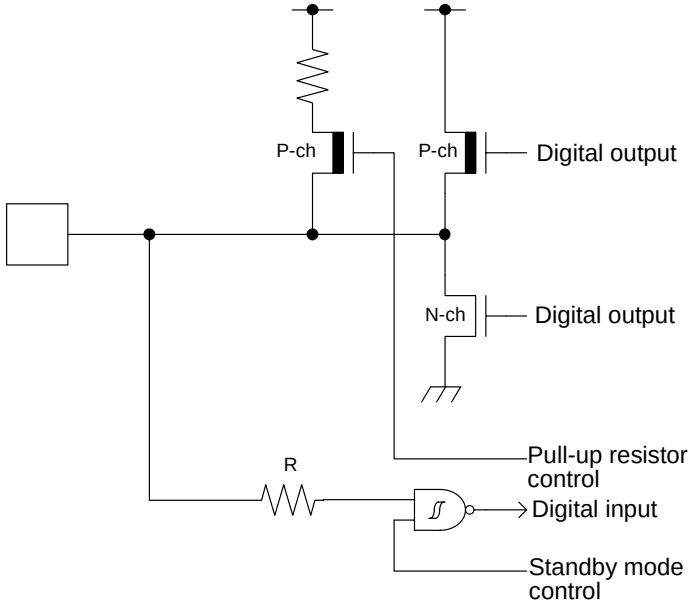
Pin function	Pin name	Function description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
ADC	ADTG_0	A/D converter external trigger input pin	101	86	-	64	C8	C8
	ADTG_1		7	7	7	85	E1	E1
	ADTG_2		23	18	13	96	J1	J1
	ADTG_3		114	94	74	72	B5	C4
	ADTG_4		81	-	-	-	-	F10
	ADTG_5		80	70	-	48	E11	F11
	ADTG_6		17	12	12	90	F3	G3
	ADTG_7		35	30	-	8	L3	M3
	ADTG_8		110	-	-	-	-	A6
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	62	52	41	30	L13	L12
	AN01		63	53	42	31	L12	K12
	AN02		64	54	43	32	K13	K11
	AN03		65	55	44	33	K12	J12
	AN04		66	56	45	34	J13	J11
	AN05		67	57	46	35	J12	J10
	AN06		68	58	47	36	J11	H12
	AN07		69	59	48	37	H12	H11
	AN08		74	64	53	42	H11	H10
	AN09		75	65	54	43	G12	G12
	AN10		76	66	55	44	G11	G11
	AN11		77	67	56	45	F12	G10
	AN12		78	68	-	46	F11	F13
	AN13		79	69	-	47	E12	F12
	AN14		80	70	-	48	E11	F11
	AN15		86	71	57	49	D13	D13
	AN16		87	72	58	50	D12	D12
	AN17		88	73	59	51	C13	D11
	AN18		89	74	-	52	C12	C12
	AN19		97	82	67	60	B9	C9
	AN20		98	83	-	61	C9	B9
	AN21		99	84	-	62	A8	A9
	AN22		100	85	-	63	B8	D8
	AN23		101	86	-	64	C8	C8
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	32	27	-	5	N2	N2
	TIOA0_1		24	19	14	97	J2	J2
	TIOA0_2		99	84	-	62	A8	A9
	TIOB0_0	Base timer ch.0 TIOB pin	37	32	22	10	L5	K5
	TIOB0_1		14	9	9	87	E3	F4
	TIOB0_2		100	85	-	63	B8	D8
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	33	28	-	6	N3	L2
	TIOA1_1		25	20	15	98	J3	J3
	TIOA1_2		5	5	5	83	D1	D2
	TIOB1_0	Base timer ch.1 TIOB pin	47	42	32	20	L7	L7
	TIOB1_1		15	10	10	88	F1	G1
	TIOB1_2		6	6	6	84	D2	D3
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	34	29	-	7	M3	N3
	TIOA2_1		26	21	16	99	K1	J4
	TIOA2_2		116	96	76	74	B3	B3
	TIOB2_0	Base timer ch.2 TIOB pin	48	43	33	21	L8	K7
	TIOB2_1		16	11	11	89	F2	G2
	TIOB2_2		115	95	75	73	B4	B4

Pin function	Pin name	Function description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
External Bus	MAD00_0	External bus interface address bus	27	22	17	100	K2	K2
	MAD01_0		28	23	18	1	L1	K3
	MAD02_0		29	24	19	2	L2	L1
	MAD03_0		47	42	32	20	L7	L7
	MAD04_0		48	43	33	21	L8	K7
	MAD05_0		49	44	34	22	M9	M8
	MAD06_0		50	45	35	23	L9	L8
	MAD07_0		62	52	41	30	L13	L12
	MAD08_0		63	53	42	31	L12	K12
	MAD09_0		64	54	43	32	K13	K11
	MAD10_0		65	55	44	33	K12	J12
	MAD11_0		66	56	45	34	J13	J11
	MAD12_0		67	57	46	35	J12	J10
	MAD13_0		68	58	47	36	J11	H12
	MAD14_0		69	59	48	37	H12	H11
	MAD15_0		74	64	53	42	H11	H10
	MAD16_0		75	65	54	43	G12	G12
	MAD17_0		76	66	55	44	G11	G11
	MAD18_0		77	67	56	45	F12	G10
	MAD19_0		78	68	-	46	F11	F13
	MAD20_0		79	69	-	47	E12	F12
	MAD21_0		80	70	-	48	E11	F11
	MAD22_0		86	71	-	49	D13	D13
	MAD23_0		88	73	-	51	C13	D11
	MAD24_0		89	74	-	52	C12	C12

Pin function	Pin name	Function description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
GPIO	P30	General-purpose I/O port 3	14	9	9	87	E3	F4
	P31		15	10	10	88	F1	G1
	P32		16	11	11	89	F2	G2
	P33		17	12	12	90	F3	G3
	P34		18	13	-	91	G1	G4
	P35		19	14	-	92	G2	H1
	P36		20	15	-	93	G3	H2
	P37		21	16	-	94	H2	H3
	P38		22	17	-	95	H3	H4
	P39		23	18	13	96	J1	J1
	P3A		24	19	14	97	J2	J2
	P3B		25	20	15	98	J3	J3
	P3C		26	21	16	99	K1	J4
	P3D		27	22	17	100	K2	K2
	P3E		28	23	18	1	L1	K3
	P3F		29	24	19	2	L2	L1
	P40	General-purpose I/O port 4	32	27	-	5	N2	N2
	P41		33	28	-	6	N3	L2
	P42		34	29	-	7	M3	N3
	P43		35	30	-	8	L3	M3
	P44		36	31	21	9	M4	L4
	P45		37	32	22	10	L5	K5
	P46		39	34	24	12	N5	N5
	P47		40	35	25	13	N6	M5
	P48		41	36	26	14	L6	L6
	P49		42	37	27	15	M7	K6
	P4B		47	42	32	20	L7	L7
	P4C		48	43	33	21	L8	K7
	P4D		49	44	34	22	M9	M8
	P4E		50	45	35	23	L9	L8
	P50	General-purpose I/O port 5	2	2	2	80	C1	C1
	P51		3	3	3	81	C2	C2
	P52		4	4	4	82	C3	D1
	P53		5	5	5	83	D1	D2
	P54		6	6	6	84	D2	D3
	P55		7	7	7	85	E1	E1
	P56		8	8	8	86	E2	E2
	P57		9	-	-	-	-	E3
	P58		10	-	-	-	-	E4
	P59		11	-	-	-	-	F1
	P5A		12	-	-	-	-	F2
	P5B		13	-	-	-	-	F3

Pin function	Pin name	Function description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
GPIO	P60	General-purpose I/O port 6	116	96	76	74	B3	B3
	P61		115	95	75	73	B4	B4
	P62		114	94	74	72	B5	C4
	P63		113	93	73	71	C5	B5
	P64		112	-	-	-	-	C5
	P65		111	-	-	-	-	D5
	P66		110	-	-	-	-	A6
	P67		109	-	-	-	-	B6
	P68		108	-	-	-	-	C6
	P70	General-purpose I/O port 7	51	-	-	-	-	K8
	P71		52	-	-	-	-	L9
	P72		53	-	-	-	-	K9
	P73		54	-	-	-	-	M10
	P74		55	-	-	-	-	L10
	P80	General-purpose I/O port 8	118	98	78	76	A3	A3
	P81		119	99	79	77	A2	A2
	PE0	General-purpose I/O port E	56	46	36	24	M10	N10
	PE2		58	48	38	26	N11	N11
	PE3		59	49	39	27	N12	N12
Multi- function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	88	73	59	51	C13	D11
	SIN0_1		65	55	44	33	K12	J12
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I^2C (operation mode 4).	87	72	58	50	D12	D12
	SOT0_1 (SDA0_1)		66	56	45	34	J13	J11
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SCL0 when it is used in an I^2C (operation mode 4).	86	71	57	49	D13	D13
	SCK0_1 (SCL0_1)		67	57	46	35	J12	J10
Multi- function Serial 1	SIN1_0	Multi-function serial interface ch.1 input pin	96	81	66	59	A9	D9
	SIN1_1		62	52	41	30	L13	L12
	SOT1_0 (SDA1_0)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I^2C (operation mode 4).	97	82	67	60	B9	C9
	SOT1_1 (SDA1_1)		63	53	42	31	L12	K12
	SCK1_0 (SCL1_0)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation modes 4) and as SCL1 when it is used in an I^2C (operation mode 4).	98	83	-	61	C9	B9
	SCK1_1 (SCL1_1)		64	54	43	32	K13	K11

Pin function	Pin name	Function description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
Multi- function Serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	114	94	74	72	B5	C4
	SIN5_1		113	-	-	-	-	B5
	SIN5_2		20	15	-	93	G3	H2
	SOT5_0 (SDA5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I²C (operation mode 4).	115	95	75	73	B4	B4
	SOT5_1 (SDA5_1)		112	-	-	-	-	C5
	SOT5_2 (SDA5_2)		21	16	-	94	H2	H3
	SCK5_0 (SCL5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation modes 2) and as SCL5 when it is used in an I²C (operation mode 4).	116	96	76	74	B3	B3
	SCK5_1 (SCL5_1)		111	-	-	-	-	D5
	SCK5_2 (SCL5_2)		22	17	-	95	H3	H4
Multi- function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	7	7	7	85	E1	E1
	SIN6_1		95	80	65	58	A10	B10
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I²C (operation mode 4).	8	8	8	86	E2	E2
	SOT6_1 (SDA6_1)		94	79	64	57	B10	A11
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation modes 2) and as SCL6 when it is used in an I²C (operation mode 4).	9	-	-	-	-	E3
	SCK6_1 (SCL6_1)		93	78	63	56	B11	C10
	SCS6_1	Multi-function serial interface ch.6 serial chip select pin	92	77	62	55	A12	B13
Multi- function Serial 7	SIN7_0	Multi-function serial interface ch.7 input pin	101	86	-	64	C8	C8
	SIN7_1		50	45	35	23	L9	L8
	SOT7_0 (SDA7_0)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I²C (operation mode 4).	100	85	-	63	B8	D8
	SOT7_1 (SDA7_1)		49	44	34	22	M9	M8
	SCK7_0 (SCL7_0)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a CSIO (operation modes 2) and as SCL7 when it is used in an I²C (operation mode 4).	99	84	-	62	A8	A9
	SCK7_1 (SCL7_1)		48	43	33	21	L8	K7
	SCS7_1	Multi-function serial interface ch.7 serial chip select pin	47	42	32	20	L7	L7

Type	Circuit	Remarks
I		• CMOS level output • CMOS level hysteresis input • 5V tolerant • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = -4mA, I_{OL} = 4mA • Available to control of PZR registers.
J		CMOS level hysteresis input
L		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = -8mA, I_{OL} = 8mA

Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF		Multi-function timer unit1
0x4002_2000	0x4003_FFFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_4FFF		Reserved
0x4003_3000	0x4003_3FFF		D/A Converter
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low Voltage Detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		RTC/Port Ctrl
0x4003_C000	0x4003_C0FF		Low-speed CR Prescaler
0x4003_C100	0x4003_C7FF		Peripheral Clock Gating
0x4003_C800	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External Memory interface
0x4004_0000	0x4005_FFFF	AHB	Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_3FFF		DSTC register
0x4006_4000	0x4006_DFFF		Reserved
0x4006_E000	0x4006_EFFF		SD-Card I/F
0x4006_F000	0x4006_FFFF		GPIO
0x4006_7000	0x41FF_FFFF		Reserved
0x200E_0000	0x200E_FFFF		WorkFlash I/F register

*5: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

*6: Data access is nothing to MainFlash memory

*7: Frequency is a value of HCLK. PCLK0 = PCLK2 = HCLK/2, PCLK1 = HCLK

*8: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

Table 12-3. Typical and maximum current consumption in Normal operation(PLL), code with data accessing running from Flash memory (flash 0 wait-cycle mode and read access 0 wait)

Parameter	Symbol	Pin name	Conditions	Frequency*4 (MHz)	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation*5 (PLL)	72MHz	46	98	mA	*3 When all peripheral clocks are ON
				60MHz	40	92		
				48MHz	33	85		
				36MHz	27	78		
				24MHz	19	70		
				12MHz	11	61		
				8MHz	8.5	58		
				4MHz	5.5	55		
				72MHz	33	85	mA	*3 When all peripheral clocks are OFF
				60MHz	29	81		
				48MHz	25	76		
				36MHz	20	71		
				24MHz	15	65		
				12MHz	9.2	59		
				8MHz	6.9	56		
				4MHz	4.6	54		

*1: T_A = +25°C, V_{CC} = 3.3V

*2: Tj = +125°C, V_{CC} = 5.5V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0 = PCLK1 = PCLK2 = HCLK

*5: When 0 wait-cycle mode (FRWTR.RWT = 00, FSYNDN.SD = 00)

12.3.2 Pin Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

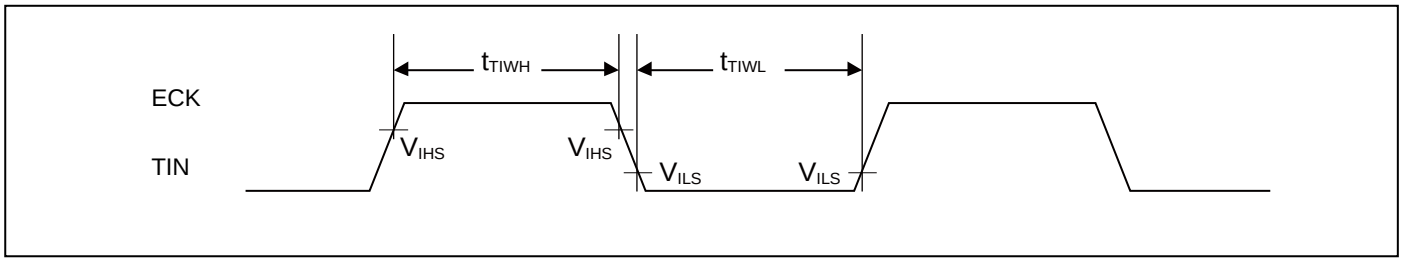
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC}×0.8	-	V_{CC} + 0.3	V	
		5V tolerant input pin	-	V_{CC}×0.8	-	V_{SS} + 5.5	V	
		Input pin doubled as I^2C Fm+	-	V_{CC}×0.7	-	V_{SS} + 5.5	V	
"L" level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		5V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		Input pin doubled as I^2C Fm+	-	V_{SS}	-	V_{CC}×0.3	V	
"H" level output voltage	V_{OH}	4mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 4mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 2mA					
		8mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 8mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 4mA					
		12mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 12mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 8mA					
		The pin doubled as I^2C Fm+	V_{CC} ≥ 4.5 V, I_{OH} = - 4mA	V_{CC} - 0.5	-	V_{CC}	V	At GPIO
			V_{CC} < 4.5 V, I_{OH} = - 3mA					

12.4.10 Base Timer Input Timing

Timer input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

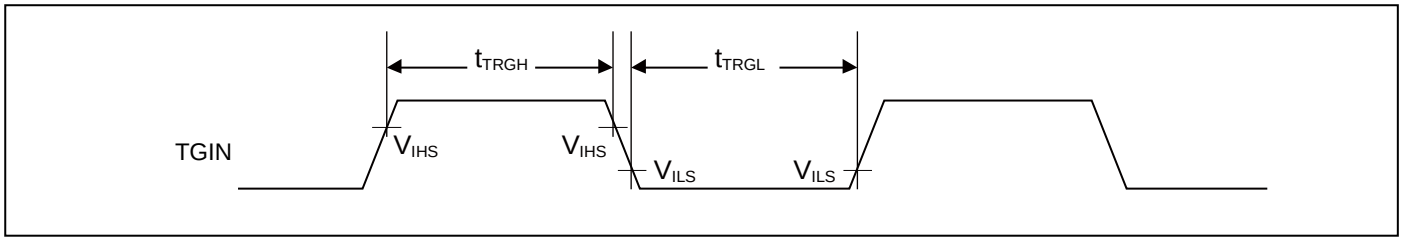
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

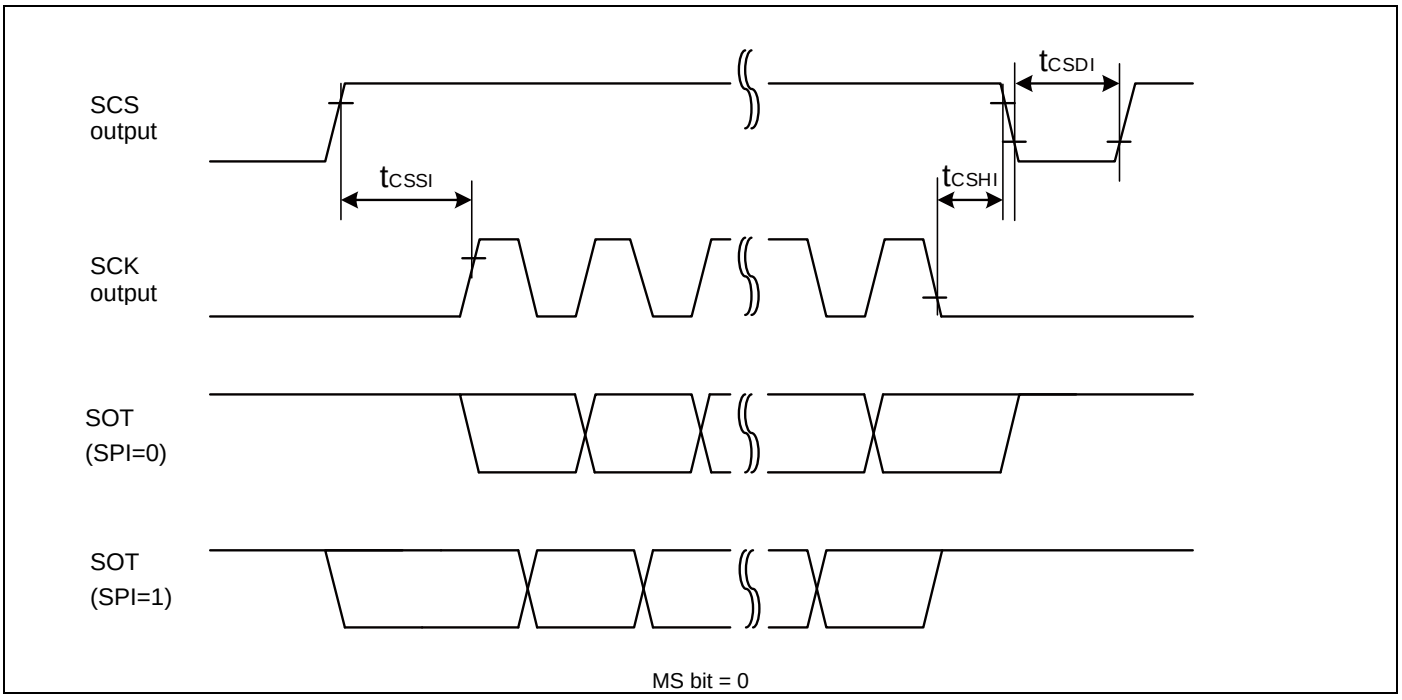
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



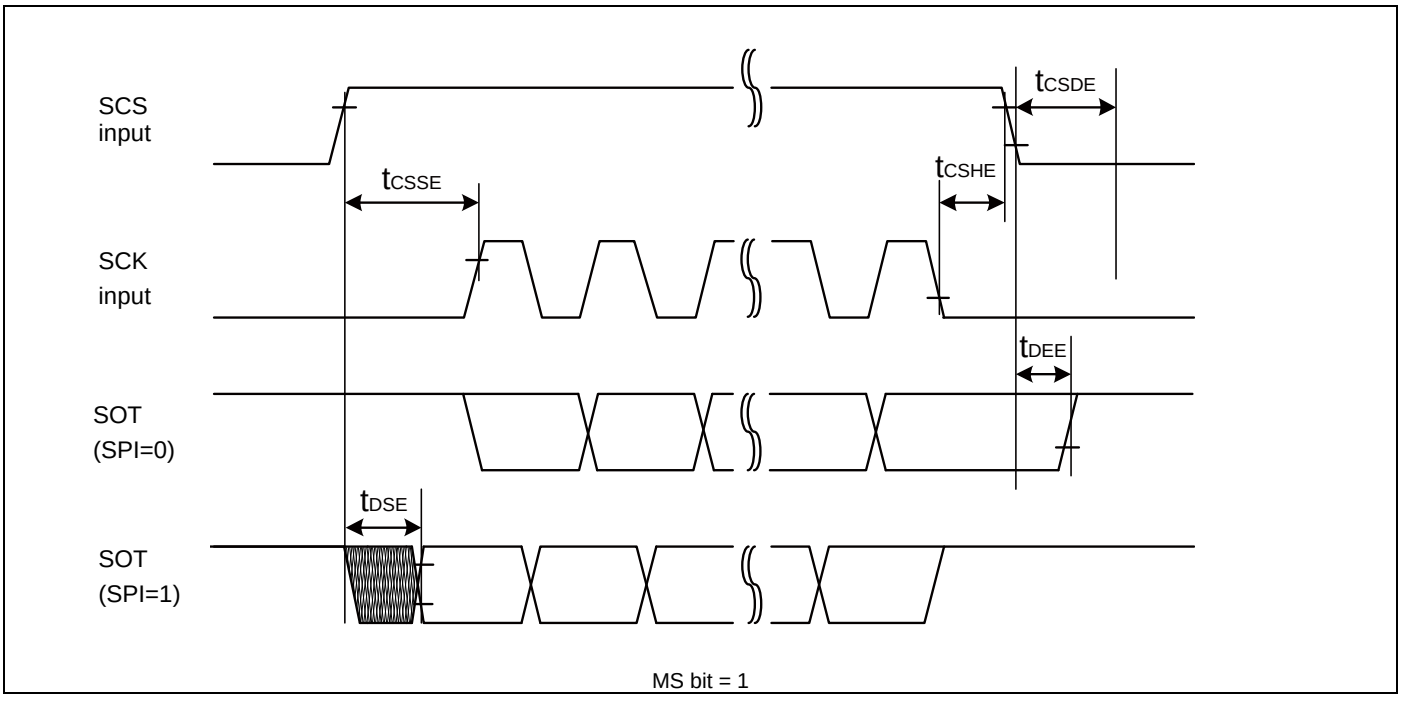
Note:

t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which the Base Timer is connected to, see “Block Diagram” in this datasheet.



MS bit = 0



MS bit = 1

When using high-speed synchronous serial chip select (SCINV = 0, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↑→SCK↓setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

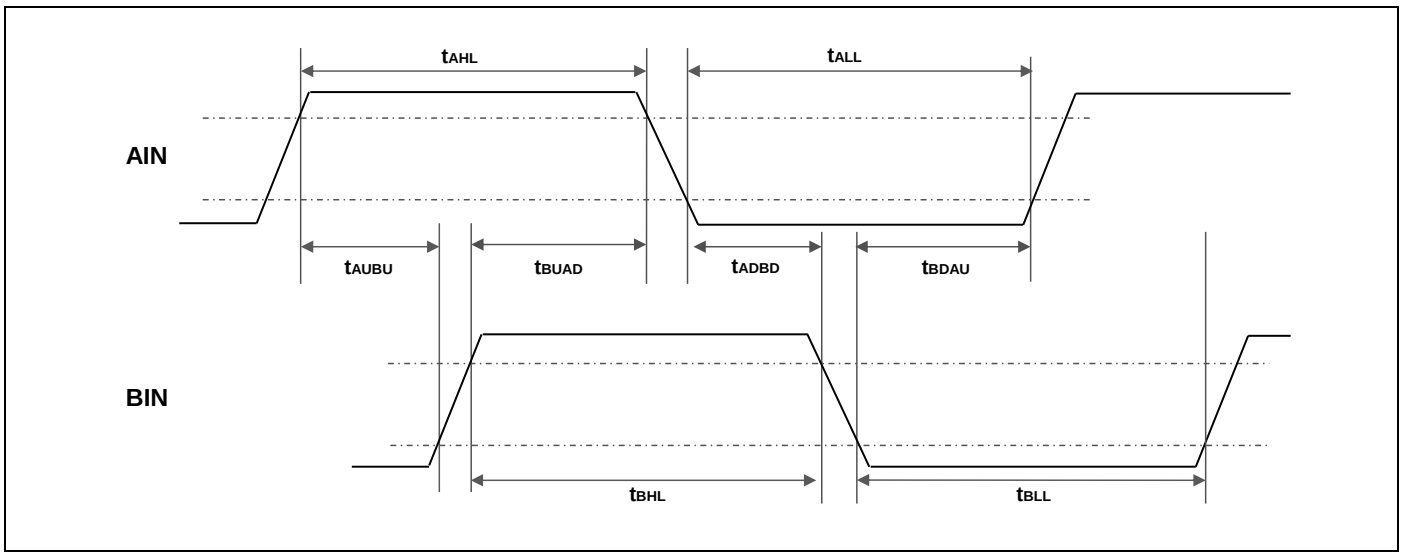
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM4 Family Peripheral Manual".*
- *When the external load capacitance C_L = 30pF.*

12.4.13 Quadrature Position/Revolution Counter Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin "H" width	t_{AHL}	-			
AIN pin "L" width	t_{ALL}	-			
BIN pin "H" width	t_{BHL}	-			
BIN pin "L" width	t_{BLL}	-			
BIN rising time from AIN pin "H" level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin "H" level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin "L" level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin "L" level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin "H" level	t_{BUAU}	PC_Mode2 or PC_Mode3	$2t_{CYCP}$*	-	ns
BIN falling time from AIN pin "H" level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin "L" level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rising time from AIN pin "L" level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin "H" width	t_{ZHL}	QCR:CGSC = "0"			
ZIN pin "L" width	t_{ZLL}	QCR:CGSC = "0"			
AIN/BIN rising and falling time from determined ZIN level	t_{ZABE}	QCR:CGSC = "1"			
Determined ZIN level from AIN/BIN rising and falling time	t_{ABEZ}	QCR:CGSC = "1"			

*: t_{CYCP} indicates the APB bus clock cycle time except stop when in STOP mode, in timer mode.
About the APB bus number which Quadrature Position/Revolution Counter is connected to, see “Block Diagram” in this data sheet.

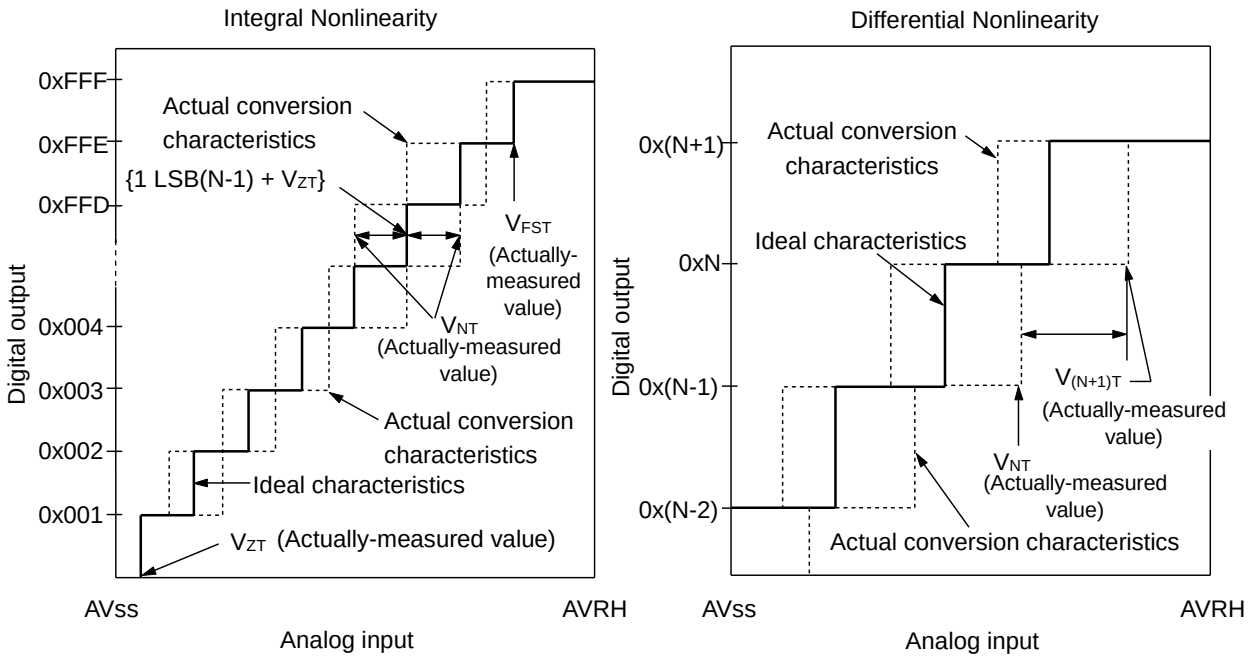


Definition of 12-bit A/D Converter Terms

■Resolution: Analog variation that is recognized by an A/D converter.

■Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.

■Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.

V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.

V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.

V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

12.8 MainFlash Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 5.5V)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector		0.3	1.1		
Half word (16-bit) write time	Write cycles ≤ 100 times	-	12	100	µs	Not including system-level overhead time
	Write cycles > 100 times			200		
Chip erase time		-	13.6	68	s	Includes write time prior to internal erase

Write cycles and data hold time

Erase/Write cycles (cycle)	Data hold time (year)
1,000	20 *
10,000	10 *
100,000	5 *

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C) .

12.9 WorkFlash Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 5.5V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.3	1.5	s	Includes write time prior to internal erase
Half word (16-bit) write time	-	20	200	µs	Not including system-level overhead time
Chip erase time	-	1.2	6	s	Includes write time prior to internal erase

Write cycles and data hold time

Erase/Write cycles (cycle)	Data hold time (year)
1,000	20 *
10,000	10 *
100,000	5 *

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C) .