Welcome to E-XFL.COM

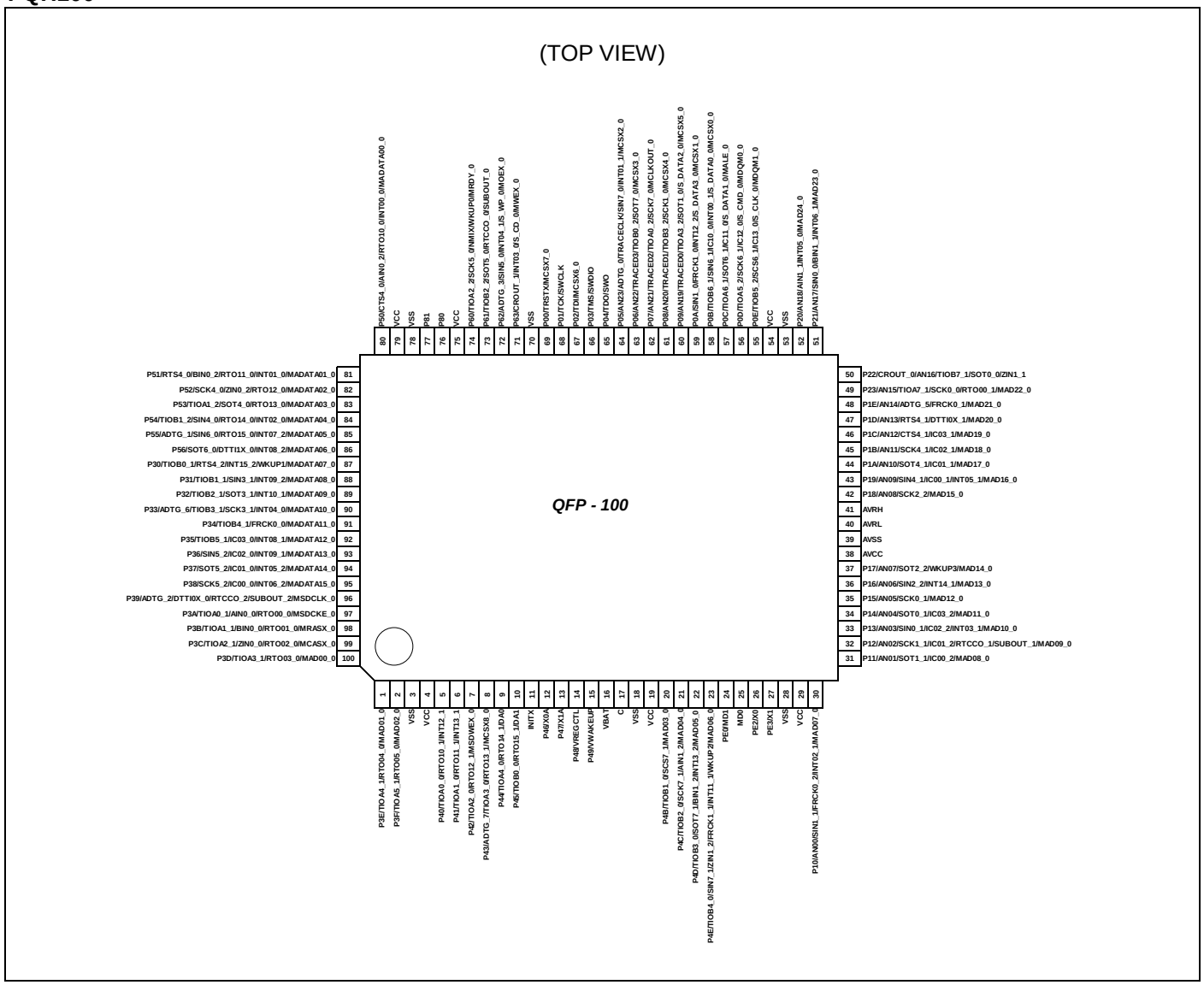
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9bf166rpmc-g-jne2

PQH100



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
26	21	16	99	K1	J4	P3C TIOA2_1 ZIN0_0 RTO02_0 (PPG02_0)	G	I
		-				MCASX_0		
27	22	17	100	K2	K2	P3D TIOA3_1 RTO03_0 (PPG02_0) MAD00_0	G	I
28	23	18	1	L1	K3	P3E TIOA4_1 RTO04_0 (PPG04_0) MAD01_0	G	I
29	24	19	2	L2	L1	P3F TIOA5_1 RTO05_0 (PPG04_0) MAD02_0	G	I
30	25	20	3	N1	N1	VSS	-	-
31	26	-	4	M1	M1	VCC	-	-
32	27	-	5	N2	N2	P40 TIOA0_0 RTO10_1 (PPG10_1) INT12_1	G	K
33	28	-	6	N3	L2	P41 TIOA1_0 RTO11_1 (PPG10_1) INT13_1	G	K
34	29	-	7	M3	N3	P42 TIOA2_0 RTO12_1 (PPG12_1) MSDWEX_0	G	I
35	30	-	8	L3	M3	P43 ADTG_7 TIOA3_0 RTO13_1 (PPG12_1) MCSX8_0	G	I

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
75	65	54	43	G12	G12	P19 AN09 SIN4_1 IC00_1 INT05_1 MAD16_0	F	M
76	66	55	44	G11	G11	P1A AN10 SOT4_1 (SDA4_1) IC01_1 MAD17_0	M	L
77	67	56	45	F12	G10	P1B AN11 SCK4_1 (SCL4_1) IC02_1 MAD18_0	M	L
78	68	-	46	F11	F13	P1C AN12 CTS4_1 IC03_1 MAD19_0	F	L
79	69	-	47	E12	F12	P1D AN13 RTS4_1 DTTI0X_1 MAD20_0	F	L
80	70	-	48	E11	F11	P1E AN14 ADTG_5 FRCK0_1 MAD21_0	F	L
81	-	-	-	-	F10	P1F ADTG_4 TIOB6_2 RTO05_1 (PPG04_1)	E	I
82	-	-	-	-	E13	P27 TIOA6_2 RTO04_1 (PPG04_1) INT02_2	E	K

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
99	84	-	62	A8	A9	P07 AN21 TRACED2 TIOA0_2 SCK7_0 (SCL7_0) MCLKOUT_0	F	N
100	85	-	63	B8	D8	P06 AN22 TRACED3 TIOB0_2 SOT7_0 (SDA7_0) MCSX3_0	F	N
101	86	-	64	C8	C8	P05 AN23 ADTG_0 TRACECLK SIN7_0 INT01_1 MCSX2_0	F	O
102	87	68	65	C7	B8	P04 TDO SWO	E	G
103	88	69	66	B7	D7	P03 TMS SWDIO	E	G
104	89	70	67	C6	C7	P02 TDI MCSX6_0	E	H
105	90	71	68	A6	B7	P01 TCK SWCLK	E	G
106	91	72	69	B6	D6	P00 TRSTX MCSX7_0	E	H
107	92	-	70	A5	A7	VSS	-	-
108	-	-	-	-	C6	P68 TIOB7_2 SCK3_0 (SCL3_0) INT00_2	E	K
109	-	-	-	-	B6	P67 TIOA7_2 SOT3_0 (SDA3_0)	E	I

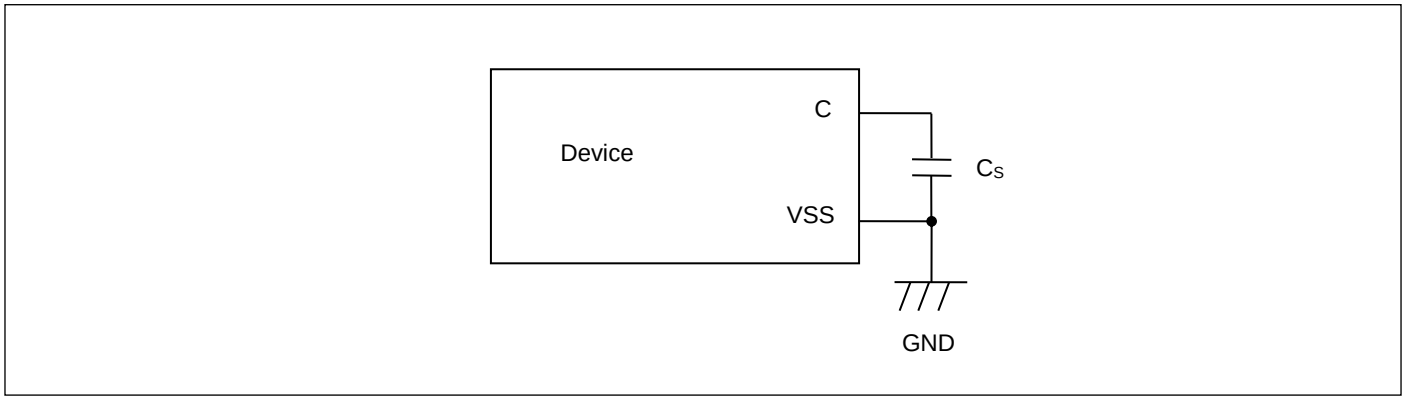
Pin function	Pin name	Function description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	35	30	-	8	L3	M3
	TIOA3_1		27	22	17	100	K2	K2
	TIOA3_2		97	82	67	60	B9	C9
	TIOB3_0	Base timer ch.3 TIOB pin	49	44	34	22	M9	M8
	TIOB3_1		17	12	12	90	F3	G3
	TIOB3_2		98	83	-	61	C9	B9
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	36	31	21	9	M4	L4
	TIOA4_1		28	23	18	1	L1	K3
	TIOA4_2		51	-	-	-	-	K8
	TIOB4_0	Base timer ch.4 TIOB pin	50	45	35	23	L9	L8
	TIOB4_1		18	13	-	91	G1	G4
	TIOB4_2		52	-	-	-	-	L9
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	84	-	-	-	-	E11
	TIOA5_1		29	24	19	2	L2	L1
	TIOA5_2		93	78	63	56	B11	C10
	TIOB5_0	Base timer ch.5 TIOB pin	83	-	-	-	-	E12
	TIOB5_1		19	14	-	92	G2	H1
	TIOB5_2		92	77	62	55	A12	B13
Base Timer 6	TIOA6_0	Base timer ch.6 TIOA pin	53	-	-	-	-	K9
	TIOA6_1		94	79	64	57	B10	A11
	TIOA6_2		82	-	-	-	-	E13
	TIOB6_0	Base timer ch.6 TIOB pin	54	-	-	-	-	M10
	TIOB6_1		95	80	65	58	A10	B10
	TIOB6_2		81	-	-	-	-	F10
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	112	-	-	-	-	C5
	TIOA7_1		86	71	57	49	D13	D13
	TIOA7_2		109	-	-	-	-	B6
	TIOB7_0	Base timer ch.7 TIOB pin	111	-	-	-	-	D5
	TIOB7_1		87	72	58	50	D12	D12
	TIOB7_2		108	-	-	-	-	C6
Debugger	SWCLK	Serial wire debug interface clock input pin	105	90	71	68	A6	B7
	SWDIO	Serial wire debug interface data input / output pin	103	88	69	66	B7	D7
	SWO	Serial wire viewer output pin	102	87	68	65	C7	B8
	TCK	JTAG test clock input pin	105	90	71	68	A6	B7
	TDI	JTAG test data input pin	104	89	70	67	C6	C7
	TDO	JTAG debug data output pin	102	87	68	65	C7	B8
	TMS	JTAG test mode state input/output pin	103	88	69	66	B7	D7
	TRACECLK	Trace CLK output pin of ETM	101	86	-	64	C8	C8
	TRACED0	Trace data output pin of ETM	97	82	-	60	B9	C9
	TRACED1		98	83	-	61	C9	B9
	TRACED2		99	84	-	62	A8	A9
	TRACED3		100	85	-	63	B8	D8
	TRSTX	JTAG test reset Input pin	106	91	72	69	B6	D6

Handling when using Multi-function serial pin as I²C pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled.
However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 µF would be recommended for this series.



Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on power-on

Turn power on/off in the following order or at the same time. The device operates normally after all power on.

VBAT only Power-on is possible when VBAT and VCC turns Power-on and Hibernation control is setting and then VCC turns Power-off. About Hibernation control, see Chapter 7-2: VBAT Domain(A) in FM4 Family Peripheral Manual Main Part(002-04856).
If not using the A/D converter and D/A converter, connect AVCC = VCC and AVSS = VSS.

Turning on : VBAT → VCC

VCC → AVCC → AVRH

Turning off : AVRH → AVCC → VCC

VCC → VBAT

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in features among the products with different memory sizes and between Flash products and MASK products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF		Multi-function timer unit1
0x4002_2000	0x4003_FFFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_4FFF		Reserved
0x4003_3000	0x4003_3FFF		D/A Converter
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low Voltage Detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		RTC/Port Ctrl
0x4003_C000	0x4003_C0FF		Low-speed CR Prescaler
0x4003_C100	0x4003_C7FF		Peripheral Clock Gating
0x4003_C800	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External Memory interface
0x4004_0000	0x4005_FFFF	AHB	Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_3FFF		DSTC register
0x4006_4000	0x4006_DFFF		Reserved
0x4006_E000	0x4006_EFFF		SD-Card I/F
0x4006_F000	0x4006_FFFF		GPIO
0x4006_7000	0x41FF_FFFF		Reserved
0x200E_0000	0x200E_FFFF		WorkFlash I/F register

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

- INITX = 0

  This is the period when the INITX pin is the "L" level.

- INITX = 1

  This is the period when the INITX pin is the "H" level.

- SPL = 0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "0".

- SPL = 1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "1".

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at "0"

  This is the status that the input function cannot be used. Internal input is fixed at "L".

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep standby mode, pins switch to the general-purpose I/O port.

- Setting prohibition

  Prohibition of a setting by specification limitation.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage *1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (VBAT) *1, *3	V_{BAT}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage *1, *4	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage *1, *4	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage *1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5V tolerant
Analog pin input voltage *1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5V)	V	
Output voltage *1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5V)	V	
"L" level maximum output current *5	I_{OL}	-	10	mA	4mA type
			20	mA	8mA type
			20	mA	12mA type
			22.4	mA	I^2C Fm+
"L" level average output current *6	I_{OLAV}	-	4	mA	4mA type
			8	mA	8mA type
			12	mA	12mA type
			20	mA	I^2C Fm+
"L" level total maximum output current	$\sum I_{OL}$	-	100	mA	
"L" level total maximum output current *7	$\sum I_{OLAV}$	-	50	mA	
"H" level maximum output current *5	I_{OH}	-	- 10	mA	4mA type
			20	mA	8mA type
			- 20	mA	12mA type
"H" level average output current *6	I_{OHAV}	-	- 4	mA	4mA type
			8	mA	8mA type
			- 12	mA	12mA type
"H" level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
"H" level total average output current *7	$\sum I_{OHAV}$	-	- 50	mA	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0V$.

*2: V_{CC} must not drop below V_{SS} - 0.5V.

*3: V_{BAT} must not drop below V_{SS} - 0.5V.

*4: Ensure that the voltage does not exceed V_{CC} + 0.5V, for example, when the power is turned on.

*5: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*6: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100ms period.

*7: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100ms.

WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.*
  Do not exceed any of these ratings.

Calculation method of power dissipation (Pd)

The power dissipation is shown in the following formula.

$Pd = V_{CC} \times I_{CC} + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (-I_{OH}))$

I_{OL}: "L" level output current
I_{OH}: "H" level output current
V_{OL}: "L" level output voltage
V_{OH}: "H" level output voltage

I_{CC} is a current consumed in device.
It can be analyzed as follows.

$I_{CC} = I_{CC}(INT) + \Sigma I_{CC}(IO)$

$I_{CC}(INT)$: Current consumed in internal logic and memory, etc. through regulator
$\Sigma I_{CC}(IO)$: Sum of current (I/O switching current) consumed in output pin

For I_{CC} (INT), it can be anticipated by "(1) Current Rating" in "3. DC Characteristics" (This rating value does not include I_{CC} (IO) for a value at pin fixed).
For Icc (IO), it depends on system used by customers.
The calculation formula is shown below.

$I_{CC}(IO) = (C_{INT} + C_{EXT}) \times V_{CC} \times fsw$

C_{INT}: Pin internal load capacitance
C_{EXT}: External load capacitance of output pin
f_{SW}: Pin switching frequency

Parameter	Symbol	Conditions	Capacitance value
Pin internal load capacitance	C_{INT}	4mA type	1.93pF
		8mA type	3.45pF
		12mA type	3.42pF

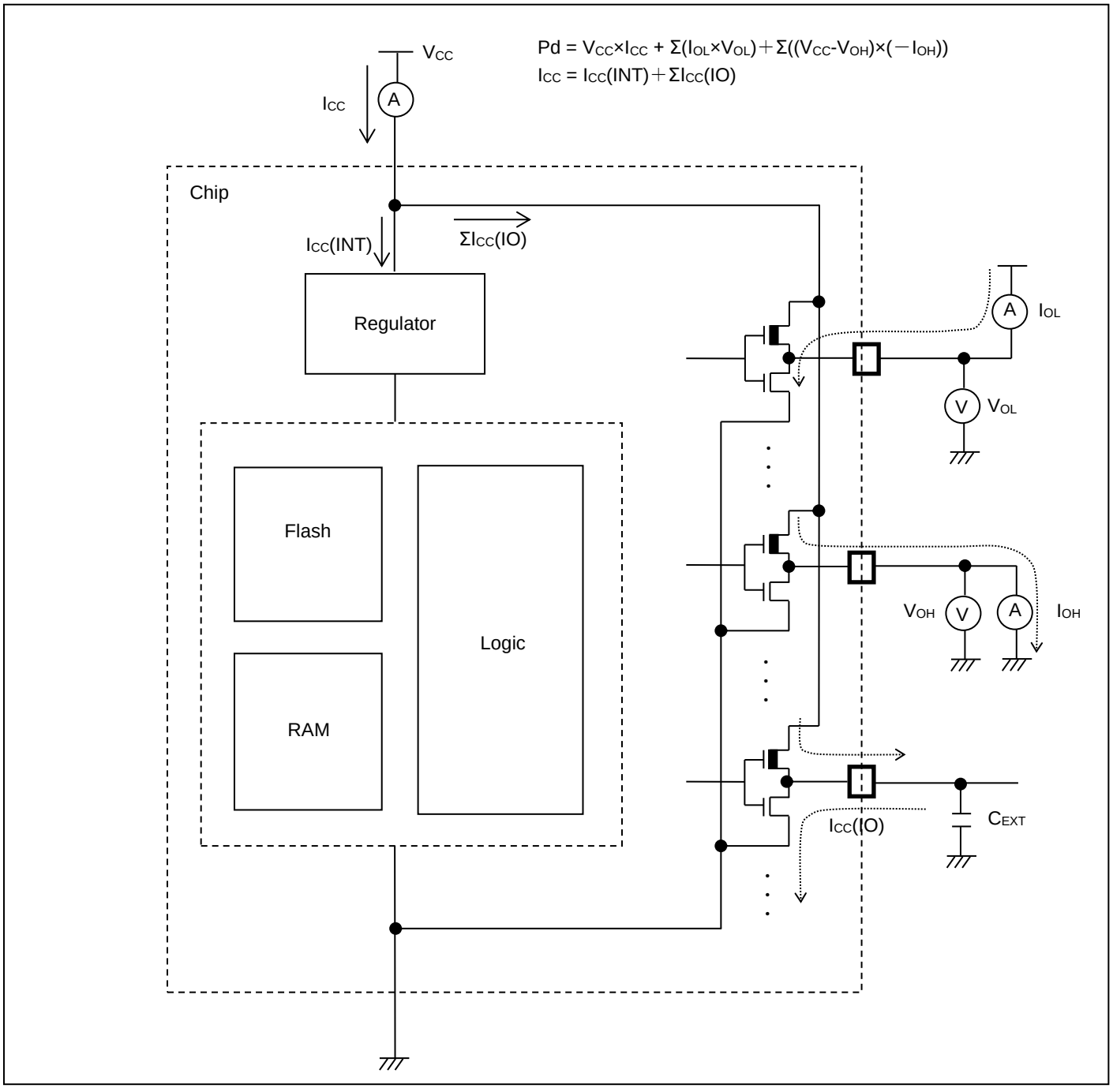
Calculate I_{CC} (Max) as follows when the power dissipation can be evaluated by yourself.

1. Measure current value I_{CC} (Typ) at normal temperature (+25°C).
2. Add maximum leak current value I_{CC} (leak_max) at operating on a value in (1).

$I_{CC}(Max) = I_{CC}(Typ) + I_{CC}(leak\_max)$

Parameter	Symbol	Conditions	Current value
Maximum leak current at operating	I_{CC}(leak_max)	Tj = +125°C	45.5mA
		Tj = +105°C	26.8mA
		Tj = +85°C	16.2mA

Current explanation diagram



12.3 DC Characteristics

12.3.1 Current Rating

Table 12-1. Typical and maximum current consumption in Normal operation(PLL), code running from Flash memory (Flash accelerator mode and trace buffer function enabled)

Parameter	Symbol	Pin name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation*5,*6 (PLL)	160MHz	54	103	mA	*3 When all peripheral clocks are ON
				144MHz	49	98		
				120MHz	41	90		
				100MHz	35	84		
				80MHz	28	77		
				60MHz	22	71		
				40MHz	16	64		
				20MHz	8.9	58		
				8MHz	5.1	54		
				4MHz	3.8	53		
				160MHz	34	83	mA	*3 When all peripheral clocks are OFF
				144MHz	31	80		
				120MHz	26	75		
				100MHz	22	71		
				80MHz	18	67		
				60MHz	14	63		
				40MHz	10	59		
				20MHz	6.2	55		
				8MHz	3.8	53		
				4MHz	3.1	52		

Table 12-2. Typical and maximum current consumption in Normal operation(PLL), code with data accessing running from Flash memory (Flash accelerator mode and trace buffer function disabled)

Parameter	Symbol	Pin name	Conditions	Frequency*7	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation*8 (PLL)	160MHz	74	126	mA	*3 When all peripheral clocks are ON
				144MHz	68	120		
				120MHz	59	112		
				100MHz	52	104		
				80MHz	44	97		
				60MHz	36	89		
				40MHz	27	79		
				20MHz	17	67		
				8MHz	8.3	58		
				4MHz	5.4	55		
				160MHz	51	103	mA	*3 When all peripheral clocks are OFF
				144MHz	47	100		
				120MHz	42	94		
				100MHz	37	90		
				80MHz	33	85		
				60MHz	28	80		
				40MHz	21	73		
				20MHz	13	64		
				8MHz	6.9	56		
				4MHz	4.6	54		

*1: T_A = +25°C, V_{CC} = 3.3V

*2: Tj = +125°C, V_{CC} = 5.5V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0 = PCLK1 = PCLK2 = HCLK/2

*5: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

*6: Data access is nothing to MainFlash memory

*7: Frequency is a value of HCLK. PCLK0 = PCLK2 = HCLK/2, PCLK1 = HCLK

*8: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

Table 12-3. Typical and maximum current consumption in Normal operation(PLL), code with data accessing running from Flash memory (flash 0 wait-cycle mode and read access 0 wait)

Parameter	Symbol	Pin name	Conditions	Frequency*4 (MHz)	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation*5 (PLL)	72MHz	46	98	mA	*3 When all peripheral clocks are ON
				60MHz	40	92		
				48MHz	33	85		
				36MHz	27	78		
				24MHz	19	70		
				12MHz	11	61		
				8MHz	8.5	58		
				4MHz	5.5	55		
				72MHz	33	85	mA	*3 When all peripheral clocks are OFF
				60MHz	29	81		
				48MHz	25	76		
				36MHz	20	71		
				24MHz	15	65		
				12MHz	9.2	59		
				8MHz	6.9	56		
				4MHz	4.6	54		

*1: T_A = +25°C, V_{CC} = 3.3V

*2: Tj = +125°C, V_{CC} = 5.5V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0 = PCLK1 = PCLK2 = HCLK

*5: When 0 wait-cycle mode (FRWTR.RWT = 00, FSYNDN.SD = 00)

Table 12-8. Typical and maximum current consumption in STOP mode, TIMER mode and RTC mode

Parameter	Symbol	Pin name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCH}	VCC	STOP mode	-	0.33	1.8	mA	*3, *4 T_A = +25°C
					-	15	mA	*3, *4 T_A = +85°C
					-	22	mA	*3, *4 T_A = +105°C
	I_{CCT}		TIMER mode (built-in high-speed CR)	4MHz	0.70	2.2	mA	*3, *4 T_A = +25°C
					-	16	mA	*3, *4 T_A = +85°C
					-	22	mA	*3, *4 T_A = +105°C
			TIMER mode (sub oscillation)	32kHz	0.33	1.8	mA	*3, *4 T_A = +25°C
					-	15	mA	*3, *4 T_A = +85°C
					-	22	mA	*3, *4 T_A = +105°C
			TIMER mode (built-in low-speed CR)	100kHz	0.34	1.8	mA	*3, *4 T_A = +25°C
					-	15	mA	*3, *4 T_A = +85°C
					-	22	mA	*3, *4 T_A = +105°C
	I_{CCR}		RTC mode (sub oscillation)	32kHz	0.33	1.8	mA	*3, *4 T_A = +25°C
					-	15	mA	*3, *4 T_A = +85°C
					-	22	mA	*3, *4 T_A = +105°C

*1: V_{CC} = 3.3V

*2: V_{CC} = 5.5V

*3: When all ports are fixed.

*4: When LVD is OFF

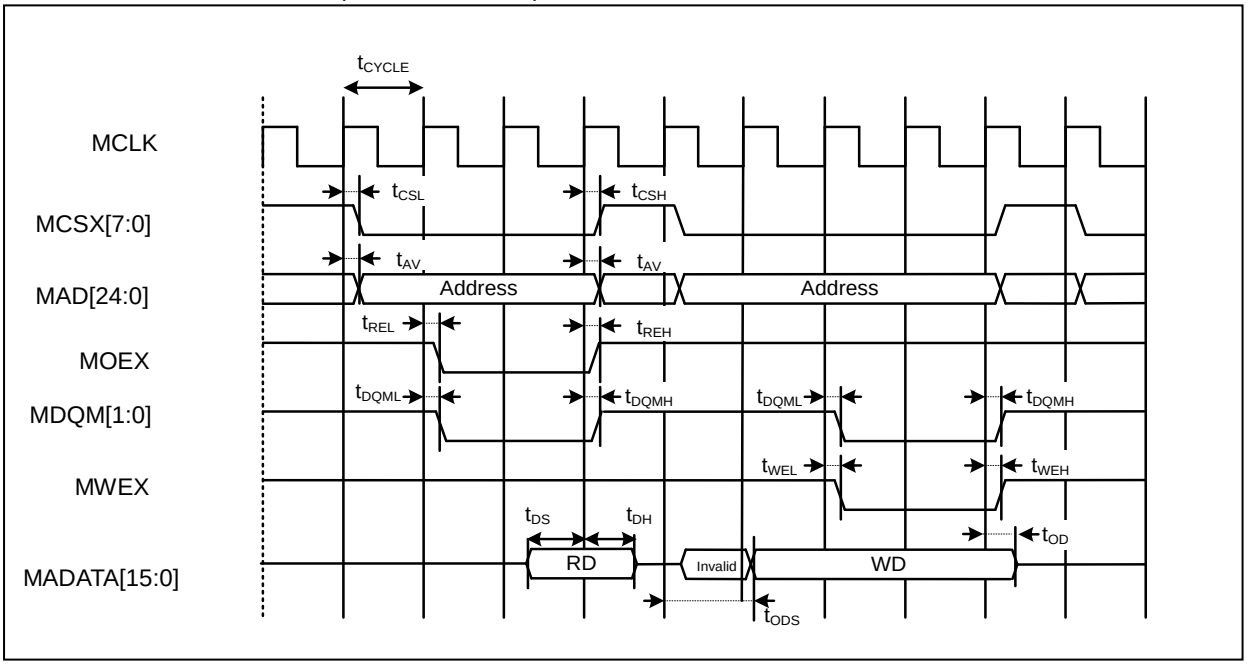
Separate Bus Access Synchronous SRAM Mode

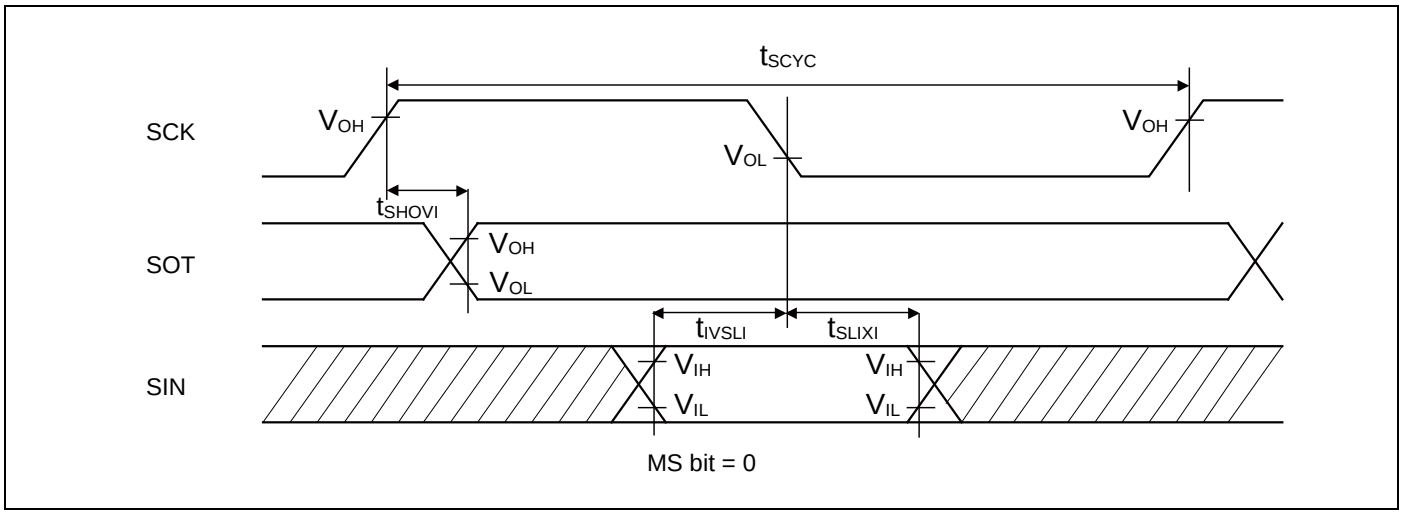
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Address delay time	t_{AV}	MCLK, MAD[24:0]	$V_{CC} \geq 4.5V$	1	9	ns
			$V_{CC} < 4.5V$		12	
MCSX delay time	t_{CSL}	MCLK, MCSX[7:0]	$V_{CC} \geq 4.5V$	1	9	ns
			$V_{CC} < 4.5V$		12	
	t_{CSH}		$V_{CC} \geq 4.5V$	1	9	ns
			$V_{CC} < 4.5V$		12	
MOEX delay time	t_{REL}	MCLK, MOEX	$V_{CC} \geq 4.5V$	1	9	ns
			$V_{CC} < 4.5V$		12	
	t_{REH}		$V_{CC} \geq 4.5V$	1	9	ns
			$V_{CC} < 4.5V$		12	
Data set up →MCLK↑ time	t_{DS}	MCLK, MADATA[15:0]	$V_{CC} \geq 4.5V$	19	-	ns
			$V_{CC} < 4.5V$	37		
MCLK↑→ Data hold time	t_{DH}	MCLK, MADATA[15:0]	$V_{CC} \geq 4.5V$	0	-	ns
			$V_{CC} < 4.5V$			
MWEX delay time	t_{WEL}	MCLK, MWEX	$V_{CC} \geq 4.5V$	1	9	ns
			$V_{CC} < 4.5V$		12	
	t_{WEH}		$V_{CC} \geq 4.5V$	1	9	ns
			$V_{CC} < 4.5V$		12	
MDQM[1:0] delay time	t_{DQML}	MCLK, MDQM[1:0]	$V_{CC} \geq 4.5V$	1	9	ns
			$V_{CC} < 4.5V$		12	
	t_{DQMH}		$V_{CC} \geq 4.5V$	1	9	ns
			$V_{CC} < 4.5V$		12	
MCLK↑→ Data output time	t_{ODS}	MCLK, MADATA[15:0]	$V_{CC} \geq 4.5V$	MCLK+1	MCLK+18	ns
			$V_{CC} < 4.5V$		MCLK+24	
MCLK↑→ Data hold time	t_{OD}	MCLK, MADATA[15:0]	$V_{CC} \geq 4.5V$	1	18	ns
			$V_{CC} < 4.5V$		24	

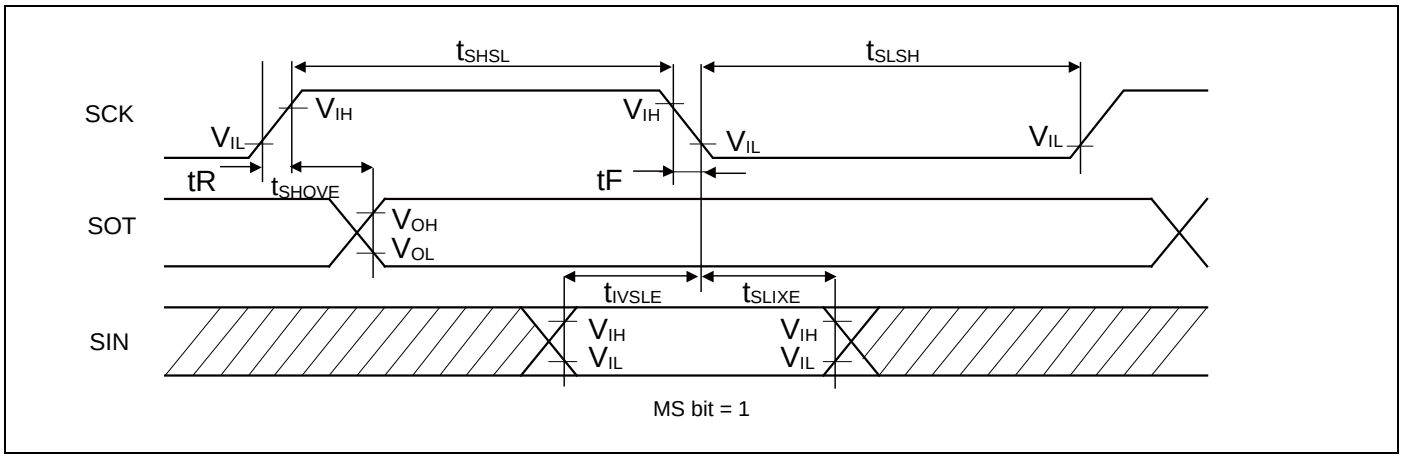
Note:

- *When the external load capacitance C_L = 30pF*

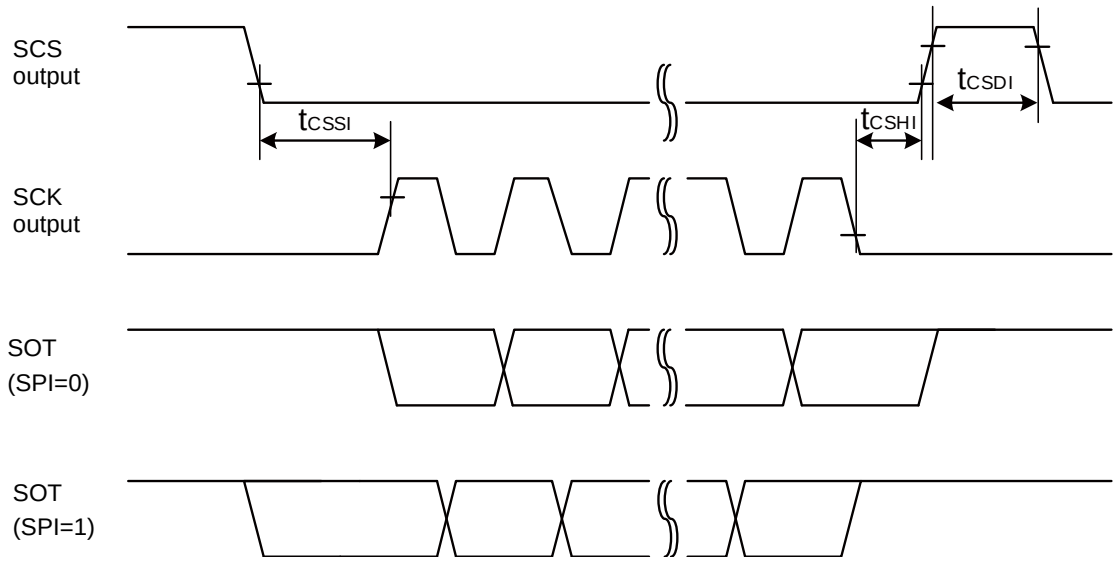




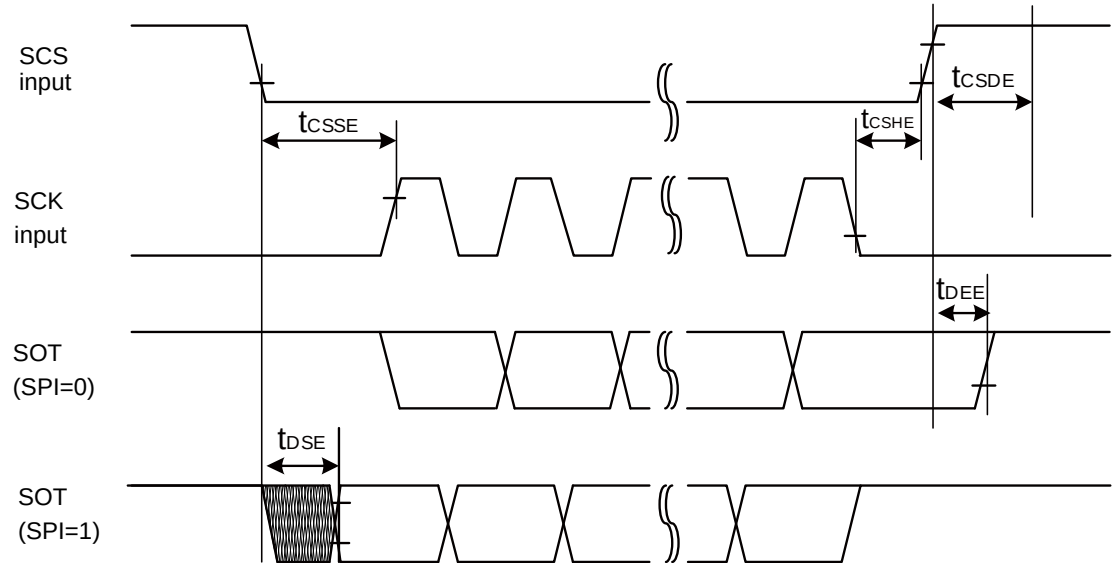
MS bit = 0



MS bit = 1



MS bit = 0



MS bit = 1

High-speed synchronous serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

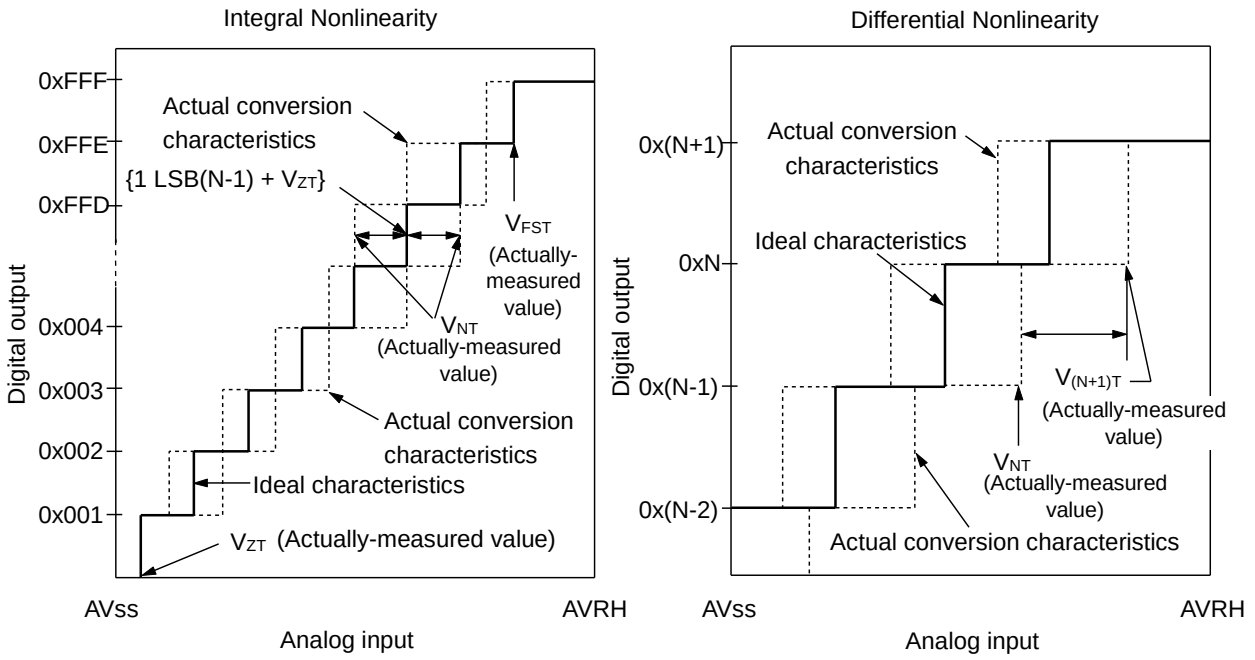
- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.
- *These characteristics only guarantee the following pins.*
  - *No chip select: SIN4_1, SOT4_1, SCK4_1*
  - *Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1*
- *When the external load capacitance C_L = 30pF. (For *, when C_L = 10pF)*

Definition of 12-bit A/D Converter Terms

■Resolution: Analog variation that is recognized by an A/D converter.

■Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.

■Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.

V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.

V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.

V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

15. Major Changes

Spansion Publication Number: DS709-00004

Page	Section	Change Results
-	-	Preliminary → Data Sheet
1	Description	Deleted the following description : The products which are described in this data sheet are placed into TYPE4 product categories in "FM4 Family PERIPHERAL MANUAL".
3	Features Multi-Function Serial Interface [I^2C]	Revised the following description : Fast mode Plus (Fm+) (Max 1000 kbps, only for ch.3 and ch.7) supported →Fast mode Plus (Fm+) (Max 1000 kbps, only for ch.3=ch.A and ch.7=ch.B) supported
7	Features Unique Id	Added new section
9	Product Lineup Function	Added “Unique ID”
51, 52	I/O Circuit Type	Revised the remarks of “Type O, P, Q”
59	Handling Devices Handling When Using Debug Pins	Added new section
60	Block Diagram	Revised the block diagram
72	Electrical Characteristics 2. Recommended Operating Conditions	Revised “Table for package thermal resistance and maximum permissible power”
75 to 80	Electrical Characteristics 3. Dc Characteristics (1) Current Rating	• Revised the value of TBD • Added the note to “ICCVBAT”
85	Electrical Characteristics 4. Ac Characteristics (2) Sub Clock Input Characteristics	Revised the waveform chart
85	Electrical Characteristics 4. Ac Characteristics (3) Built-In Cr Oscillationcharacteristics	• Revised the value of TBD • Revised the table and the note of “Built-in High-speed CR”
144	Electrical Characteristics 5. 12-Bit A/D Converter Electrical Characteristics For The A/D Converter	• Revised the value of TBD • Revised the condition of the electrical characteristics table
147	Electrical Characteristics 6. 12-Bit D/A Converter Electrical Characteristics For The D/A Converter	• Revised the value of TBD • Revised the condition and Remarks of the electrical characteristics table
150	Electrical Characteristics 10. Standby Recovery Time (1) Recovery Cause: Interrupt/Wkup	• Revised the value of TBD • Revised the table of Recovery count time
152	Electrical Characteristics 10. Standby Recovery Time (2) Recovery Cause:Reset	• Revised the value of TBD • Revised the table of Recovery count time

Note: Please see “Document History” about later revised information.