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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	63
Program Memory Size	1.03125MB (1.03125M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9bf168mpmc-g-jne2

Clock and Reset

[Clocks]

Five clock sources (2 external oscillators, 2 internal CR oscillator, and Main PLL) that are dynamically selectable.

- Main clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- High-speed internal CR Clock: 4 MHz
- Low-speed internal CR Clock: 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timers reset
- Low voltage detector reset
- Clock supervisor reset

Clock Super Visor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series include 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-power Consumption Mode

Six low-power consumption modes are supported.

- SLEEP
- TIMER
- RTC
- STOP
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby stop (selectable from with/without RAM retention)

VBAT

The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- RTC
- 32 kHz oscillation circuit
- Power-on circuit
- Back up register: 32 bytes
- Port circuit

Debug

- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.

Unique ID

Unique value of the device (41-bit) is set.

Power Supply

Two Power Supplies

- Wide range voltage: VCC = 2.7V to 5.5V
- Power supply for VBAT: VBAT = 2.7V to 5.5V

2. Packages

Package \ Product name	MB9BF166M MB9BF167M MB9BF168M	MB9BF166N MB9BF167N MB9BF168N	MB9BF166R MB9BF167R MB9BF168R
LQFP: LQH080 (0.5mm pitch)	❍	-	-
LQFP: LQJ080 (0.65mm pitch)	❍	-	-
QFP: PQH100 (0.65mm pitch)	-	❍	-
LQFP: LQI100 (0.5mm pitch)	-	❍	-
LQFP: LQM120 (0.5mm pitch)	-	-	❍
BGA: LDC112 (0.5mm pitch)	-	❍	-
BGA: LDC144 (0.5mm pitch)	-	-	❍

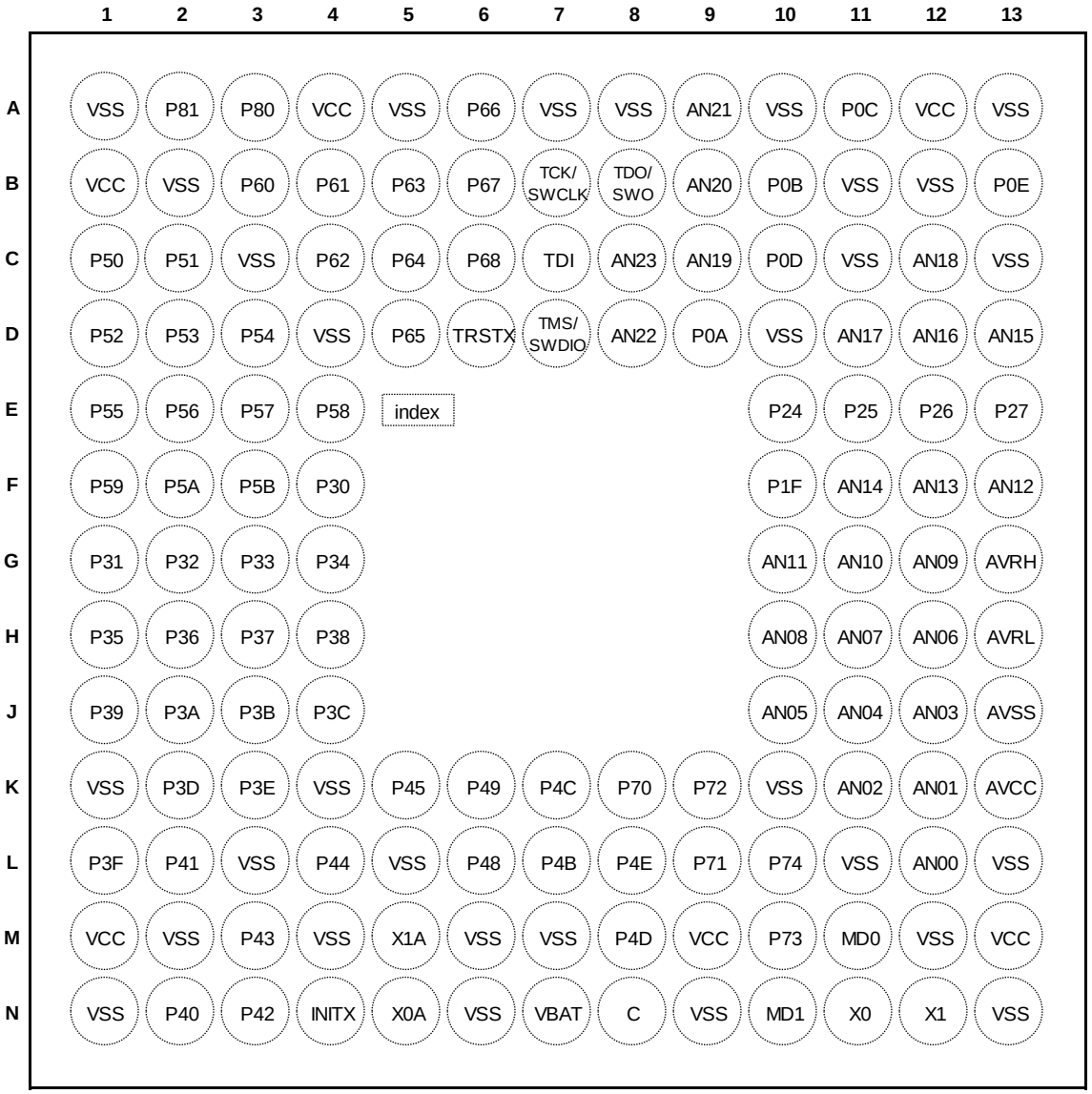
❍: Supported

Note:

- *See "Package Dimensions" for detailed information on each package.*

LDC144

(TOP VIEW)



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
64	54	43	32	K13	K11	P12 AN02 SCK1_1 (SCL1_1) IC01_2 RTCCO_1 SUBOUT_1 MAD09_0	F	L
65	55	44	33	K12	J12	P13 AN03 SIN0_1 IC02_2 INT03_1 MAD10_0	F	M
66	56	45	34	J13	J11	P14 AN04 SOT0_1 (SDA0_1) IC03_2 MAD11_0	F	L
67	57	46	35	J12	J10	P15 AN05 SCK0_1 (SCL0_1) MAD12_0	F	L
68	58	47	36	J11	H12	P16 AN06 SIN2_2 INT14_1 MAD13_0	F	M
69	59	48	37	H12	H11	P17 AN07 SOT2_2 (SDA2_2) WKUP3 MAD14_0	F	P
70	60	49	38	H13	K13	AVCC	-	-
71	61	50	39	G13	J13	AVSS	-	-
72	62	51	40	F13	H13	AVRL	-	-
73	63	52	41	E13	G13	AVRH	-	-
74	64	53	42	H11	H10	P18 AN08 SCK2_2 (SCL2_2) MAD15_0	F	L

List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin function	Pin name	Function description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
ADC	ADTG_0	A/D converter external trigger input pin	101	86	-	64	C8	C8
	ADTG_1		7	7	7	85	E1	E1
	ADTG_2		23	18	13	96	J1	J1
	ADTG_3		114	94	74	72	B5	C4
	ADTG_4		81	-	-	-	-	F10
	ADTG_5		80	70	-	48	E11	F11
	ADTG_6		17	12	12	90	F3	G3
	ADTG_7		35	30	-	8	L3	M3
	ADTG_8		110	-	-	-	-	A6
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	62	52	41	30	L13	L12
	AN01		63	53	42	31	L12	K12
	AN02		64	54	43	32	K13	K11
	AN03		65	55	44	33	K12	J12
	AN04		66	56	45	34	J13	J11
	AN05		67	57	46	35	J12	J10
	AN06		68	58	47	36	J11	H12
	AN07		69	59	48	37	H12	H11
	AN08		74	64	53	42	H11	H10
	AN09		75	65	54	43	G12	G12
	AN10		76	66	55	44	G11	G11
	AN11		77	67	56	45	F12	G10
	AN12		78	68	-	46	F11	F13
	AN13		79	69	-	47	E12	F12
	AN14		80	70	-	48	E11	F11
	AN15		86	71	57	49	D13	D13
	AN16		87	72	58	50	D12	D12
	AN17		88	73	59	51	C13	D11
	AN18		89	74	-	52	C12	C12
	AN19		97	82	67	60	B9	C9
	AN20		98	83	-	61	C9	B9
	AN21		99	84	-	62	A8	A9
	AN22		100	85	-	63	B8	D8
	AN23		101	86	-	64	C8	C8
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	32	27	-	5	N2	N2
	TIOA0_1		24	19	14	97	J2	J2
	TIOA0_2		99	84	-	62	A8	A9
	TIOB0_0	Base timer ch.0 TIOB pin	37	32	22	10	L5	K5
	TIOB0_1		14	9	9	87	E3	F4
	TIOB0_2		100	85	-	63	B8	D8
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	33	28	-	6	N3	L2
	TIOA1_1		25	20	15	98	J3	J3
	TIOA1_2		5	5	5	83	D1	D2
	TIOB1_0	Base timer ch.1 TIOB pin	47	42	32	20	L7	L7
	TIOB1_1		15	10	10	88	F1	G1
	TIOB1_2		6	6	6	84	D2	D3
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	34	29	-	7	M3	N3
	TIOA2_1		26	21	16	99	K1	J4
	TIOA2_2		116	96	76	74	B3	B3
	TIOB2_0	Base timer ch.2 TIOB pin	48	43	33	21	L8	K7
	TIOB2_1		16	11	11	89	F2	G2
	TIOB2_2		115	95	75	73	B4	B4

Calculation method of power dissipation (Pd)

The power dissipation is shown in the following formula.

$Pd = V_{CC} \times I_{CC} + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (-I_{OH}))$

I_{OL}: "L" level output current
I_{OH}: "H" level output current
V_{OL}: "L" level output voltage
V_{OH}: "H" level output voltage

I_{CC} is a current consumed in device.
It can be analyzed as follows.

$I_{CC} = I_{CC}(INT) + \Sigma I_{CC}(IO)$

$I_{CC}(INT)$: Current consumed in internal logic and memory, etc. through regulator
$\Sigma I_{CC}(IO)$: Sum of current (I/O switching current) consumed in output pin

For I_{CC} (INT), it can be anticipated by "(1) Current Rating" in "3. DC Characteristics" (This rating value does not include I_{CC} (IO) for a value at pin fixed).
For Icc (IO), it depends on system used by customers.
The calculation formula is shown below.

$I_{CC}(IO) = (C_{INT} + C_{EXT}) \times V_{CC} \times fsw$

C_{INT}: Pin internal load capacitance
C_{EXT}: External load capacitance of output pin
f_{SW}: Pin switching frequency

Parameter	Symbol	Conditions	Capacitance value
Pin internal load capacitance	C_{INT}	4mA type	1.93pF
		8mA type	3.45pF
		12mA type	3.42pF

Calculate I_{CC} (Max) as follows when the power dissipation can be evaluated by yourself.

1. Measure current value I_{CC} (Typ) at normal temperature (+25°C).
2. Add maximum leak current value I_{CC} (leak_max) at operating on a value in (1).

$I_{CC}(Max) = I_{CC}(Typ) + I_{CC}(leak\_max)$

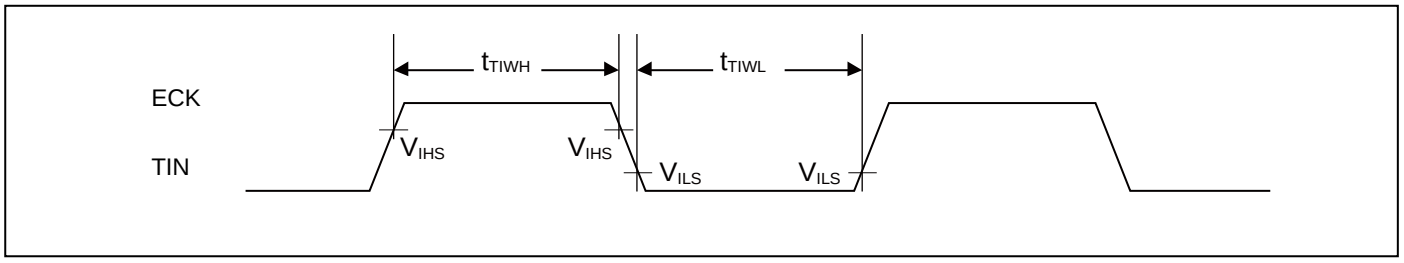
Parameter	Symbol	Conditions	Current value
Maximum leak current at operating	I_{CC}(leak_max)	Tj = +125°C	45.5mA
		Tj = +105°C	26.8mA
		Tj = +85°C	16.2mA

12.4.10 Base Timer Input Timing

Timer input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

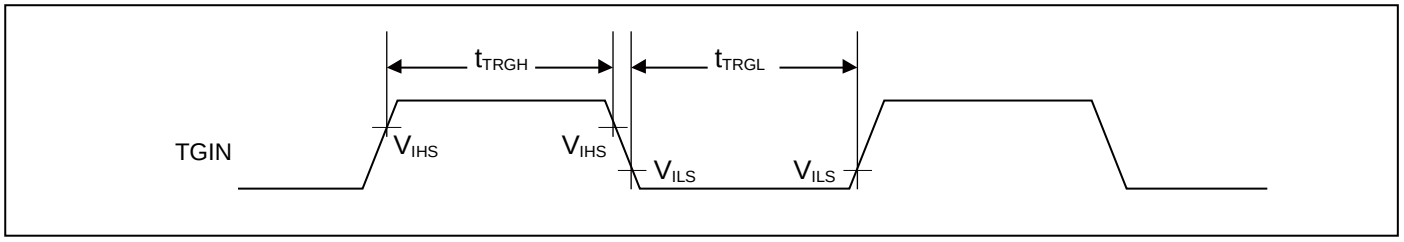
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

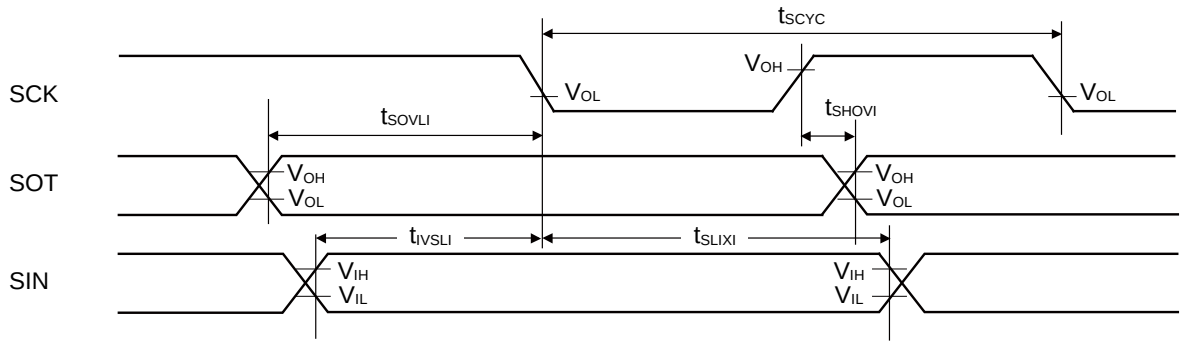
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



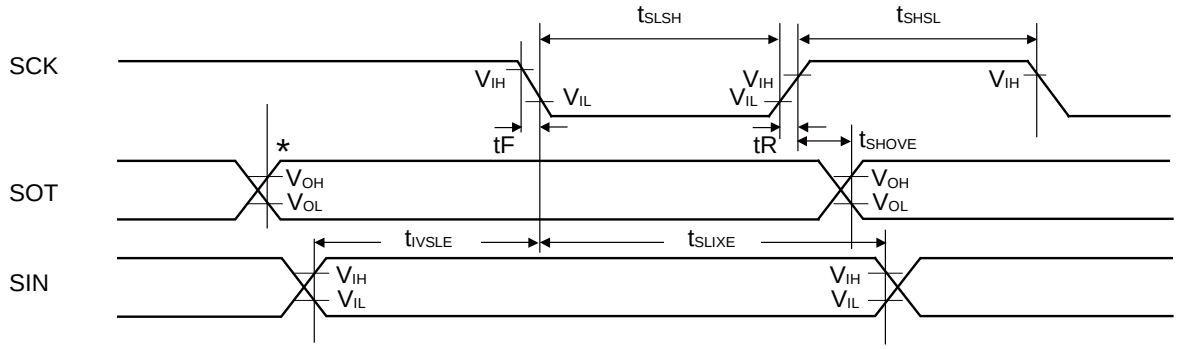
Note:

t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which the Base Timer is connected to, see “Block Diagram” in this datasheet.



MS bit = 0



MS bit = 1

*: Changes when writing to TDR register

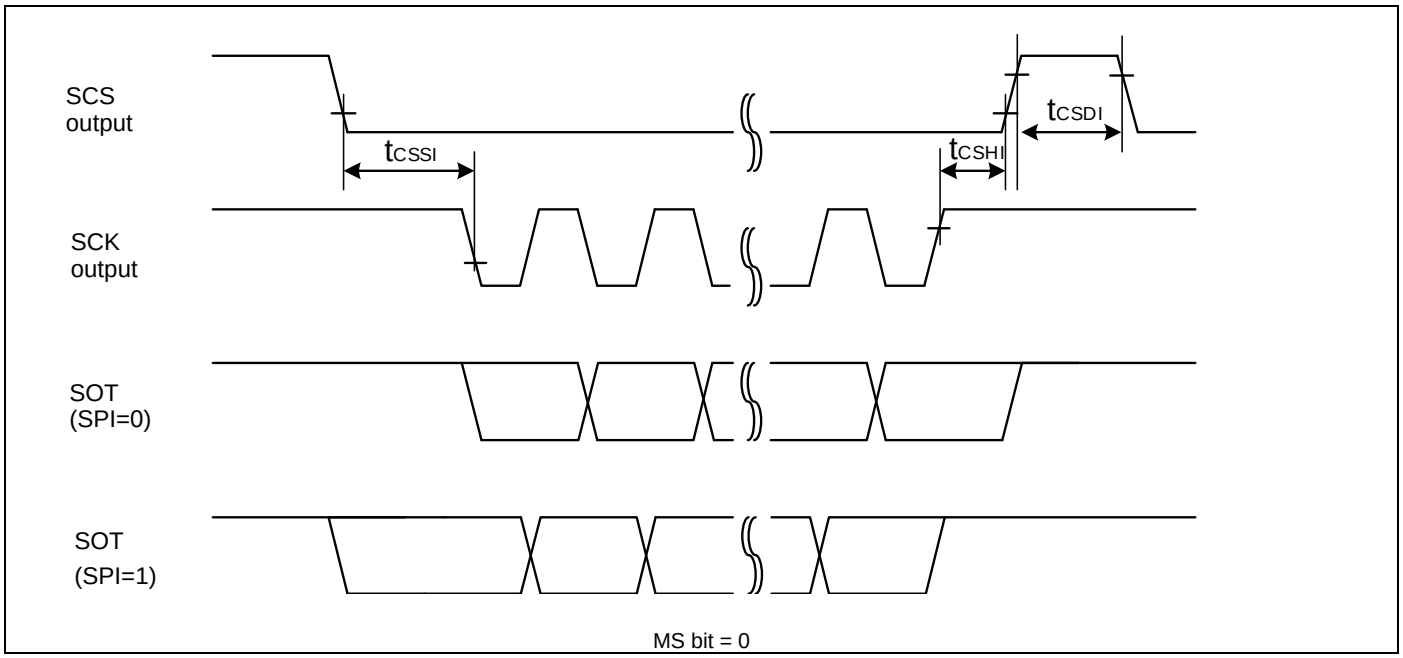
Synchronous serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

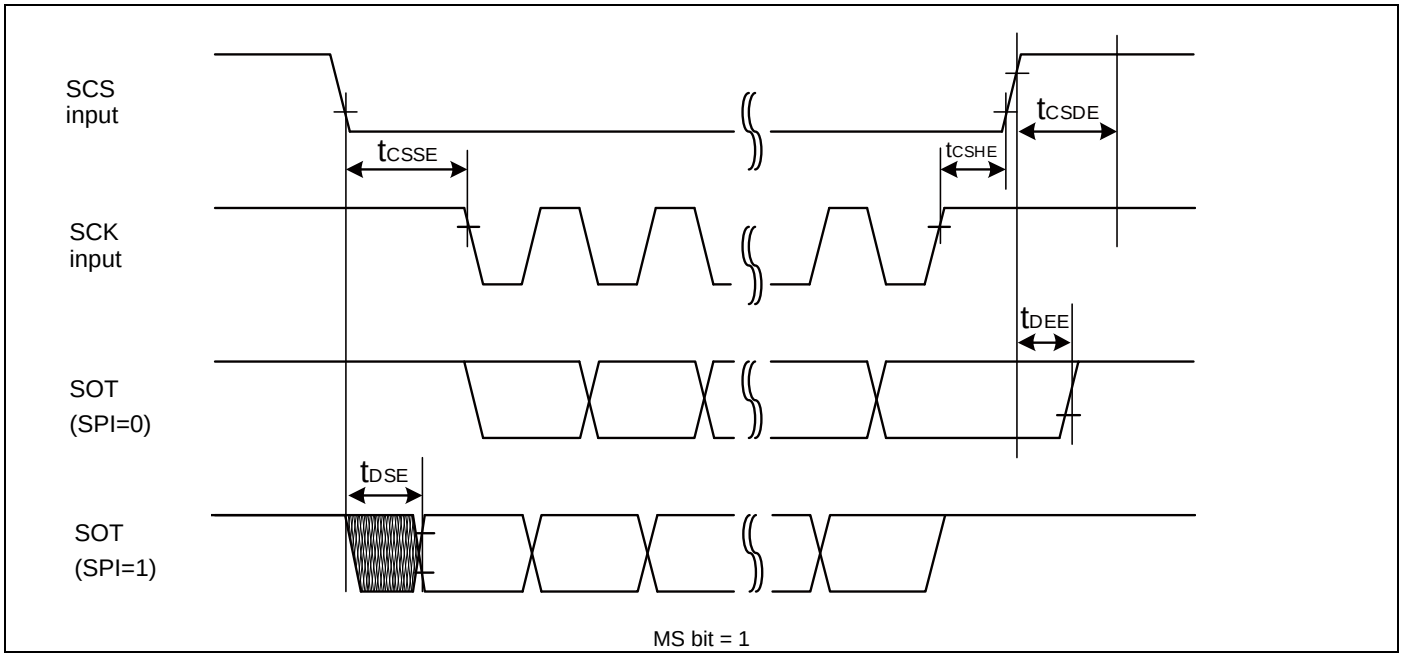
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

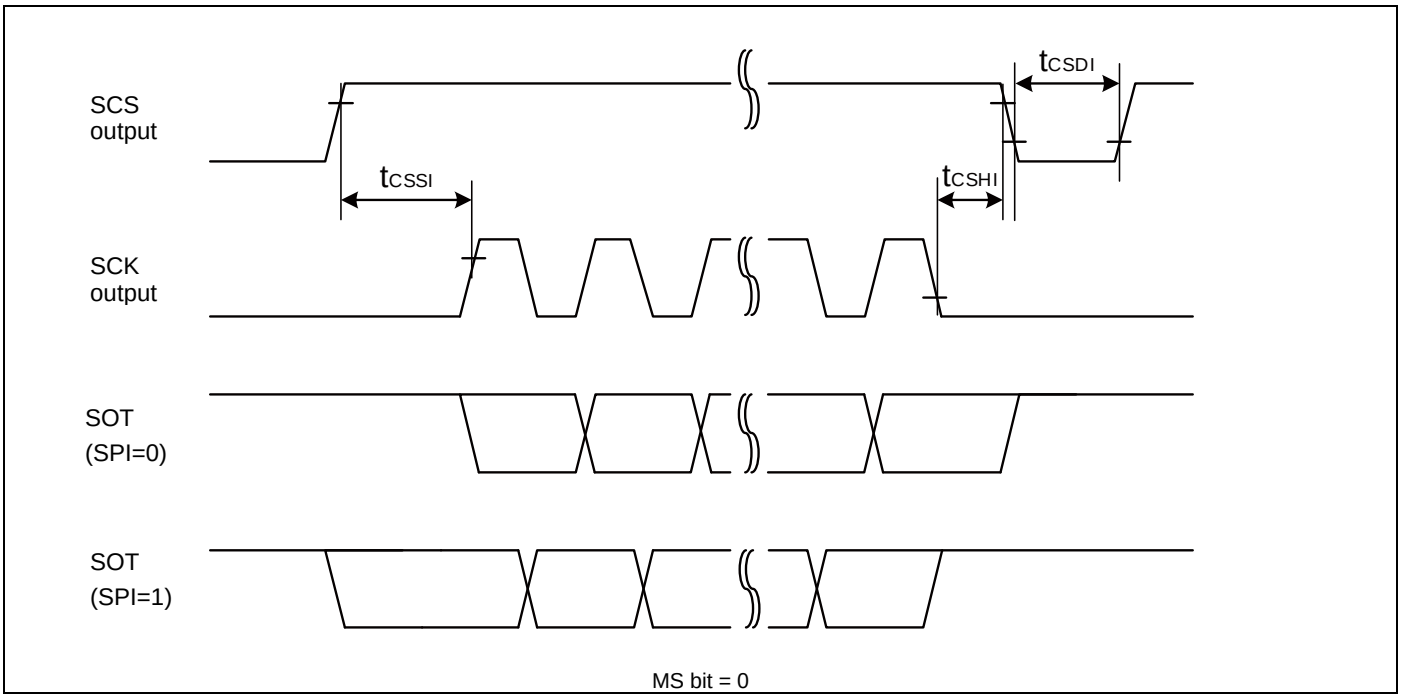
- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30pF.*



MS bit = 0



MS bit = 1



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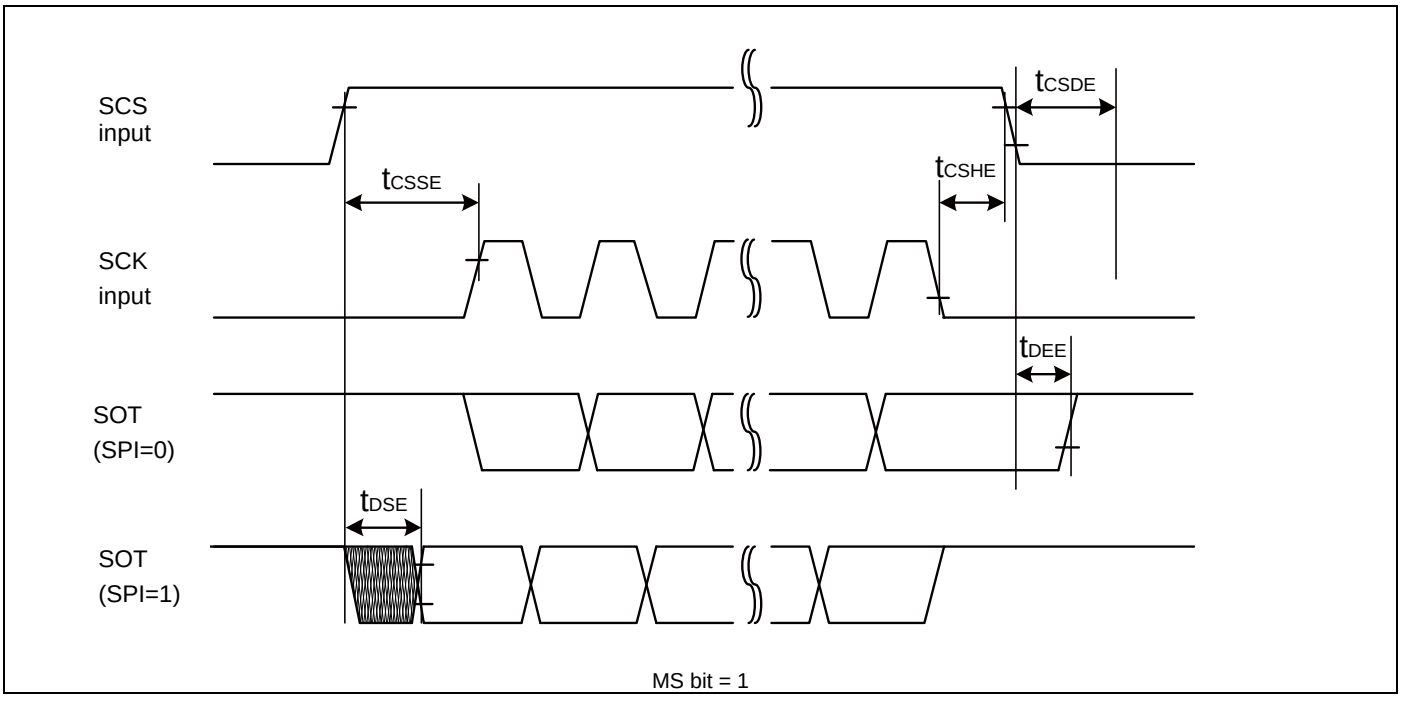
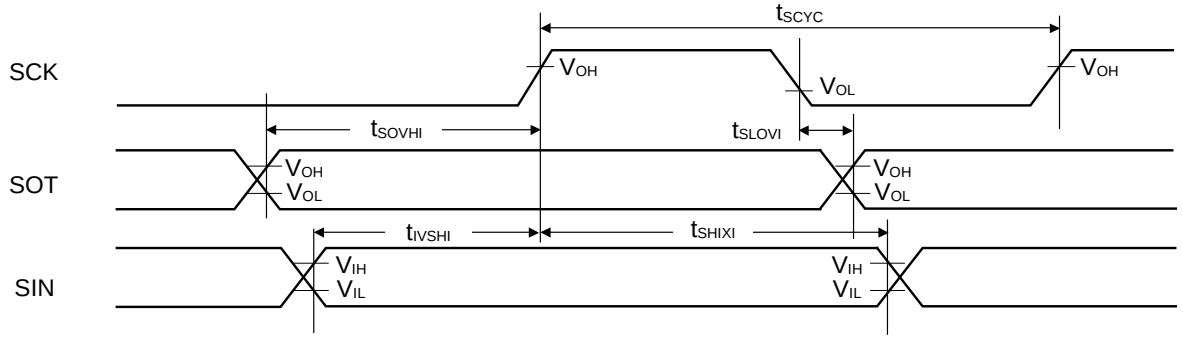
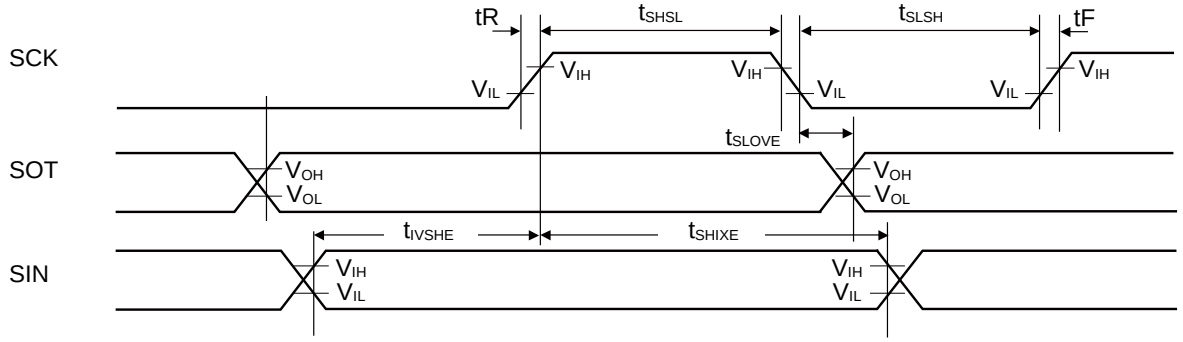


MS bit = 1



MS bit = 0



MS bit = 1

When using high-speed synchronous serial chip select (SCINV = 0, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↓→SCK↓setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↓→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

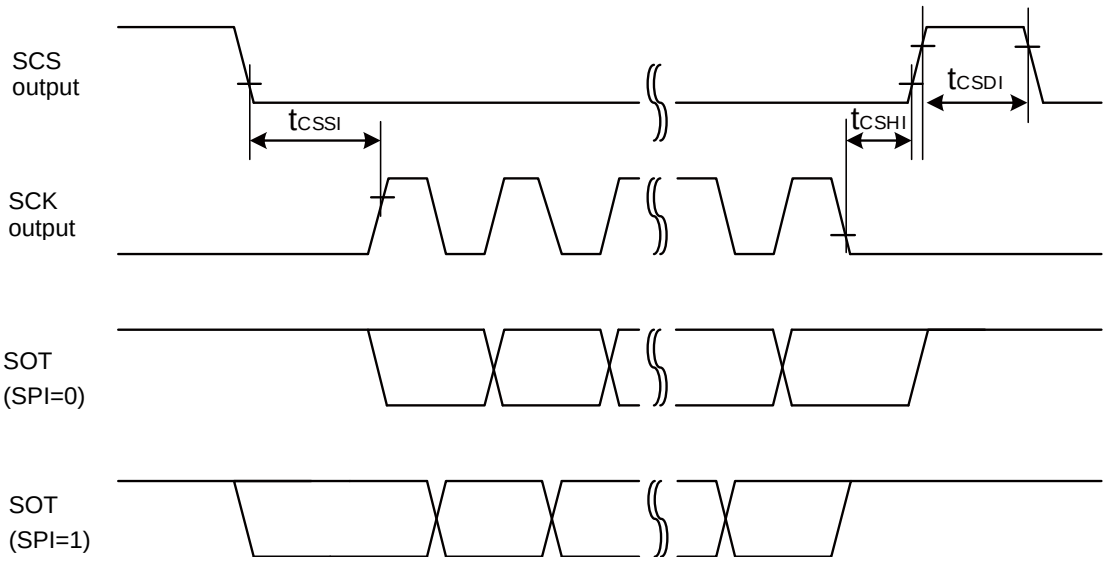
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

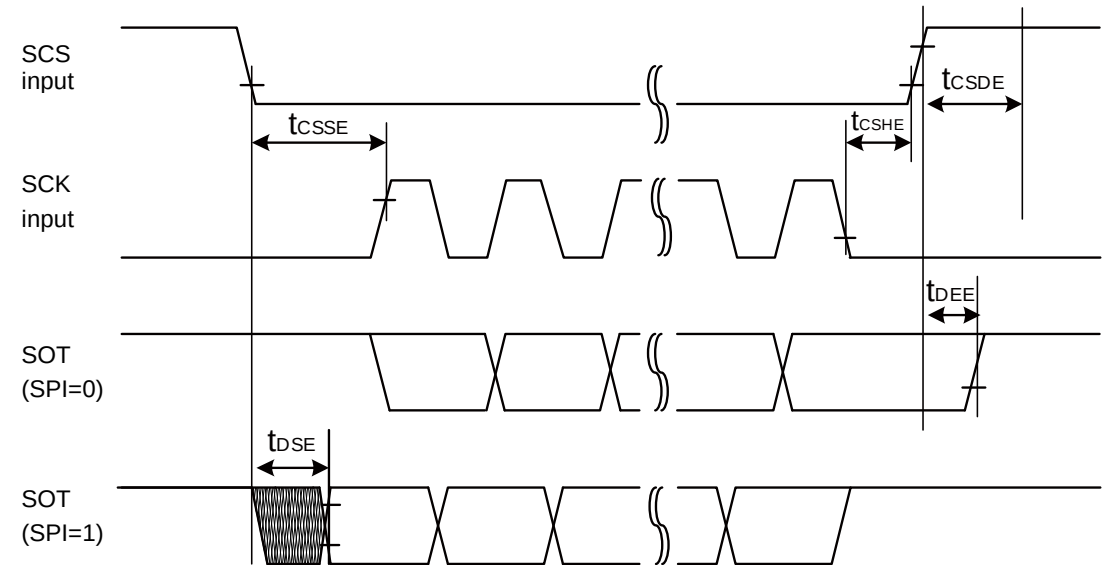
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

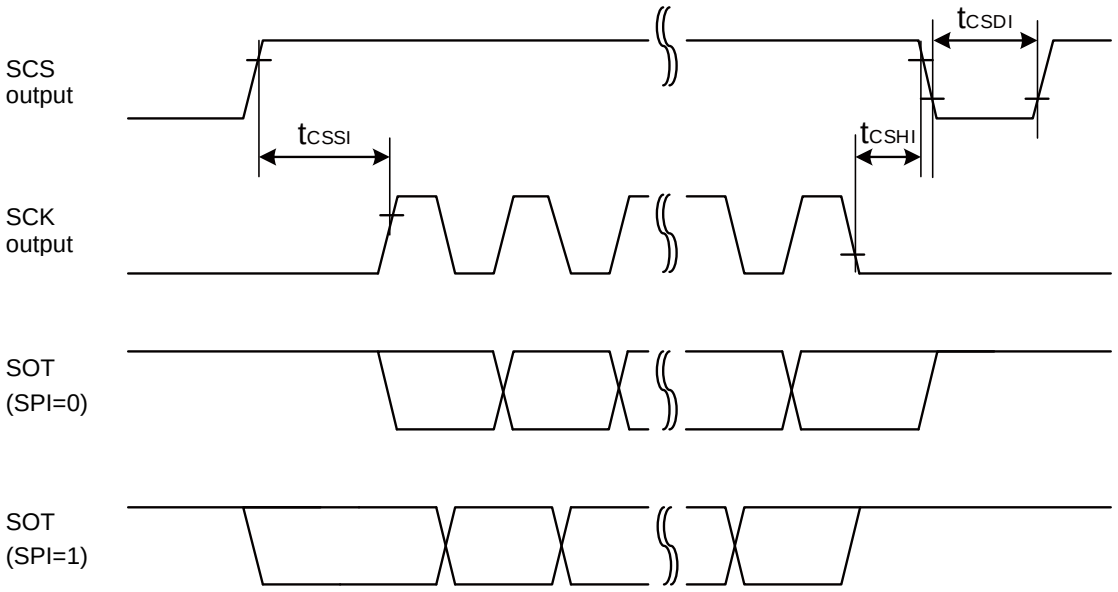
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM4 Family Peripheral Manual".*
- *When the external load capacitance C_L = 30pF.*



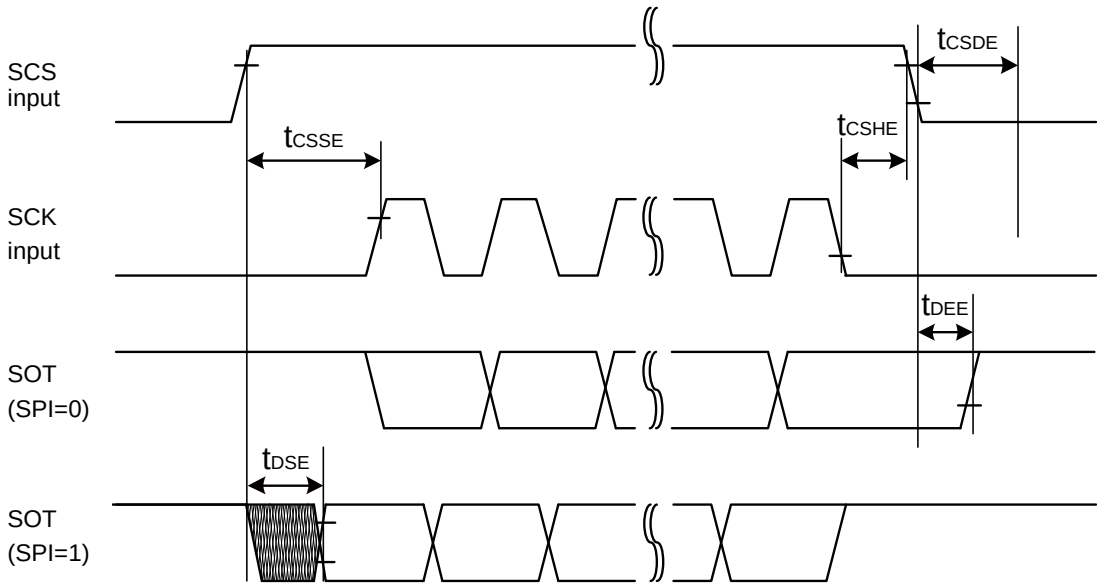
MS bit = 0



MS bit = 1



MS bit = 0



MS bit = 1

Fast-mode Plus (Fm+)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Fast-mode Plus (Fm+)*6		Unit	Remarks
			Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30pF, R = (V_p/I_{OL})*1	0	1000	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		0.26	-	µs	
SCL clock "L" width	t_{LOW}		0.5	-	µs	
SCL clock "H" width	t_{HIGH}		0.26	-	µs	
SCL clock frequency	t_{SUSTA}		0.26	-	µs	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDDAT}		0	0.45*2, *3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		50	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		0.26	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		0.5	-	µs	
Noise filter	t_{SP}	60MHz ≤ t_{CYCP}<80MHz	6 t_{CYCP}*4	-	ns	*5
		80MHz ≤ t_{CYCP}<100MHz	8 t_{CYCP}*4	-	ns	
		100MHz ≤ t_{CYCP}<120MHz	10 t_{CYCP}*4	-	ns	
		120MHz ≤ t_{CYCP}<140MHz	12 t_{CYCP}*4	-	ns	
		140MHz ≤ t_{CYCP}<160MHz	14 t_{CYCP}*4	-	ns	
		160MHz ≤ t_{CYCP}<180MHz	16 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

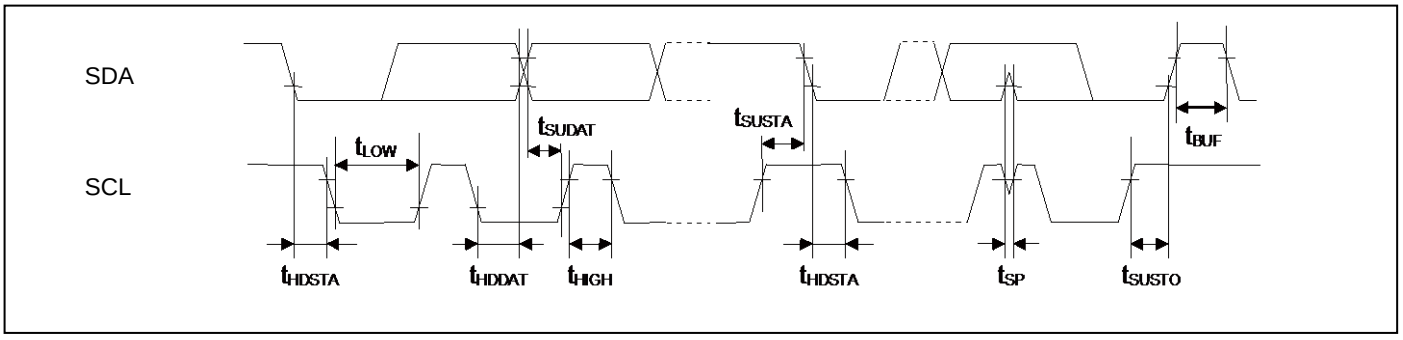
*2: The maximum t_{HDDAT} must satisfy that it does not extend at least "L" period (t_{LOW}) of device's SCL signal.

*3: A Fast-mode I^2C bus device can be used on a Standard-mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I^2C is connected to, see “Block Diagram” in this data sheet.
To use Fast-mode Plus (Fm+), set the peripheral bus clock at 64 MHz or more.

*5: The noise filter time can be changed by register settings.
Change the number of the noise filter steps according to APB bus clock frequency.

*6: When using Fast-mode Plus (Fm+), set the I/O pin to the mode corresponding to I^2C Fm+ in the EPFR register.
See “Chapter: I/O Port” in “FM4 Family Peripheral Manual” for the details.



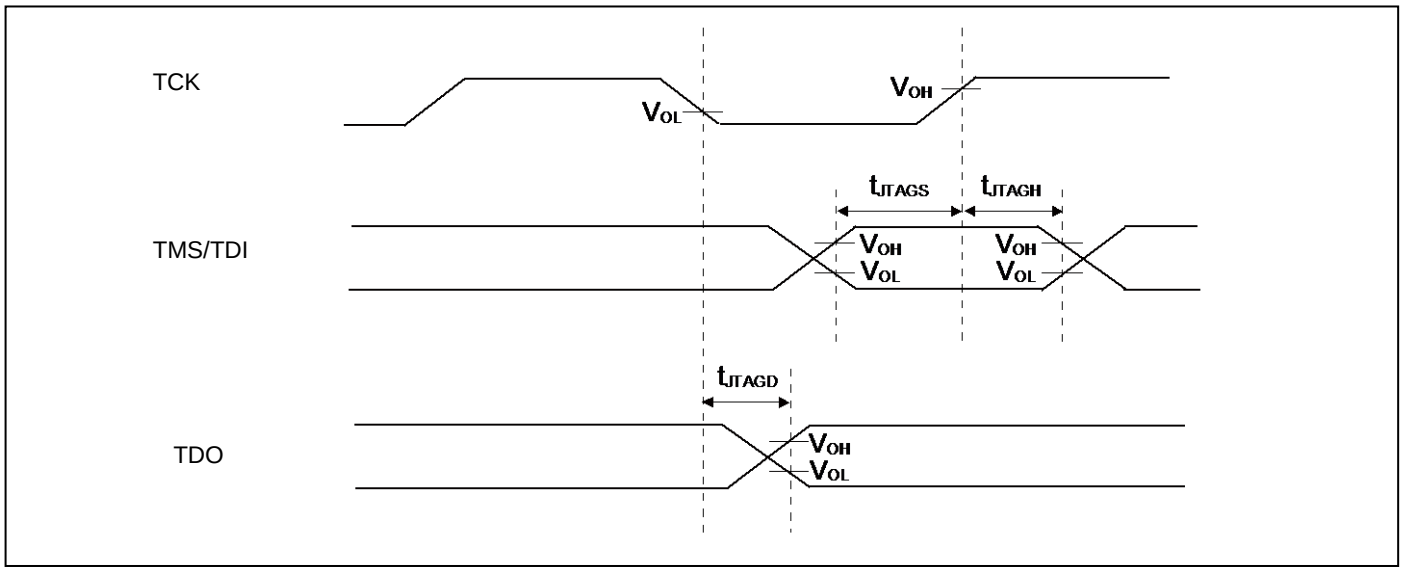
12.4.17 JTAG Timing

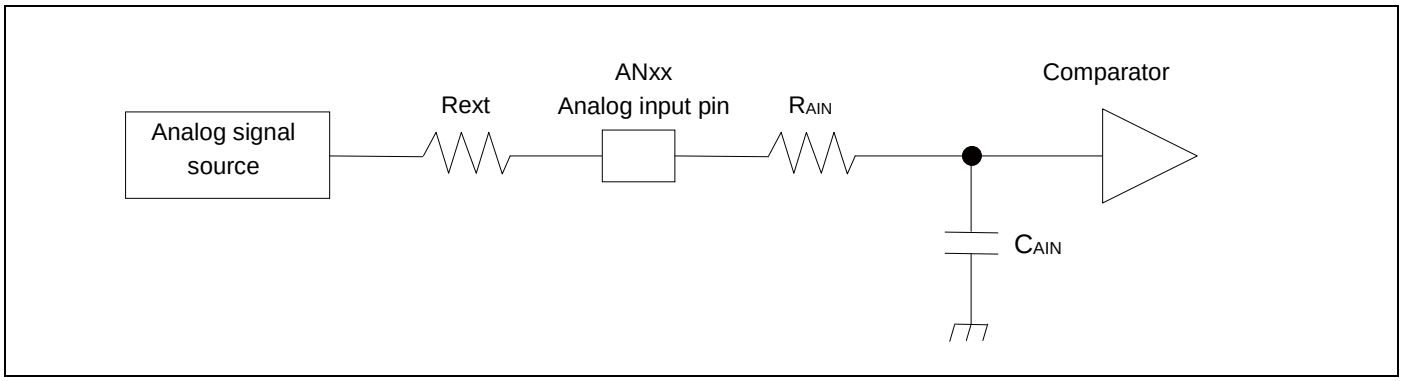
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 4.5V$	15	-	ns	
			$V_{CC} < 4.5V$				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 4.5V$	15	-	ns	
			$V_{CC} < 4.5V$				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 4.5V$	-	25	ns	
			$V_{CC} < 4.5V$	-	45		

Note:

- *When the external load capacitance C_L = 30pF.*





(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

Ts: Sampling time

R_{AIN}: Input resistance of A/D = 1.2kΩ at 4.5V ≤ AV_{CC} ≤ 5.5V

Input resistance of A/D = 1.8kΩ at 2.7V ≤ AV_{CC} ≤ 4.5V

C_{AIN}: Input capacity of A/D = 12.05pF at 2.7V ≤ AV_{CC} ≤ 5.5V

Rext: Output impedance of external circuit

(Equation 2) $Tc = Tcck \times 14$

Tc: Compare time

Tcck: Compare clock cycle

12.6 12-bit D/A Converter

Electrical Characteristics for the D/A Converter

(V_{CC} = AV_{CC} = 2.7Vto5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	12	bit	
Conversion time	tc20		0.56	0.69	0.81	µs	Load 20pF
	tc100		2.79	3.42	4.06	µs	Load 100pF
Integral Nonlinearity*	INL		- 16	-	+ 16	LSB	
Differential Nonlinearity*	DNL		- 0.98	-	+ 1.5	LSB	
Output voltage offset	V_{OFF}		-	-	10.0	mV	When setting 0x000
			- 20.0	-	+ 1.4	mV	When setting 0xFFF
Analog output impedance	R_O		3.10	3.80	4.50	kΩ	D/A operation
			2.0	-	-	MΩ	When D/A stop
Power supply current*	IDDA	AVCC	260	330	410	µA	D/A 1unit operation AV_{CC} = 3.3V
			400	510	620	µA	D/A 1unit operation AV_{CC} = 5.0V
	IDSA		-	-	14	µA	When D/A stop

*: During no load

12.10.2 Recovery cause: Reset

The time from reset release to the program operation start is shown.

Recovery count time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	Trcnt	155	266	µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		155	266	µs	
Low-speed CR timer mode		315	567	µs	
Sub timer mode		315	567	µs	
RTC mode stop mode		315	567	µs	
Deep standby RTC mode with RAM retention		336	667	µs	without RAM retention
Deep standby stop mode with RAM retention				µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of standby recovery operation (when in INITX recovery)