Cypress Semiconductor Corp - MB9BF168NPMC-G-JNE2 Datasheet

Welcome to E-XFL.COM

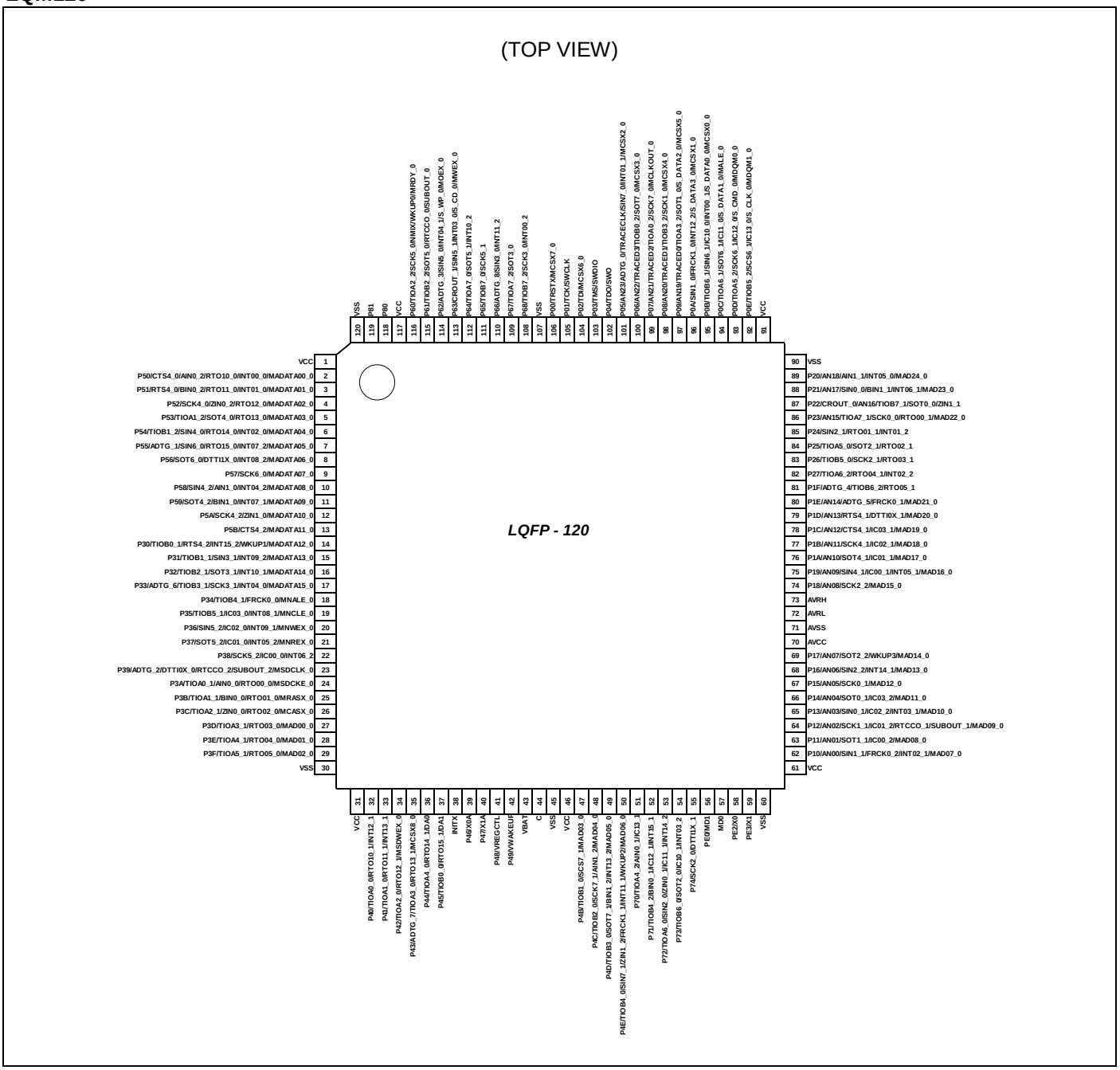
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1.03125MB (1.03125M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9bf168npmc-g-jne2

LQM120



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
16	11	11	89	F2	G2	P32 TIOB2_1 SOT3_1 (SDA3_1) INT10_1	N	K
-					-	MADATA09_0		
16	-	-	-	-	G2	MADATA14_0		
17	12	12	90	F3	G3	P33 ADTG_6 TIOB3_1 SCK3_1 (SCL3_1) INT04_0	N	K
-					-	MADATA10_0		
17	-	-	-	-	G3	MADATA15_0		
18	13	-	91	G1	G4	P34 TIOB4_1 FRCK0_0	E	I
-					-	MADATA11_0		
18	-	-	-	-	G4	MNALE_0		
19	14	-	92	G2	H1	P35 TIOB5_1 IC03_0 INT08_1	E	K
-					-	MADATA12_0		
19	-	-	-	-	H1	MNCLE_0		

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
51	-	-	-	-	K8	P70 TIOA4_2 AIN0_1 IC13_1	E	I
52	-	-	-	-	L9	P71 TIOB4_2 BIN0_1 IC12_1 INT15_1	E	K
53	-	-	-	-	K9	P72 TIOA6_0 SIN2_0 ZIN0_1 IC11_1 INT14_2	E	K
54	-	-	-	-	M10	P73 TIOB6_0 SOT2_0 (SDA2_0) IC10_1 INT03_2	E	K
55	-	-	-	-	L10	P74 SCK2_0 (SCL2_0) DTTI1X_1	E	I
56	46	36	24	M10	N10	PE0 MD1	C	E
57	47	37	25	M11	M11	MD0	J	D
58	48	38	26	N11	N11	PE2 X0	A	A
59	49	39	27	N12	N12	PE3 X1	A	B
60	50	40	28	N13	N13	VSS	-	-
61	51	-	29	M13	M13	VCC	-	-
62	52	41	30	L13	L12	P10 AN00 SIN1_1 FRCK0_2 INT02_1 MAD07_0	F	M
63	53	42	31	L12	K12	P11 AN01 SOT1_1 (SDA1_1) IC00_2 MAD08_0	F	L

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP120	LQFP100	LQFP80	QFP100	BGA112	BGA144			
83	-	-	-	-	E12	P26 TIOB5_0 SCK2_1 (SCL2_1) RTO03_1 (PPG02_1)	E	I
84	-	-	-	-	E11	P25 TIOA5_0 SOT2_1 (SDA2_1) RTO02_1 (PPG02_1)	E	I
85	-	-	-	-	E10	P24 SIN2_1 RTO01_1 (PPG00_1) INT01_2	E	K
86	71	57 -	49	D13	D13	P23 AN15 TIOA7_1 SCK0_0 (SCL0_0) RTO00_1 (PPG00_1) MAD22_0	F	L
87	72	58 -	50	D12	D12	P22 CROUT_0 AN16 TIOB7_1 SOT0_0 (SDA0_0) ZIN1_1	F	L
88	73	59 - 59 -	51	C13	D11	P21 AN17 SIN0_0 BIN1_1 INT06_1 MAD23_0	F	M
89	74	-	52	C12	C12	P20 AN18 AIN1_1 INT05_0 MAD24_0	F	M
90	75	60	53	A13	A13	VSS	-	-
91	76	61	54	B13	A12	VCC	-	-

7. Handling Devices

Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each POWER pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between VCC and VSS near this device.

Power supply pins

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the VCC power supply voltage. As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard VCC value, and the transient fluctuation rate does not exceed 0.1 V/µs at a momentary fluctuation such as switching the power supply.

Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Sub crystal oscillator

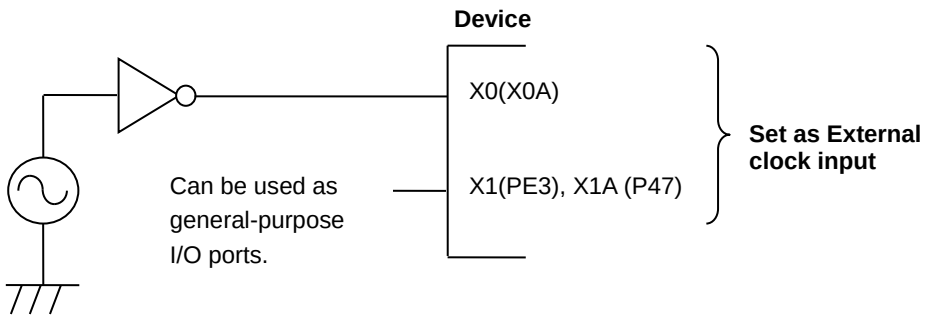
This series sub oscillator circuit is low gain to keep the low current consumption.
The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

- Surface mount type
  - Size: More than 3.2 mm × 1.5 mm
  - Load capacitance: Approximately 6 pF to 7 pF
- Lead type
  - Load capacitance: Approximately 6 pF to 7 pF

Using an external clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

● Example of Using an External Clock



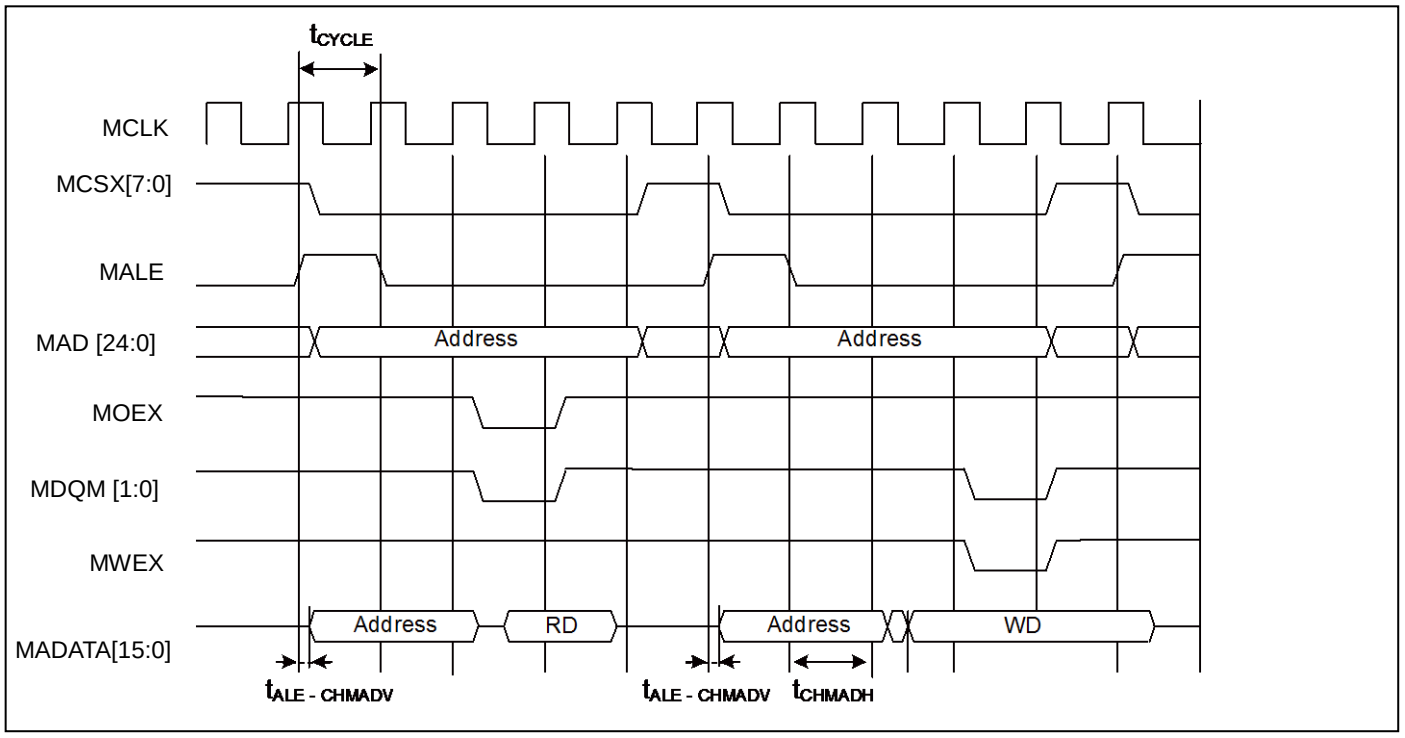
Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MADATA[15:0]	$V_{CC} \geq 4.5V$	0	10	ns
			$V_{CC} < 4.5V$		20	
Multiplexed address hold time	t_{CHMADH}		$V_{CC} \geq 4.5V$	MCLK×n+0	MCLK×n+10	ns
			$V_{CC} < 4.5V$	MCLK×n+0	MCLK×n+20	

Note:

- *When the external load capacitance C_L = 30pF (m = 0 to 15, n = 1 to 16)*



12.4.11 CSIO/UART Timing

Synchronous serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30pF.*

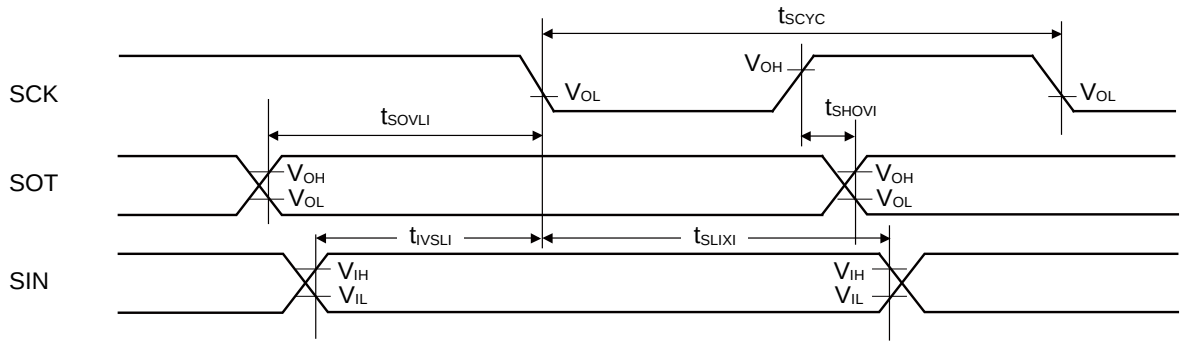
Synchronous serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

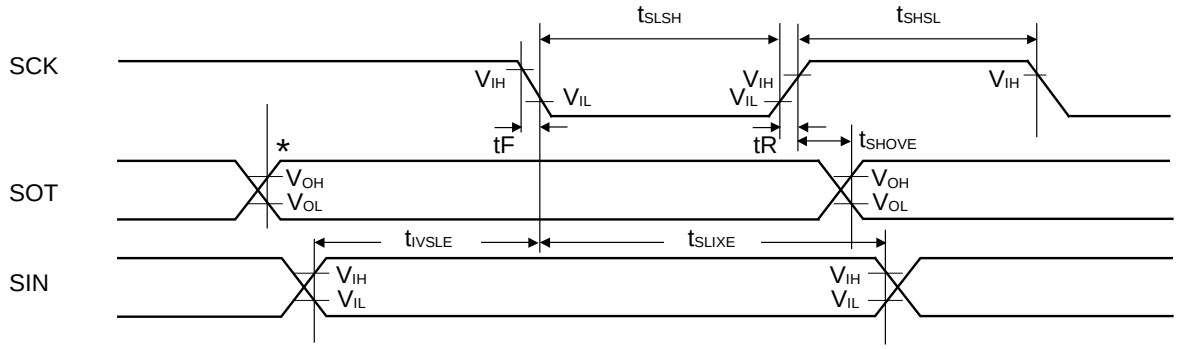
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30pF.*



MS bit = 0



MS bit = 1

*: Changes when writing to TDR register

When using synchronous serial chip select (SCINV = 1, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↑setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↑setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

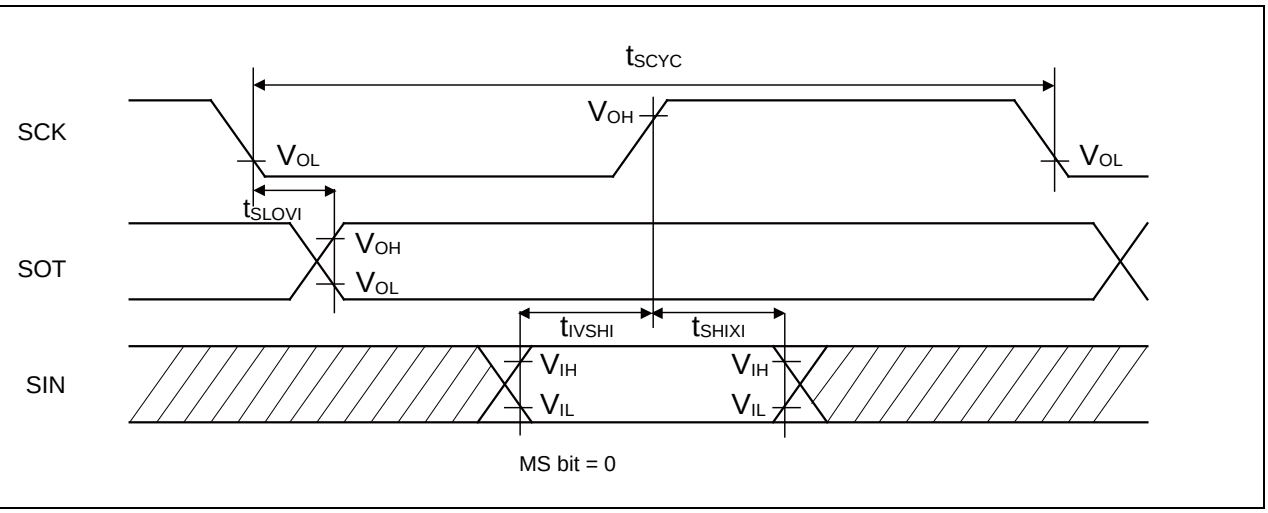
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

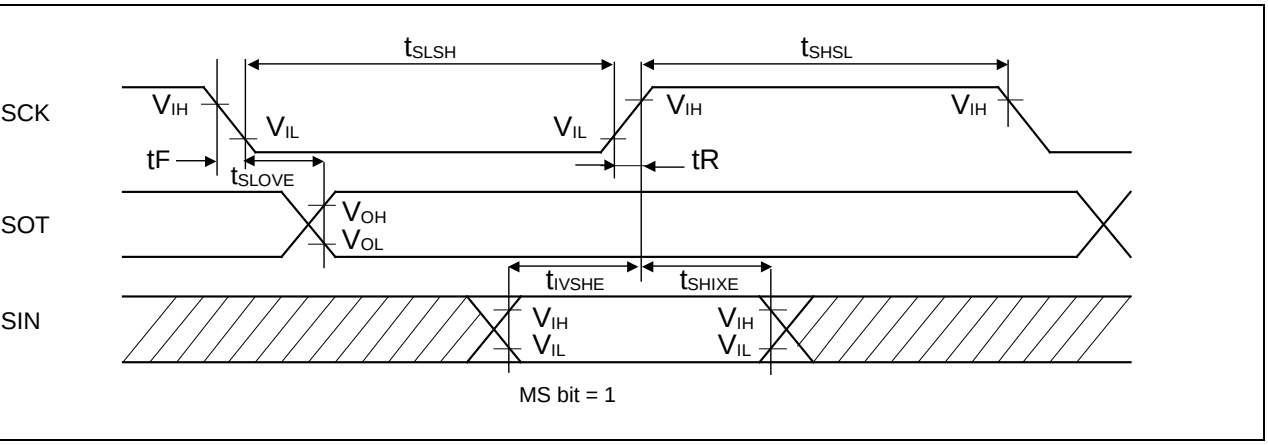
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM4 Family Peripheral Manual".*
- *When the external load capacitance C_L = 30pF.*


tSCYC
SCK
VOH
VOL
VOL
tSLOVI
SOT
VOH
VOL
tIVSHI
tSHIXI
SIN
VIH
VIL
VIH
VIL
MS bit = 0


tSLSH
tSHSL
SCK
VIH
VIL
VIL
VIH
VIH
tF
tSLOVE
tR
SOT
VOH
VOL
tIVSHE
tSHIXE
SIN
VIH
VIL
VIH
VIL
MS bit = 1

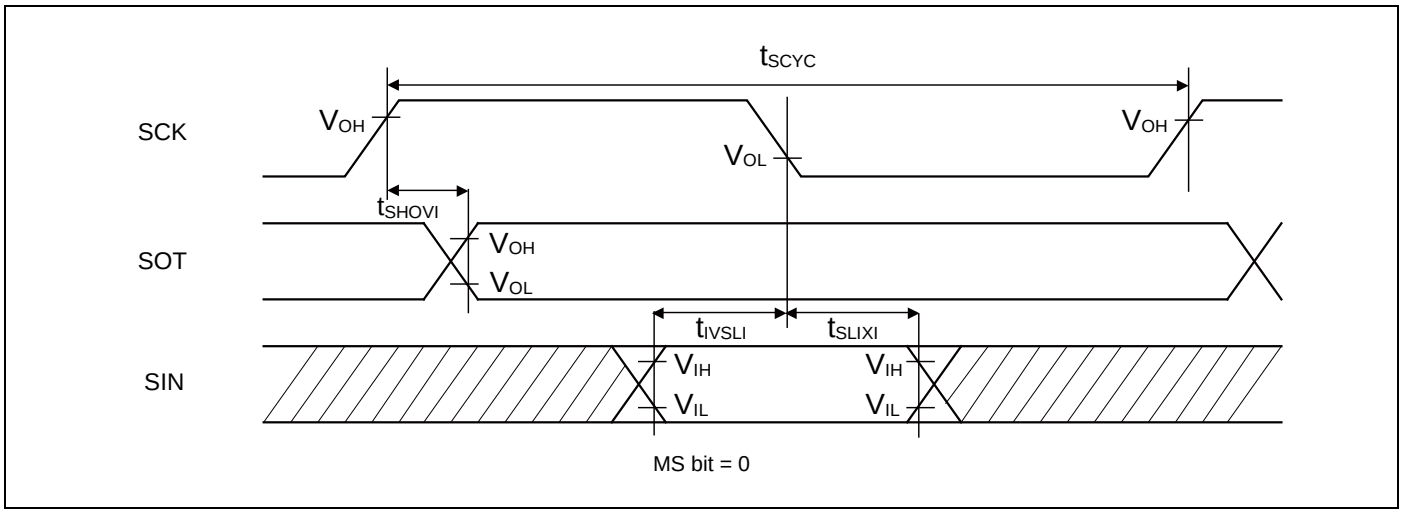
High-speed synchronous serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

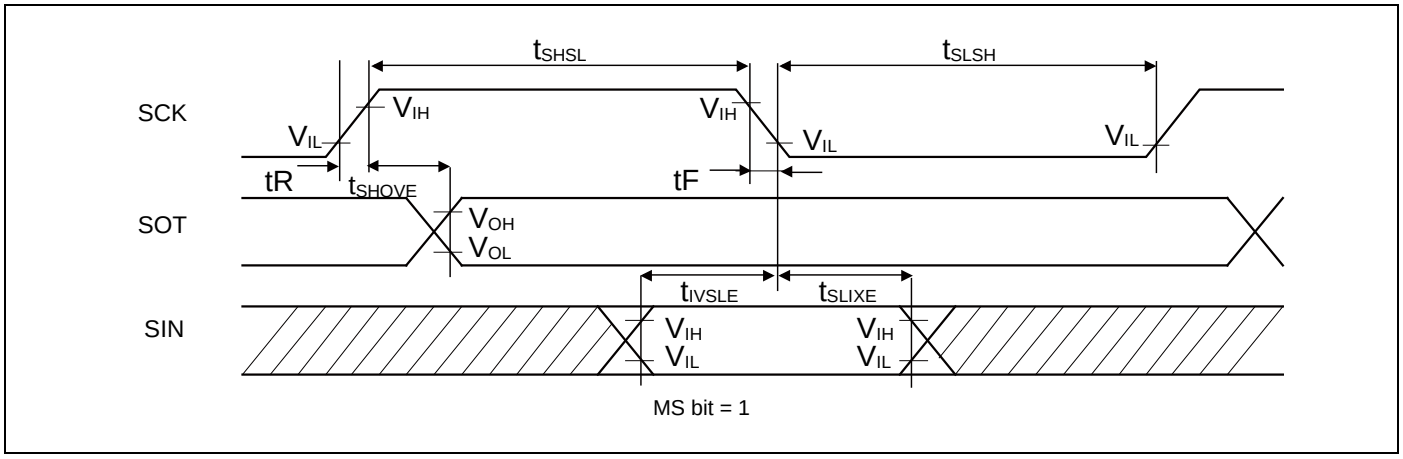
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.
- *These characteristics only guarantee the following pins.*
  - *No chip select: SIN4_1, SOT4_1, SCK4_1*
  - *Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1*
- *When the external load capacitance C_L = 30pF. (For *, when C_L = 10pF)*



MS bit = 0



MS bit = 1

High-speed synchronous serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Internal shift clock operation	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ – 10	-	$2t_{CYCP}$ – 10	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.
- *These characteristics only guarantee the following pins.*
  - *No chip select: SIN4_1, SOT4_1, SCK4_1*
  - *Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1*
- *When the external load capacitance C_L = 30pF. (For *, when C_L = 10pF)*

When using high-speed synchronous serial chip select (SCINV = 1, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↑setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↓→SCK↑setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↓→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM4 Family Peripheral Manual".*
- *When the external load capacitance C_L = 30pF.*

12.10 Standby Recovery Time

12.10.1 Recovery cause: Interrupt/WKUP

The time from recovery cause reception of the internal circuit to the program operation start is shown.

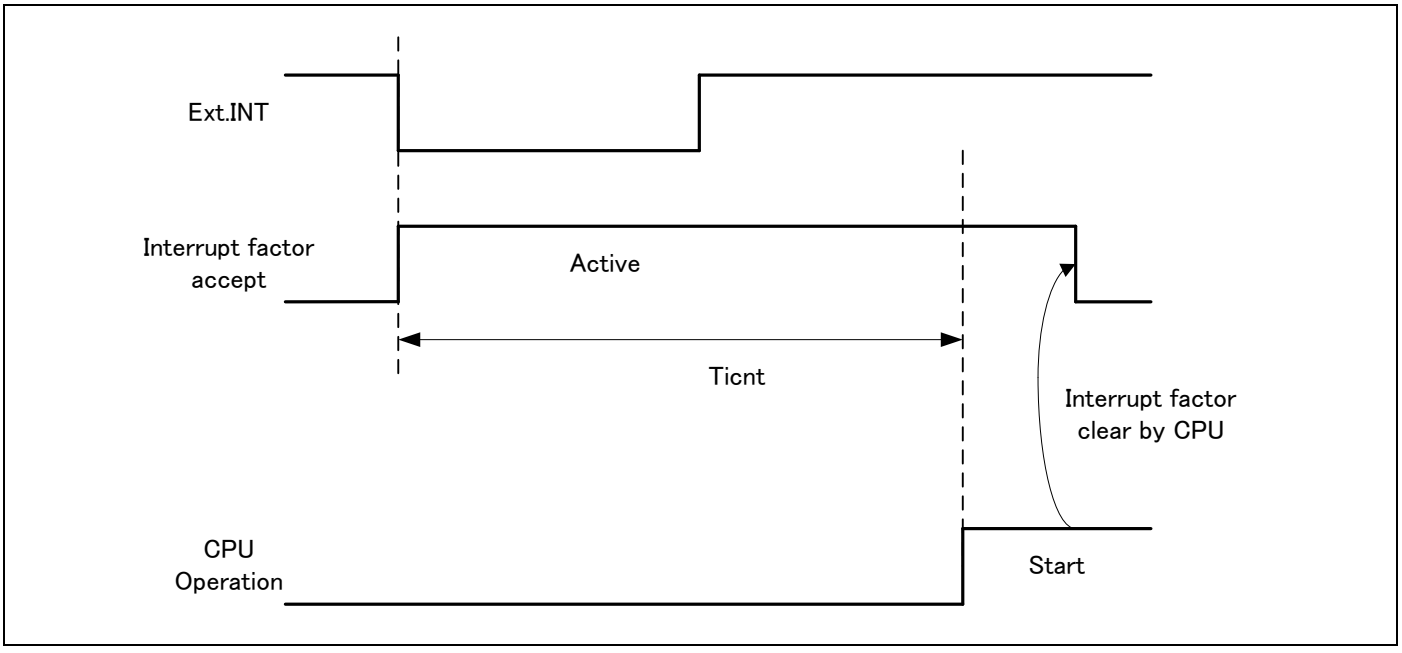
Recovery count time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	Ticnt	HCLK×1		µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		40	80	µs	
Low-speed CR timer mode		450	900	µs	
Sub timer mode		896	1136	µs	
RTC mode stop mode (High-speed CR /Main/PLL run mode return)		316	581	µs	
RTC mode stop mode (Low-speed CR/sub run mode return)		270	540		
Deep standby RTC mode with RAM retention		365	667	µs	without RAM retention
Deep standby stop mode with RAM retention		365	667	µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of standby recovery operation (when in external interrupt recovery*)

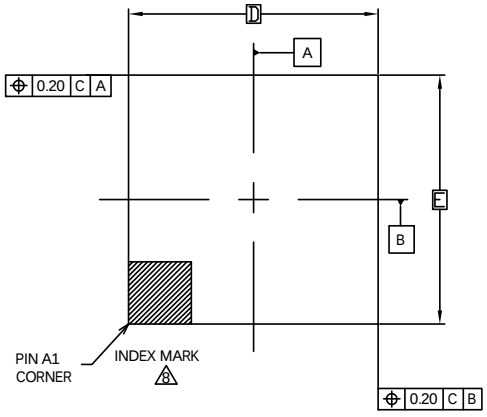


*: External interrupt is set to detecting fall edge.

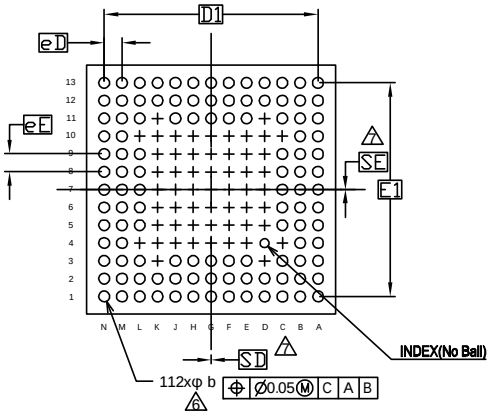
13. Ordering Information

Part Number	Flash	RAM	Package
MB9BF168MPMC-G-JNE2	1 MB	128 KB	Plastic・LQFP (0.5 mm pitch), 80 pin (LQH080)
MB9BF167MPMC-G-JNE2	768 KB	96 KB	
MB9BF166MPMC-G-JNE2	512 KB	64 KB	
MB9BF168MPMC1-G-JNE2	1 MB	128 KB	Plastic・LQFP (0.65 mm pitch), 80 pin (LQJ080)
MB9BF167MPMC1-G-JNE2	768 KB	96 KB	
MB9BF166MPMC1-G-JNE2	512 KB	64 KB	
MB9BF168NPMC-G-JNE2	1 MB	128 KB	Plastic・LQFP (0.5 mm pitch), 100 pin (LQI100)
MB9BF167NPMC-G-JNE2	768 KB	96 KB	
MB9BF166NPMC-G-JNE2	512 KB	64 KB	
MB9BF168RPMC-G-JNE2	1 MB	128 KB	Plastic・LQFP (0.5 mm pitch), 120 pin (LQM120)
MB9BF167RPMC-G-JNE2	768 KB	96 KB	
MB9BF166RPMC-G-JNE2	512 KB	64 KB	
MB9BF168NBGL-GE1	1 MB	128 KB	Plastic・PFBGA (0.5 mm pitch), 112 pin (LDC112)
MB9BF167NBGL-GE1	768 KB	96 KB	
MB9BF166NBGL-GE1	512 KB	64 KB	
MB9BF168RBGL-GK7E1	1 MB	128 KB	Plastic・PFBGA (0.5 mm pitch), 144 pin (LDC144)
MB9BF167RBGL-GK7E1	768 KB	96 KB	
MB9BF166RBGL-GK7E1	512 KB	64 KB	
MB9BF168NPQC-G-JNE2	1 MB	128 KB	Plastic・QFP (0.65 mm pitch), 100 pin (PQH100)
MB9BF167NPQC-G-JNE2	768 KB	96 KB	
MB9BF166NPQC-G-JNE2	512 KB	64 KB	

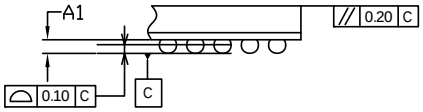
Package Type	Package Code
BGA-112	LDC112



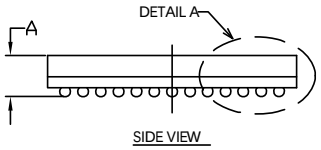
TOP VIEW



BOTTOM VIEW



DETAIL A



SIDE VIEW

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.35
A_1	0.15	0.25	0.35
D		7.00 BSC	
E		7.00 BSC	
D1		6.00 BSC	
E 1		6.00 BSC	
MD		13	
ME		13	
n		112	
Φb	0.20	0.30	0.40
eD		0.50 BSC	
eE		0.50 BSC	
SD / SE		0.00	

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" =0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

PACKAGE OUTLINE, 112 BALL FBGA
7.0X7.0X1.35 MM LDC112 REV**

002-16663 **

15. Major Changes

Spansion Publication Number: DS709-00004

Page	Section	Change Results
-	-	Preliminary → Data Sheet
1	Description	Deleted the following description : The products which are described in this data sheet are placed into TYPE4 product categories in "FM4 Family PERIPHERAL MANUAL".
3	Features Multi-Function Serial Interface [I^2C]	Revised the following description : Fast mode Plus (Fm+) (Max 1000 kbps, only for ch.3 and ch.7) supported →Fast mode Plus (Fm+) (Max 1000 kbps, only for ch.3=ch.A and ch.7=ch.B) supported
7	Features Unique Id	Added new section
9	Product Lineup Function	Added “Unique ID”
51, 52	I/O Circuit Type	Revised the remarks of “Type O, P, Q”
59	Handling Devices Handling When Using Debug Pins	Added new section
60	Block Diagram	Revised the block diagram
72	Electrical Characteristics 2. Recommended Operating Conditions	Revised “Table for package thermal resistance and maximum permissible power”
75 to 80	Electrical Characteristics 3. Dc Characteristics (1) Current Rating	• Revised the value of TBD • Added the note to “ICCVBAT”
85	Electrical Characteristics 4. Ac Characteristics (2) Sub Clock Input Characteristics	Revised the waveform chart
85	Electrical Characteristics 4. Ac Characteristics (3) Built-In Cr Oscillationcharacteristics	• Revised the value of TBD • Revised the table and the note of “Built-in High-speed CR”
144	Electrical Characteristics 5. 12-Bit A/D Converter Electrical Characteristics For The A/D Converter	• Revised the value of TBD • Revised the condition of the electrical characteristics table
147	Electrical Characteristics 6. 12-Bit D/A Converter Electrical Characteristics For The D/A Converter	• Revised the value of TBD • Revised the condition and Remarks of the electrical characteristics table
150	Electrical Characteristics 10. Standby Recovery Time (1) Recovery Cause: Interrupt/Wkup	• Revised the value of TBD • Revised the table of Recovery count time
152	Electrical Characteristics 10. Standby Recovery Time (2) Recovery Cause:Reset	• Revised the value of TBD • Revised the table of Recovery count time

Note: Please see “Document History” about later revised information.