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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	1.03125MB (1.03125M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9bf168rpmc-g-jne2

[UART]

- Full-duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control : Automatically control the transmission by CTS/RTS (only ch.4)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[CSIO]

- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detect function available
- Serial chip select function (ch.6 and ch.7 only)
- Supports high-speed SPI (ch.4 and ch.6 only)
- Data length 5 to 16-bit

[LIN]

- LIN protocol Rev.2.1 supported
- Full-duplex double buffer
- Master/Slave mode supported
- LIN break field generation (can change to 13 to 16-bit length)
- LIN break delimiter generation (can change to 1 to 4-bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[I^2C]

- Standard-mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported
- Fast-mode Plus (Fm+) (Max 1000 kbps, only for ch.3 = ch.A and ch.7 = ch.B) supported

DMA Controller (8 channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System data Transfer Controller) (128 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor system and, following the specified contents of the Descriptor which has already been constructed on the memory, can access directly the memory /peripheral device and performs the data transfer operation.

It supports the software activation, the hardware activation and the chain activation functions.

A/D Converter (Max 24 channels)

[12-bit A/D Converter]

- Successive Approximation type
- Built-in 3 units
- Conversion time: 0.5µs @ 5V
- Priority conversion available (priority at 2levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16steps, for Priority conversion: 4steps)

DA converter (Max 2 channels)

- R-2R type
- 12-bit resolution

Base Timer (Max 8 channels)

Operation mode is selectable from the followings for each channel.

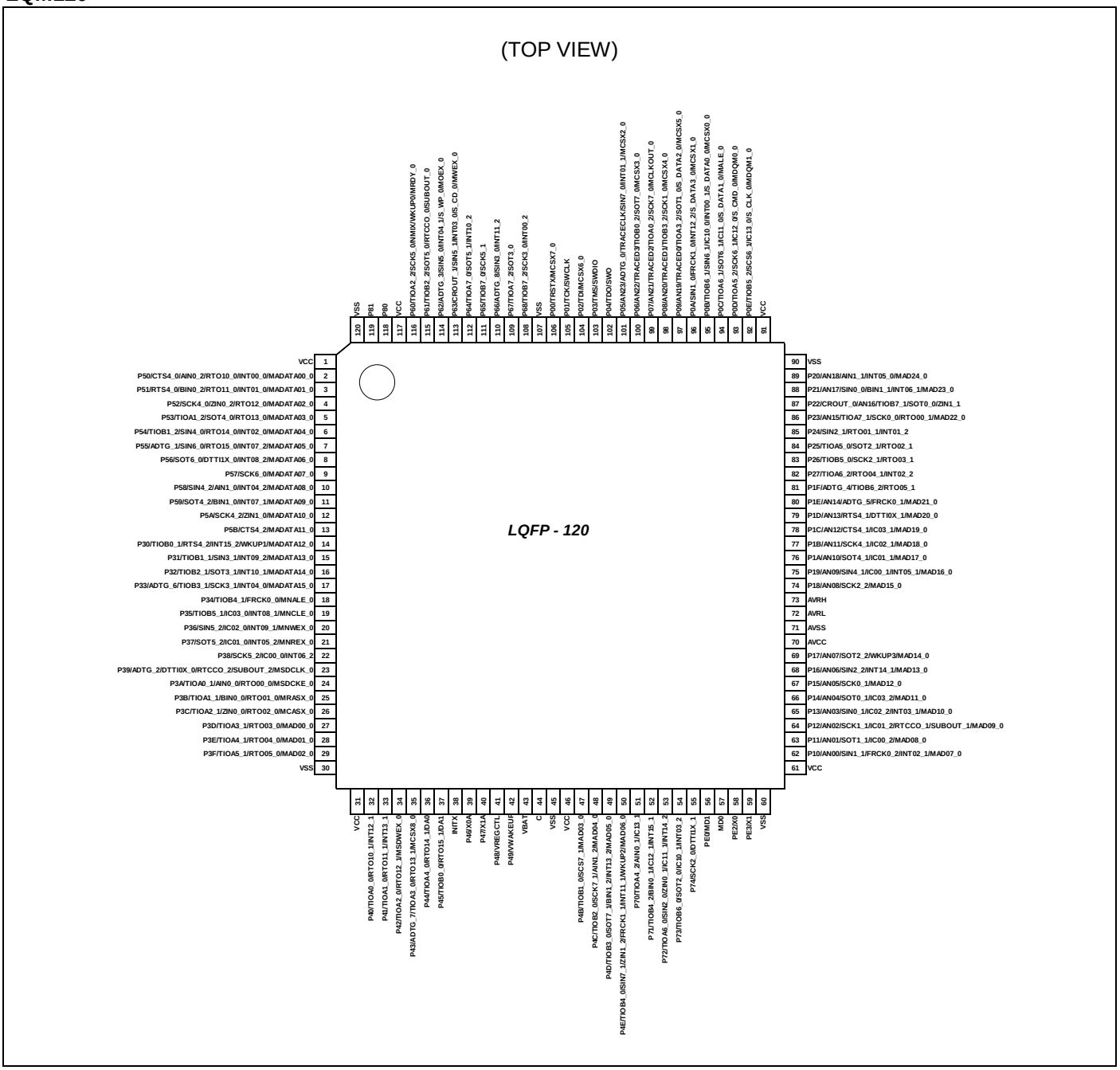
- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 100 high-speed general-purpose I/O ports @ 120pin Package
- Some pin is 5V tolerant I/O.
- See “Pin Description” and “I/O Circuit Type” for the corresponding pins.

LQM120



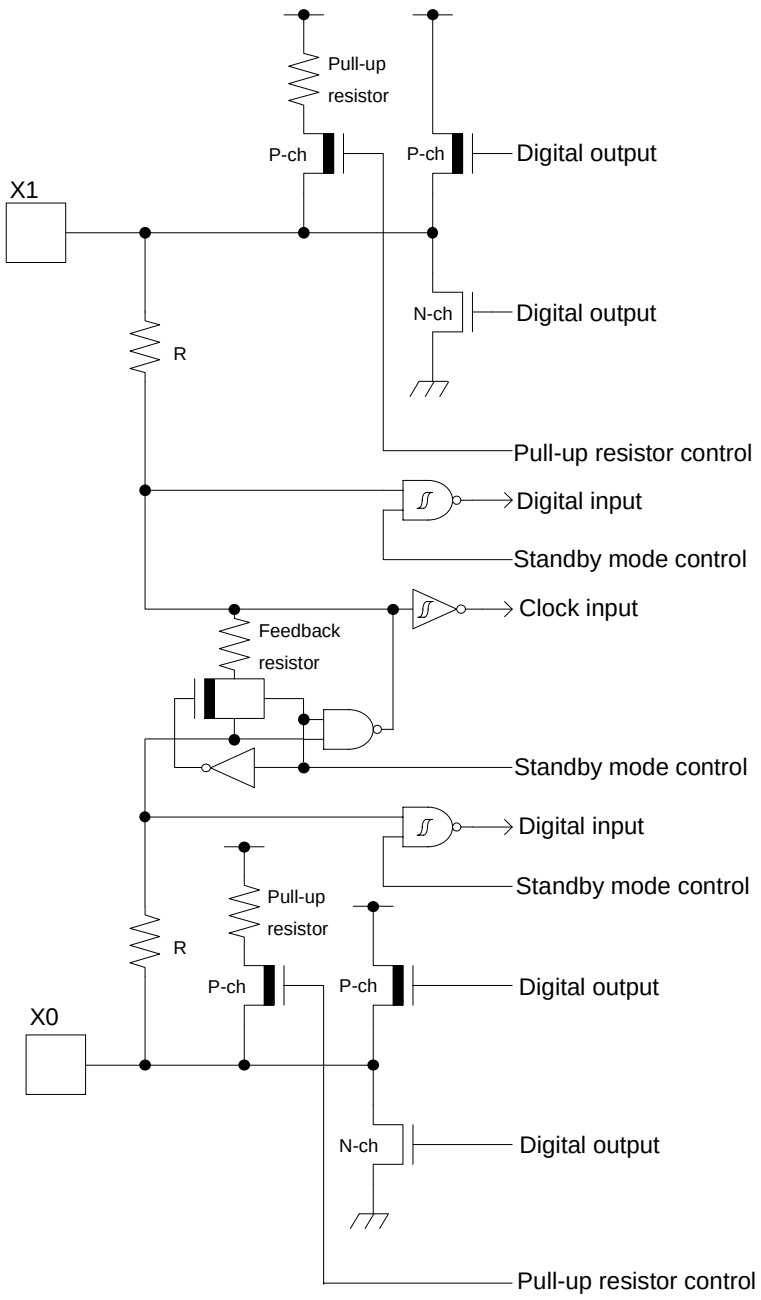
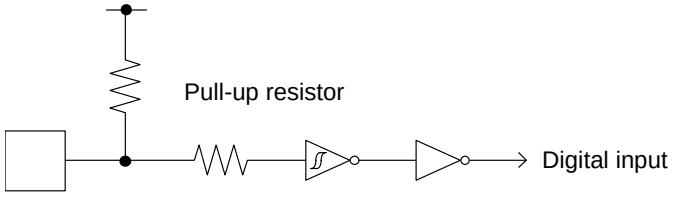
Note:

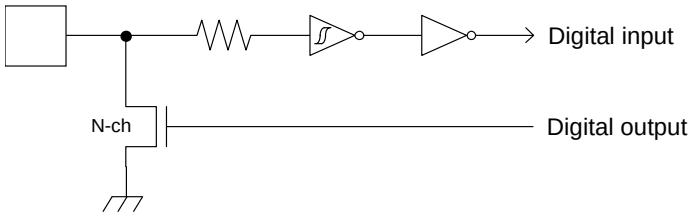
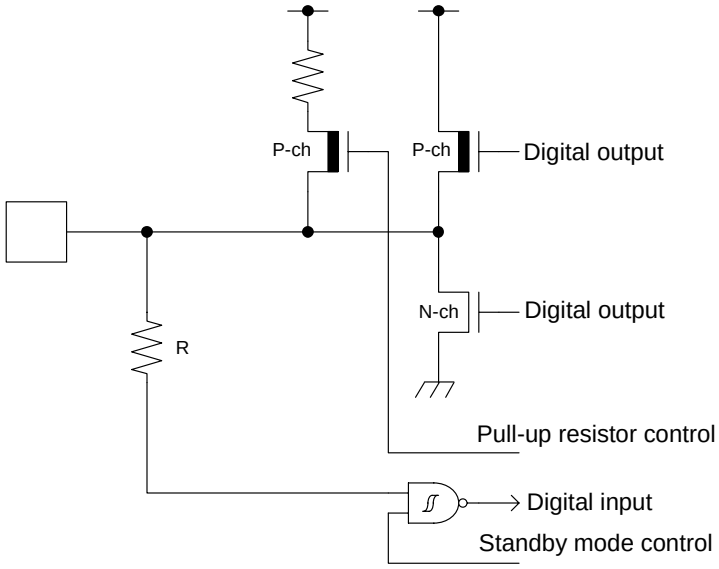
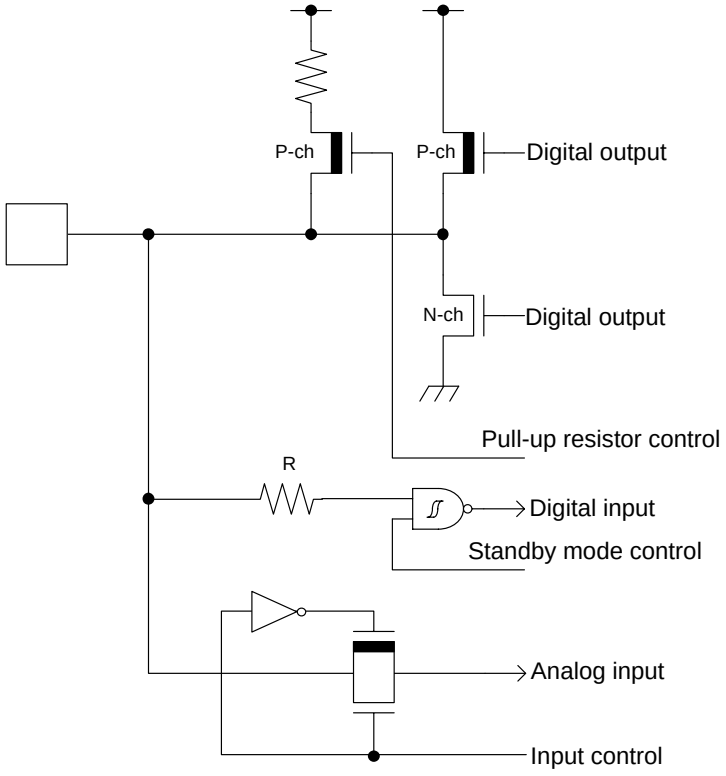
- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

Pin function	Pin name	Function description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
External Bus	MAD00_0	External bus interface address bus	27	22	17	100	K2	K2
	MAD01_0		28	23	18	1	L1	K3
	MAD02_0		29	24	19	2	L2	L1
	MAD03_0		47	42	32	20	L7	L7
	MAD04_0		48	43	33	21	L8	K7
	MAD05_0		49	44	34	22	M9	M8
	MAD06_0		50	45	35	23	L9	L8
	MAD07_0		62	52	41	30	L13	L12
	MAD08_0		63	53	42	31	L12	K12
	MAD09_0		64	54	43	32	K13	K11
	MAD10_0		65	55	44	33	K12	J12
	MAD11_0		66	56	45	34	J13	J11
	MAD12_0		67	57	46	35	J12	J10
	MAD13_0		68	58	47	36	J11	H12
	MAD14_0		69	59	48	37	H12	H11
	MAD15_0		74	64	53	42	H11	H10
	MAD16_0		75	65	54	43	G12	G12
	MAD17_0		76	66	55	44	G11	G11
	MAD18_0		77	67	56	45	F12	G10
	MAD19_0		78	68	-	46	F11	F13
	MAD20_0		79	69	-	47	E12	F12
	MAD21_0		80	70	-	48	E11	F11
	MAD22_0		86	71	-	49	D13	D13
	MAD23_0		88	73	-	51	C13	D11
	MAD24_0		89	74	-	52	C12	C12

Pin function	Pin name	Function description	Pin No					
			LQFP 120	LQFP 100	LQFP 80	QFP 100	BGA 112	BGA 144
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	2	80	C1	C1
	INT00_1		95	80	65	58	A10	B10
	INT00_2		108	-	-	-	-	C6
	INT01_0	External interrupt request 01 input pin	3	3	3	81	C2	C2
	INT01_1		101	86	-	64	C8	C8
	INT01_2		85	-	-	-	-	E10
	INT02_0	External interrupt request 02 input pin	6	6	6	84	D2	D3
	INT02_1		62	52	41	30	L13	L12
	INT02_2		82	-	-	-	-	E13
	INT03_0	External interrupt request 03 input pin	113	93	73	71	C5	B5
	INT03_1		65	55	44	33	K12	J12
	INT03_2		54	-	-	-	-	M10
	INT04_0	External interrupt request 04 input pin	17	12	12	90	F3	G3
	INT04_1		114	94	74	72	B5	C4
	INT04_2		10	-	-	-	-	E4
	INT05_0	External interrupt request 05 input pin	89	74	-	52	C12	C12
	INT05_1		75	65	54	43	G12	G12
	INT05_2		21	16	-	94	H2	H3
	INT06_1	External interrupt request 06 input pin	88	73	59	51	C13	D11
	INT06_2		22	17	-	95	H3	H4
	INT07_1	External interrupt request 07 input pin	11	-	-	-	-	F1
	INT07_2		7	7	7	85	E1	E1
	INT08_1	External interrupt request 08 input pin	19	14	-	92	G2	H1
	INT08_2		8	8	8	86	E2	E2
	INT09_1	External interrupt request 09 input pin	20	15	-	93	G3	H2
	INT09_2		15	10	10	88	F1	G1
	INT10_1	External interrupt request 10 input pin	16	11	11	89	F2	G2
	INT10_2		112	-	-	-	-	C5
	INT11_1	External interrupt request 11 input pin	50	45	35	23	L9	L8
	INT11_2		110	-	-	-	-	A6
	INT12_1	External interrupt request 12 input pin	32	27	-	5	N2	N2
	INT12_2		96	81	66	59	A9	D9
	INT13_1	External interrupt request 13 input pin	33	28	-	6	N3	L2
	INT13_2		49	44	34	22	M9	M8
	INT14_1	External interrupt request 14 input pin	68	58	47	36	J11	H12
	INT14_2		53	-	-	-	-	K9
	INT15_1	External interrupt request 15 input pin	52	-	-	-	-	L9
	INT15_2		14	9	9	87	E3	F4
	NMIX	Non-Maskable Interrupt input pin	116	96	76	74	B3	B3

5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. • Oscillation feedback resistor : Approximately 1MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = -4mA, I_{OL} = 4mA
B		• CMOS level hysteresis input • Pull-up resistor : Approximately 50kΩ

Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = -4mA, I_{OL} = 4mA
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = -4mA, I_{OL} = 4mA

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	TIMER mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
K	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixedat "0" / Analog input enabled	Hi-Z / Internal input fixedat "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected									
M	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at "0"			
	GPIO selected									

List of VBAT Domain Pin Status

VBAT pin status type	Function group	Power-on reset*1	INITX input state	Device internal reset state	Run mode or SLEEP mode state	TIMER mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state	VBAT RTC mode state	Return from VBAT RTC mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable	Power supply stable	Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1	-	-
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-	-	-
S	GPIO selected	Setting disabled	Maintain Previous state	Maintain Previous state	Maintain previous state	Maintain previous state	Maintain Previous state	Maintain Previous state	Maintain Previous state	Maintain Previous state	Setting prohibition	-
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Maintain previous state	Maintain previous state
T	GPIO selected	Setting disabled	Maintain Previous state	Maintain Previous state	Maintain previous state	Maintain previous state	Maintain Previous state	Maintain Previous state	Maintain Previous state	Maintain Previous state	Setting prohibition	-
	External sub clock input selected	Setting disabled	Maintain Previous state	Maintain Previous state	Maintain previous state	Maintain previous state	Maintain Previous state	Maintain previous state	Maintain Previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ or Input enable	Maintain Previous state	Maintain Previous state	Maintain previous state	Maintain previous state/When oscillation stops, Hi-Z*2	Maintain previous state/When oscillation stops, Hi-Z*2	Maintain previous state/When oscillation stops, Hi-Z*2	Maintain previous state/When oscillation stops, Hi-Z*2	Maintain Previous state	Maintain previous state	Maintain previous state
U	Resource selected / GPIO selected	Hi-Z	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state

*1: When VBAT and VCC power on.

*2: When the SOSCNTL bit in the WTOSCCNT register is 0, the sub crystal oscillator output pin is maintained in the previous state. When the SOSCNTL bit in the WTOSCCNT register is 1, oscillation is stopped at Stop mode and Deep Standby Stop

12.4.4 Operating Conditions of Main PLL (In the case of using main clock for input clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	200	-	-	µs	
PLL input clock frequency	F_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	80	multiplier	
PLL macro oscillation clock frequency	F_{PLLO}	200	-	320	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	160	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see “Chapter: Clock” in “FM4 Family Peripheral Manual”.

12.4.5 Operating Conditions of Main PLL (In the case of using built-in high-speed CR clock for input clock of main PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	200	-	-	µs	
PLL input clock frequency	F_{PLLI}	3.8	4	4.2	MHz	
PLL multiplication rate	-	50	-	75	multiplier	
PLL macro oscillation clock frequency	F_{PLLO}	190	-	320	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	160	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see “Chapter: Clock” in “FM4 Family Peripheral Manual”.

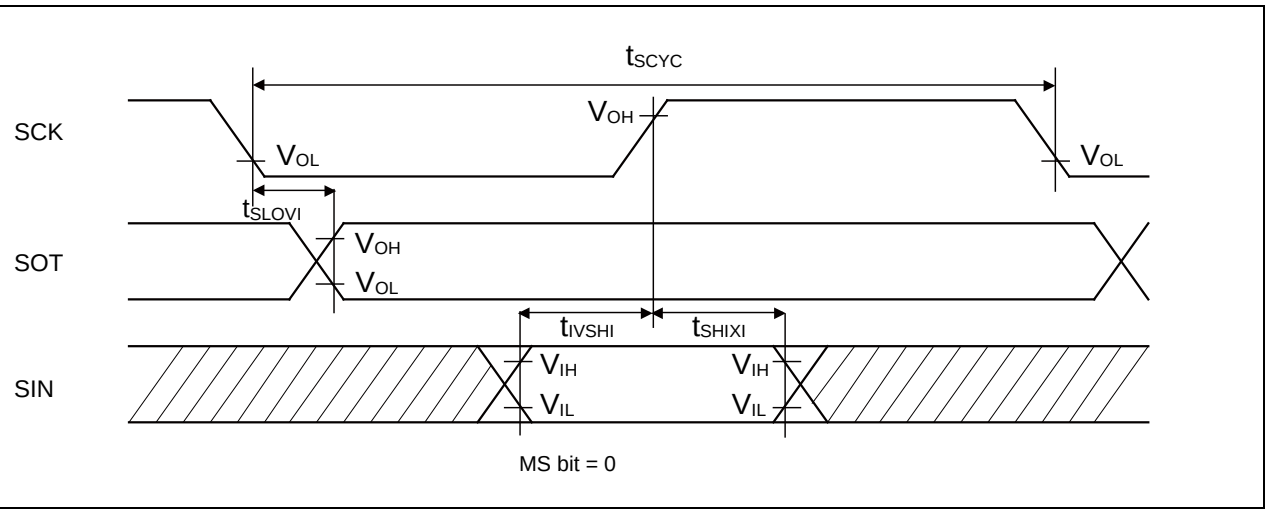
Note:

- *Make sure to input to the main PLL source clock, the high-speed CR clock (CLKHC) that the frequency and temperature has been trimmed.*

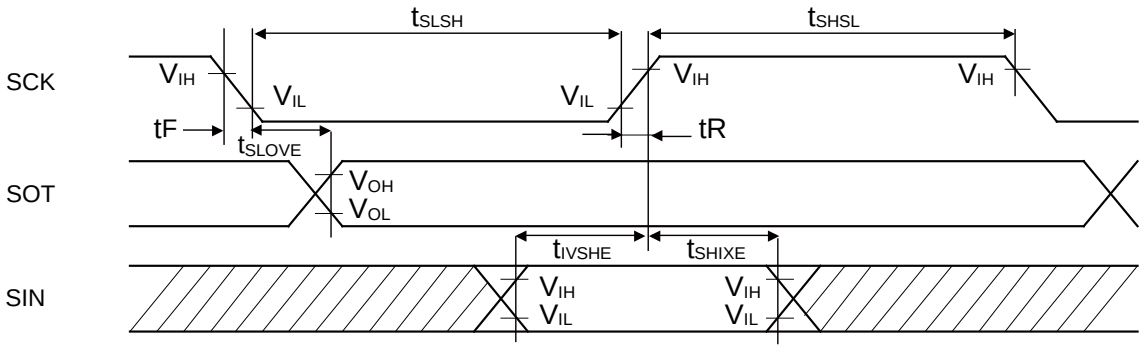
12.4.6 Reset Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	



MS bit = 0



MS bit = 1

When using synchronous serial chip select (SCINV = 0, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↓setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM4 Family Peripheral Manual".*
- *When the external load capacitance C_L = 30pF.*

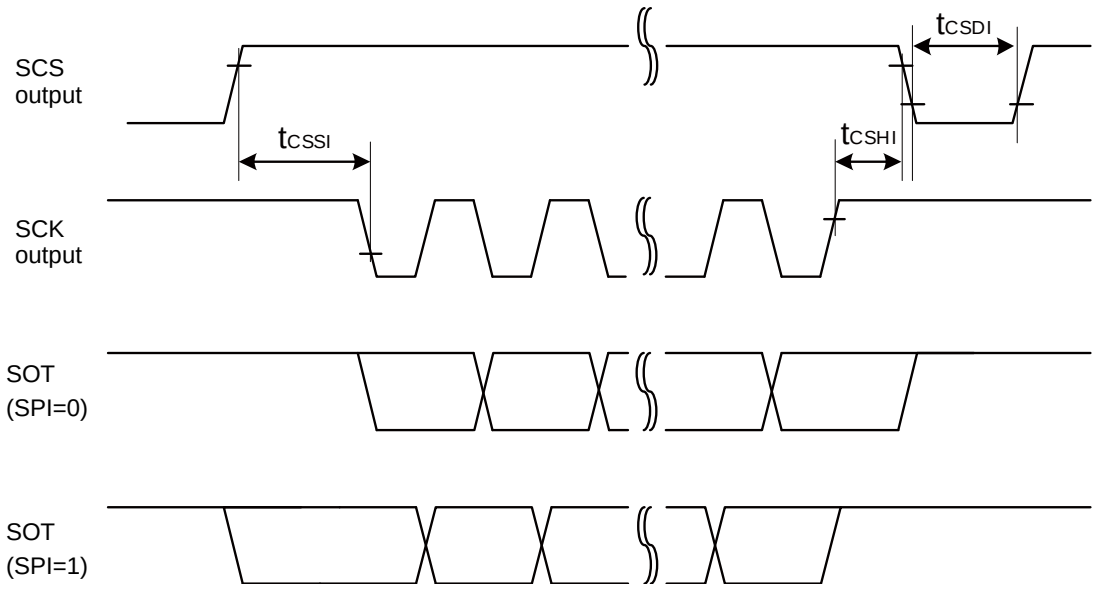
High-speed synchronous serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

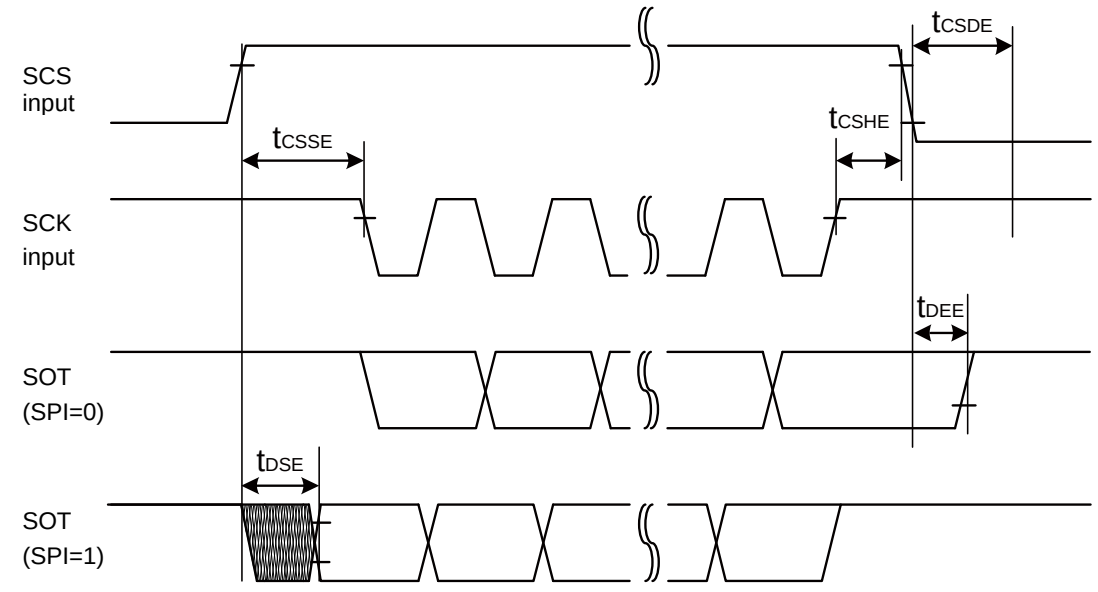
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see "Block Diagram" in this datasheet.
- *These characteristics only guarantee the following pins.*
  - *No chip select: SIN4_1, SOT4_1, SCK4_1*
  - *Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1*
- *When the external load capacitance C_L = 30pF. (For *, when C_L = 10pF)*



MS bit = 0



MS bit = 1

12.4.14 I²C Timing

Standard-mode, Fast-mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock "L" width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock "H" width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	2MHz ≤ t_{CYCP}<40MHz	$2t_{CYCP}$*4	-	$2t_{CYCP}$*4	-	ns	*5
		40MHz ≤ t_{CYCP}<60MHz	$4t_{CYCP}$*4	-	$4t_{CYCP}$*4	-	ns	
		60MHz ≤ t_{CYCP}<80MHz	$6t_{CYCP}$*4	-	$6t_{CYCP}$*4	-	ns	
		80MHz ≤ t_{CYCP}<100MHz	$8t_{CYCP}$*4	-	$8t_{CYCP}$*4	-	ns	
		100MHz ≤ t_{CYCP}<120MHz	$10t_{CYCP}$*4	-	$10t_{CYCP}$*4	-	ns	
		120MHz ≤ t_{CYCP}<140MHz	$12t_{CYCP}$*4	-	$12t_{CYCP}$*4	-	ns	
		140MHz ≤ t_{CYCP}<160MHz	$14t_{CYCP}$*4	-	$14t_{CYCP}$*4	-	ns	
		160MHz ≤ t_{CYCP}<180MHz	$16t_{CYCP}$*4	-	$16t_{CYCP}$*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it does not extend at least "L" period (t_{LOW}) of device's SCL signal.

*3: A Fast-mode I²C bus device can be used on a Standard-mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I²C is connected to, see "Block Diagram" in this data sheet.

*5: The noise filter time can be changed by register settings.
Change the number of the noise filter steps according to APB bus clock frequency.

Fast-mode Plus (Fm+)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Fast-mode Plus (Fm+)*6		Unit	Remarks
			Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30pF, R = (V_p/I_{OL})*1	0	1000	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		0.26	-	µs	
SCL clock "L" width	t_{LOW}		0.5	-	µs	
SCL clock "H" width	t_{HIGH}		0.26	-	µs	
SCL clock frequency	t_{SUSTA}		0.26	-	µs	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDDAT}		0	0.45*2, *3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		50	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		0.26	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		0.5	-	µs	
Noise filter	t_{SP}	60MHz ≤ t_{CYCP}<80MHz	6 t_{CYCP}*4	-	ns	*5
		80MHz ≤ t_{CYCP}<100MHz	8 t_{CYCP}*4	-	ns	
		100MHz ≤ t_{CYCP}<120MHz	10 t_{CYCP}*4	-	ns	
		120MHz ≤ t_{CYCP}<140MHz	12 t_{CYCP}*4	-	ns	
		140MHz ≤ t_{CYCP}<160MHz	14 t_{CYCP}*4	-	ns	
		160MHz ≤ t_{CYCP}<180MHz	16 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

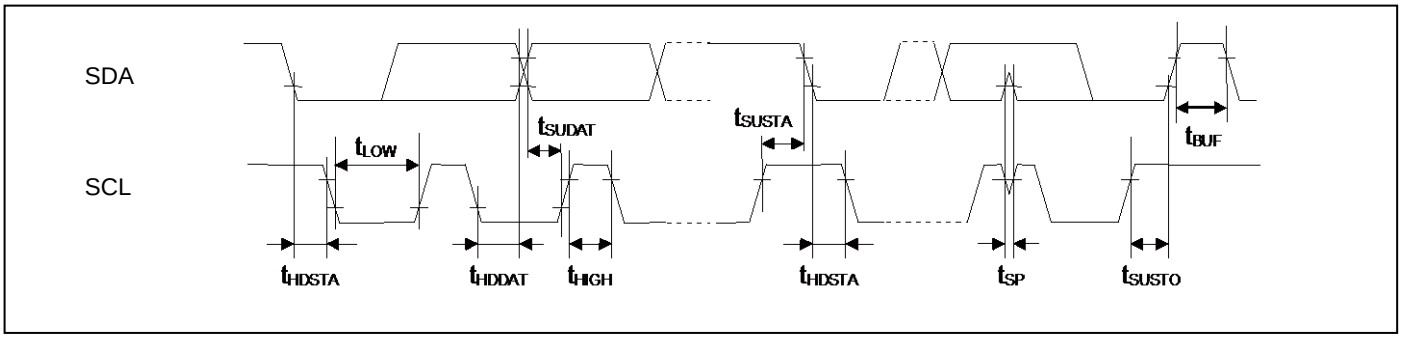
*2: The maximum t_{HDDAT} must satisfy that it does not extend at least "L" period (t_{LOW}) of device's SCL signal.

*3: A Fast-mode I^2C bus device can be used on a Standard-mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I^2C is connected to, see “Block Diagram” in this data sheet.
To use Fast-mode Plus (Fm+), set the peripheral bus clock at 64 MHz or more.

*5: The noise filter time can be changed by register settings.
Change the number of the noise filter steps according to APB bus clock frequency.

*6: When using Fast-mode Plus (Fm+), set the I/O pin to the mode corresponding to I^2C Fm+ in the EPFR register.
See “Chapter: I/O Port” in “FM4 Family Peripheral Manual” for the details.



12.4.15 SD Card Interface Timing

Default-Speed Mode

■Clock CLK (All values are referred to V_{IH} and V_{IL})

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer Mode	f_{PP}	S_CLK	C_{CARD} ≤ 10pF (1card)	0	16	MHz
Clock frequency Identification Mode	f_{OD}	S_CLK		0*/100	400	kHz
Clock low time	t_{WL}	S_CLK		10	-	ns
Clock high time	t_{WH}	S_CLK		10	-	ns
Clock rising time	t_{TLH}	S_CLK		-	10	ns
Clock falling time	t_{THL}	S_CLK		-	10	ns

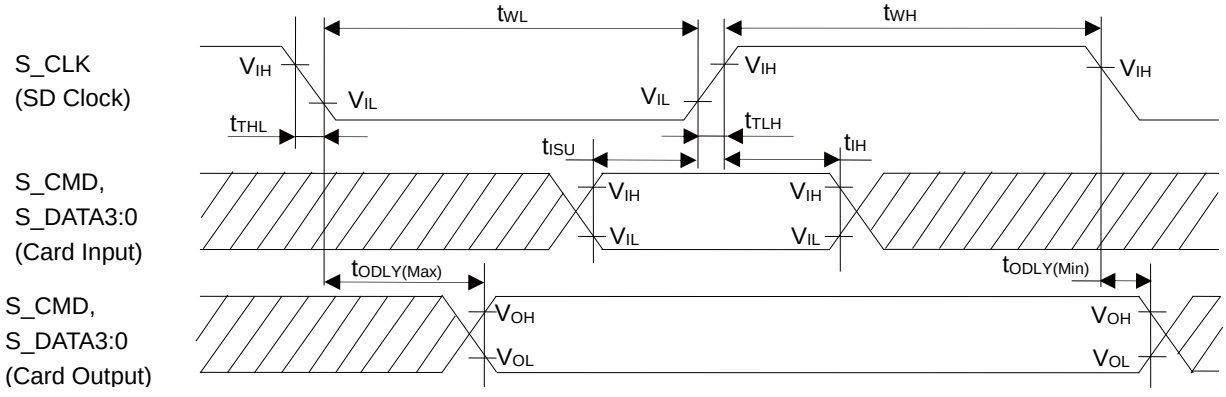
*: 0Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

■Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	t_{ISU}	S_CMD, S_DATA3:0	C_{CARD} ≤ 10pF (1card)	5	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3:0		5	-	ns

■Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin name	Conditions	Value		Remarks
				Min	Max	
Output Delay time during Data Transfer Mode	t_{ODLY}	S_CMD, S_DATA3:0	C_{CARD} ≤ 40pF (1card)	0	22	ns
Output Delay time durinn Identification Mode	t_{ODLY}	S_CMD, S_DATA3:0		0	50	ns



Defalt-Speed Mode

Note:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*

High-Speed Mode

■Clock CLK (All values are referred to V_{IH} and V_{IL})

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer Mode	f_{PP}	S_CLK	C_{CARD} ≤ 10pF (1card)	0	32	MHz
Clock low time	t_{WL}	S_CLK		7	-	ns
Clock high time	t_{WH}	S_CLK		7	-	ns
Clock rising time	t_{TLH}	S_CLK		-	3	ns
Clock falling time	t_{THL}	S_CLK		-	3	ns

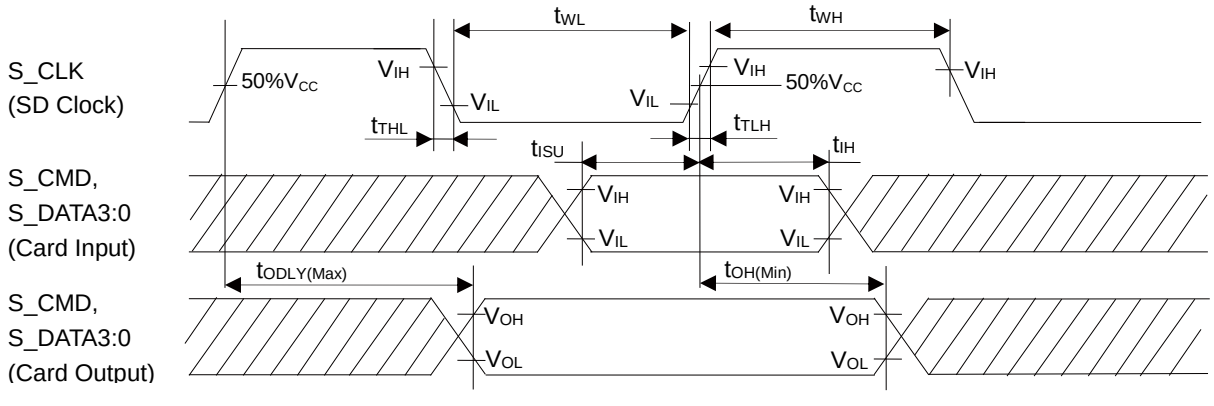
■Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	t_{ISU}	S_CMD, S_DATA3:0	C_{CARD} ≤ 10pF (1card)	8	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3:0		2	-	ns

■Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin name	Conditions	Value		Remarks
				Min	Max	
Output Delay time during Data Transfer Mode	t_{ODLY}	S_CMD, S_DATA3:0	C_L ≤ 40pF (1card)	-	22	ns
Output Hold time	t_{OH}	S_CMD, S_DATA3:0	C_L ≥ 15pF (1card)	2.5	-	ns
Total System capacitance for each line*	C_L	-	1card	-	40	pF

*: In order to satisfy severe timing, host shall drive only one card.



High-Speed Mode

Notes:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *In high-speed mode, set the Clock frequency (f_{PP}) and the AHB Bus Clock frequency to the same values.*

12.6 12-bit D/A Converter

Electrical Characteristics for the D/A Converter

(V_{CC} = AV_{CC} = 2.7Vto5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	12	bit	
Conversion time	tc20		0.56	0.69	0.81	µs	Load 20pF
	tc100		2.79	3.42	4.06	µs	Load 100pF
Integral Nonlinearity*	INL		- 16	-	+ 16	LSB	
Differential Nonlinearity*	DNL		- 0.98	-	+ 1.5	LSB	
Output voltage offset	V_{OFF}		-	-	10.0	mV	When setting 0x000
			- 20.0	-	+ 1.4	mV	When setting 0xFFF
Analog output impedance	R_O		3.10	3.80	4.50	kΩ	D/A operation
			2.0	-	-	MΩ	When D/A stop
Power supply current*	IDDA	AVCC	260	330	410	µA	D/A 1unit operation AV_{CC} = 3.3V
			400	510	620	µA	D/A 1unit operation AV_{CC} = 5.0V
	IDSA		-	-	14	µA	When D/A stop

*: During no load

12.8 MainFlash Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 5.5V)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector		0.3	1.1		
Half word (16-bit) write time	Write cycles ≤ 100 times	-	12	100	µs	Not including system-level overhead time
	Write cycles > 100 times			200		
Chip erase time		-	13.6	68	s	Includes write time prior to internal erase

Write cycles and data hold time

Erase/Write cycles (cycle)	Data hold time (year)
1,000	20 *
10,000	10 *
100,000	5 *

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C) .

12.9 WorkFlash Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 5.5V)

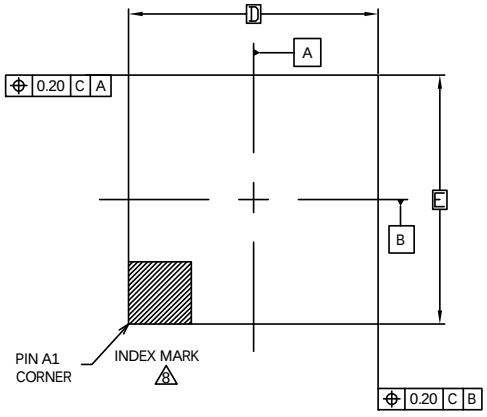
Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.3	1.5	s	Includes write time prior to internal erase
Half word (16-bit) write time	-	20	200	µs	Not including system-level overhead time
Chip erase time	-	1.2	6	s	Includes write time prior to internal erase

Write cycles and data hold time

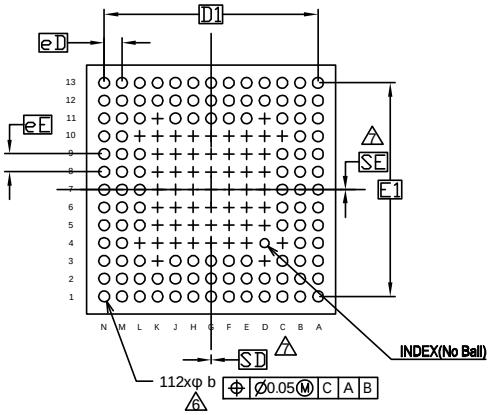
Erase/Write cycles (cycle)	Data hold time (year)
1,000	20 *
10,000	10 *
100,000	5 *

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C) .

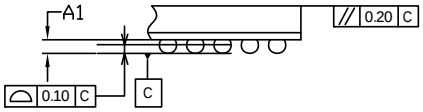
Package Type	Package Code
BGA-112	LDC112



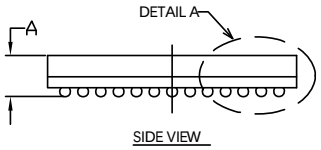
TOP VIEW



BOTTOM VIEW



DETAIL A



SIDE VIEW

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.35
A_1	0.15	0.25	0.35
D		7.00 BSC	
E		7.00 BSC	
D1		6.00 BSC	
E 1		6.00 BSC	
MD		13	
ME		13	
n		112	
Φb	0.20	0.30	0.40
eD		0.50 BSC	
eE		0.50 BSC	
SD / SE		0.00	

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" =0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

PACKAGE OUTLINE, 112 BALL FBGA
7.0X7.0X1.35 MM LDC112 REV**

002-16663 **