Renesas Electronics America Inc - R5F52203BDFM#30 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52203bdfm-30

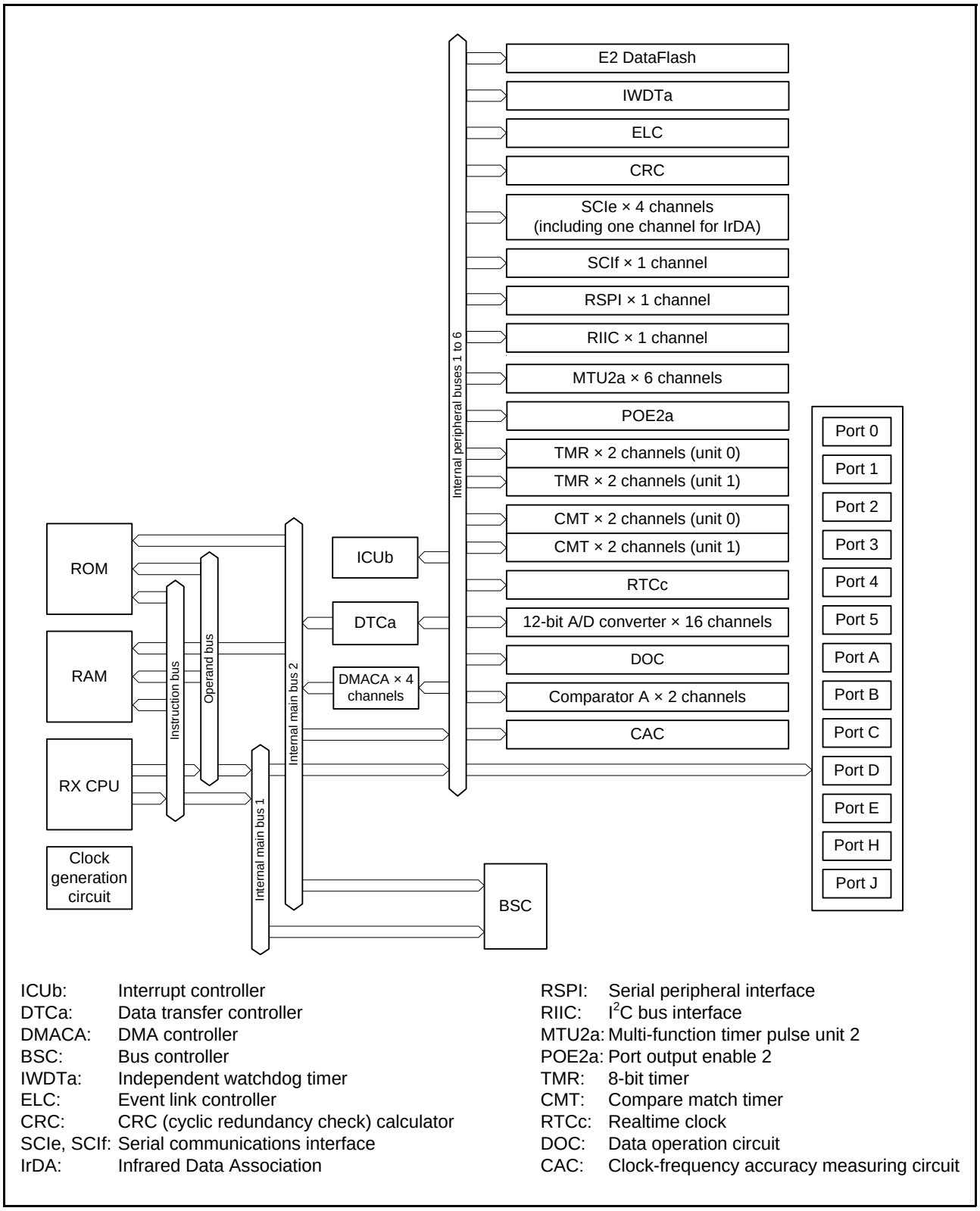
Table 1.1 Outline of Specifications (3 / 3)

Classification	Module/Function	Description
Communication function	Serial communications interfaces (SCIe, SCIf)	• 5 channels (channel 1, 5, 6, and 9: SCIe, channel 12: SCIf) (including one channel for IrDA) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Average transfer rate clock can be input from TMR timers (SCI5, SCI6, and SCI12) • Simple IIC • Simple SPI • Master/slave mode supported (SCIf only) • Start frame and information frame are included (SCIf only) • Detection of a start bit in asynchronous mode: Low level or falling edge is selectable (SCIe/SCIf)
	IrDA interface (IRDA)	• 1 channel (SCI5 is used) • Supports encoding/decoding the waveforms conforming to the IrDA specification version 1.0
	I^2C bus interface (RIIC)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master/slave selectable • Supports the fast mode
	Serial peripheral interface (RSPI)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
12-bit A/D converter (S12ADb)		• 12 bits (16 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.56 μs per channel (in operation with ADCLK at 32 MHz) • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) • Sample-and-hold function • Self-diagnosis for the A/D converter • Assistance in detecting disconnected analog inputs • Double-trigger mode (duplication of A/D conversion data) • A/D conversion start conditions A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC
CRC calculator (CRC)		• CRC code generation for any desired data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator A (CMPA)		• 2 channels • Comparison of reference voltage and analog input voltage
Data Operation Circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Power supply voltage/Operating frequency		VCC = 1.62 to 2.7 V: 8 MHz, VCC = 2.7 to 5.5 V: 32 MHz
Operating temperature		D version: –40 to +85°C, G version: –40 to +105°C*1
Package		100-pin LQFP (PLQP0100KB-A) 64-pin LQFP (PLQP0064KB-A) 64-pin LQFP (PLQP0064GA-A) 48-pin LQFP (PLQP0048KB-A)

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

1.3 Block Diagram

Figure 1.2 shows a block diagram.



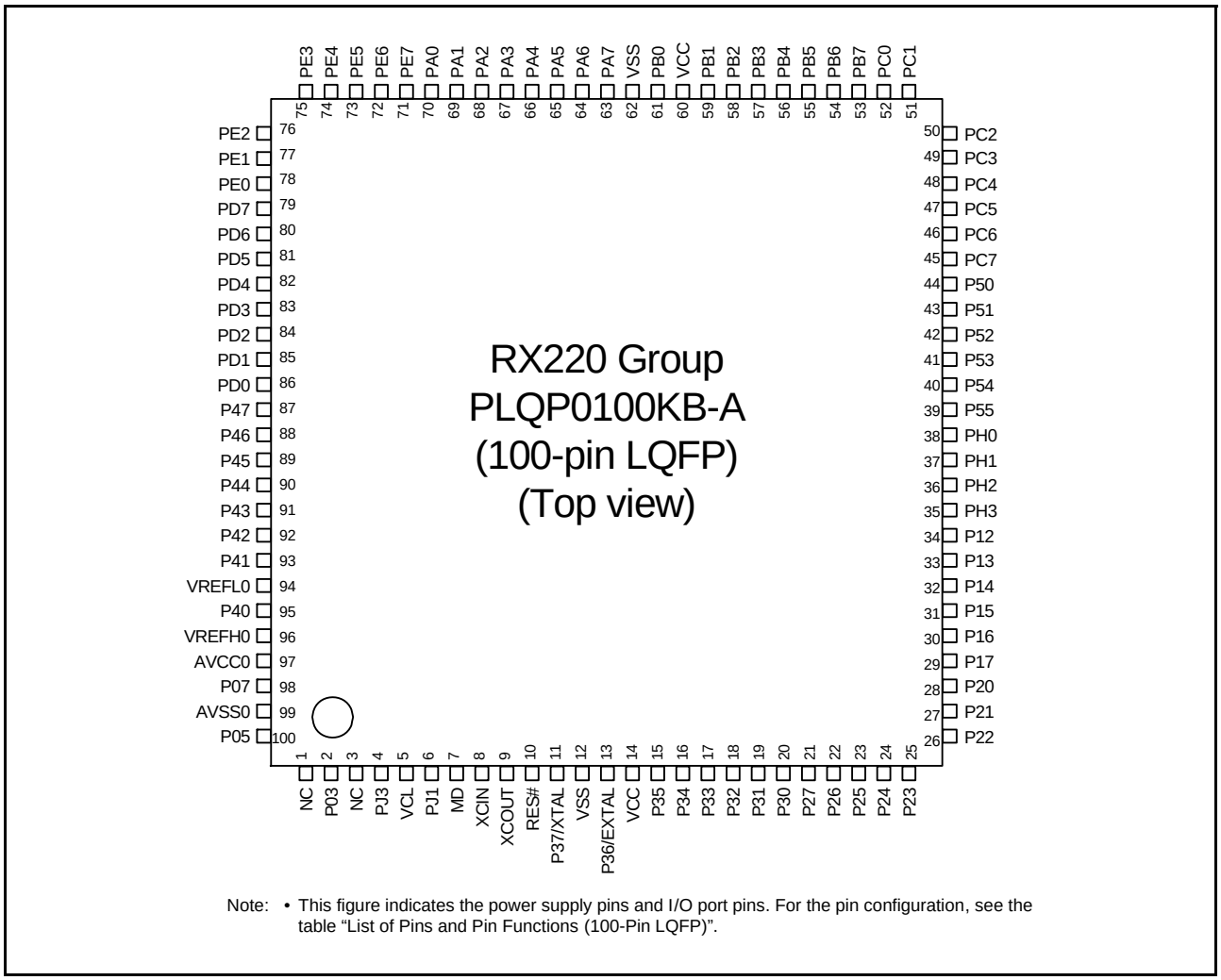
ICUb: Interrupt controller
DTCa: Data transfer controller
DMACA: DMA controller
BSC: Bus controller
IWDTa: Independent watchdog timer
ELC: Event link controller
CRC: CRC (cyclic redundancy check) calculator
SCIe, SCIf: Serial communications interface
IrDA: Infrared Data Association

RSPI: Serial peripheral interface
RIIC: I^2C bus interface
MTU2a: Multi-function timer pulse unit 2
POE2a: Port output enable 2
TMR: 8-bit timer
CMT: Compare match timer
RTCc: Realtime clock
DOC: Data operation circuit
CAC: Clock-frequency accuracy measuring circuit

Figure 1.2 Block Diagram

1.5 Pin Assignments

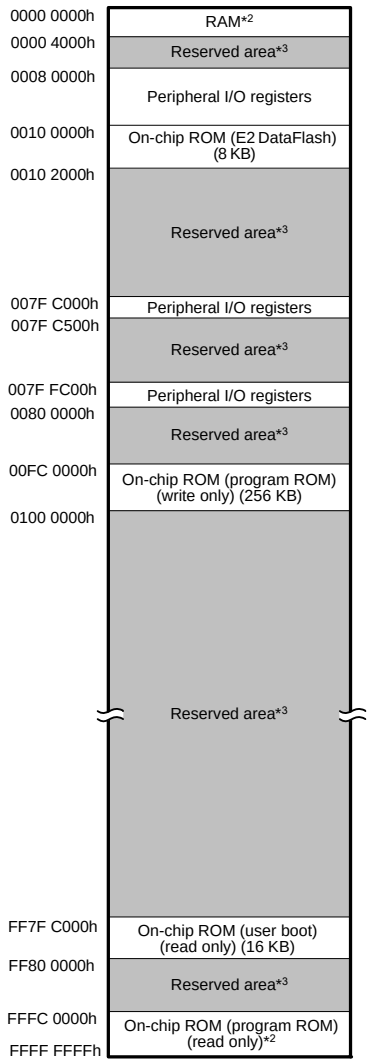
Figure 1.3 to Figure 1.5 show the pin assignments. Table 1.5 to Table 1.7 show the lists of pins and pin functions.



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin LQFP)”.

Figure 1.3 Pin Assignments of the 100-Pin LQFP

Single-chip mode*1



Note 1. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
256 K	FFFC 0000h to FFFF FFFFh	16 K	0000 0000h to 0000 3FFFh
128 K	FFFE 0000h to FFFF FFFFh	8 K	0000 0000h to 0000 1FFFh
64K	FFFF 0000h to FFFF FFFFh		
32 K	FFFF 8000h to FFFF FFFFh	4 K	0000 0000h to 0000 0FFFh

Note:•See Table 1.3, List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For numbers of clock cycles for access to I/O registers, see Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral bus 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction bus access from the different bus master (DMAC or DTC).

Table 4.1 List of I/O Registers (Address Order) (5 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK	
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK	
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK	
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK	
0008 7167h	ICU	DTC activation enable register 103	DTCER103	8	8	2 ICLK	
0008 716Ah	ICU	DTC activation enable register 106	DTCER106	8	8	2 ICLK	
0008 7172h	ICU	DTC activation enable register 114	DTCER114	8	8	2 ICLK	
0008 7173h	ICU	DTC activation enable register 115	DTCER115	8	8	2 ICLK	
0008 7174h	ICU	DTC activation enable register 116	DTCER116	8	8	2 ICLK	
0008 7175h	ICU	DTC activation enable register 117	DTCER117	8	8	2 ICLK	
0008 7179h	ICU	DTC activation enable register 121	DTCER121	8	8	2 ICLK	
0008 717Ah	ICU	DTC activation enable register 122	DTCER122	8	8	2 ICLK	
0008 717Dh	ICU	DTC activation enable register 125	DTCER125	8	8	2 ICLK	
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8	2 ICLK	
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8	2 ICLK	
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8	2 ICLK	
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8	2 ICLK	
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8	2 ICLK	
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8	2 ICLK	
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8	2 ICLK	
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8	2 ICLK	
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8	2 ICLK	
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8	2 ICLK	
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8	2 ICLK	
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8	2 ICLK	
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8	2 ICLK	
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8	2 ICLK	
0008 71AFh	ICU	DTC activation enable register 175	DTCER175	8	8	2 ICLK	
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8	2 ICLK	
0008 71B2h	ICU	DTC activation enable register 178	DTCER178	8	8	2 ICLK	
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8	2 ICLK	
0008 71B5h	ICU	DTC activation enable register 181	DTCER181	8	8	2 ICLK	
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8	2 ICLK	
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8	2 ICLK	
0008 71C6h	ICU	DTC activation enable register 198	DTCER198	8	8	2 ICLK	
0008 71C7h	ICU	DTC activation enable register 199	DTCER199	8	8	2 ICLK	
0008 71C8h	ICU	DTC activation enable register 200	DTCER200	8	8	2 ICLK	
0008 71C9h	ICU	DTC activation enable register 201	DTCER201	8	8	2 ICLK	
0008 71DBh	ICU	DTC activation enable register 219	DTCER219	8	8	2 ICLK	
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8	2 ICLK	
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8	2 ICLK	
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8	2 ICLK	
0008 71E3h	ICU	DTC activation enable register 227	DTCER227	8	8	2 ICLK	
0008 71E4h	ICU	DTC activation enable register 228	DTCER228	8	8	2 ICLK	
0008 71EBh	ICU	DTC activation enable register 235	DTCER235	8	8	2 ICLK	
0008 71ECh	ICU	DTC activation enable register 236	DTCER236	8	8	2 ICLK	
0008 71EFh	ICU	DTC activation enable register 239	DTCER239	8	8	2 ICLK	
0008 71F0h	ICU	DTC activation enable register 240	DTCER240	8	8	2 ICLK	
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8	2 ICLK	
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8	2 ICLK	
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (11 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 8704h	MTU0	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8705h	MTU0	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8706h	MTU0	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8708h	MTU0	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 870Ah	MTU0	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 870Ch	MTU0	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
0008 870Eh	MTU0	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
0008 8720h	MTU0	Timer general register E	TGRE	16	16	2, 3 PCLKB	2 ICLK
0008 8722h	MTU0	Timer general register F	TGRF	16	16	2, 3 PCLKB	2 ICLK
0008 8724h	MTU0	Timer interrupt enable register 2	TIER2	8	8	2, 3 PCLKB	2 ICLK
0008 8726h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK
0008 8780h	MTU1	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8781h	MTU1	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8782h	MTU1	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
0008 8784h	MTU1	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8785h	MTU1	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8786h	MTU1	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8788h	MTU1	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 878Ah	MTU1	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8790h	MTU1	Timer input capture control register	TICCR	8	8	2, 3 PCLKB	2 ICLK
0008 8800h	MTU2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8801h	MTU2	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8802h	MTU2	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
0008 8804h	MTU2	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8805h	MTU2	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8806h	MTU2	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8808h	MTU2	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 880Ah	MTU2	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8880h	MTU5	Timer counter U	TCNTU	16	16	2, 3 PCLKB	2 ICLK
0008 8882h	MTU5	Timer general register U	TGRU	16	16	2, 3 PCLKB	2 ICLK
0008 8884h	MTU5	Timer control register U	TCRU	8	8	2, 3 PCLKB	2 ICLK
0008 8886h	MTU5	Timer I/O control register U	TIORU	8	8	2, 3 PCLKB	2 ICLK
0008 8890h	MTU5	Timer counter V	TCNTV	16	16	2, 3 PCLKB	2 ICLK
0008 8892h	MTU5	Timer general register V	TGRV	16	16	2, 3 PCLKB	2 ICLK
0008 8894h	MTU5	Timer control register V	TCRV	8	8	2, 3 PCLKB	2 ICLK
0008 8896h	MTU5	Timer I/O control register V	TIORV	8	8	2, 3 PCLKB	2 ICLK
0008 88A0h	MTU5	Timer counter W	TCNTW	16	16	2, 3 PCLKB	2 ICLK
0008 88A2h	MTU5	Timer general register W	TGRW	16	16	2, 3 PCLKB	2 ICLK
0008 88A4h	MTU5	Timer control register W	TCRW	8	8	2, 3 PCLKB	2 ICLK
0008 88A6h	MTU5	Timer I/O control register W	TIORW	8	8	2, 3 PCLKB	2 ICLK
0008 88B2h	MTU5	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 88B4h	MTU5	Timer start register	TSTR	8	8	2, 3 PCLKB	2 ICLK
0008 88B6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	2, 3 PCLKB	2 ICLK
0008 8900h	POE	Input level control/status register 1	ICSR1	16	8, 16	2, 3 PCLKB	2 ICLK
0008 8902h	POE	Output level control/status register 1	OCSR1	16	8, 16	2, 3 PCLKB	2 ICLK
0008 8908h	POE	Input level control/status register 2	ICSR2	16	8, 16	2, 3 PCLKB	2 ICLK
0008 890Ah	POE	Software port output enable register	SPOER	8	8	2, 3 PCLKB	2 ICLK
0008 890Bh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK
0008 890Ch	POE	Port output enable control register 2	POECR2	8	8	2, 3 PCLKB	2 ICLK
0008 890Eh	POE	Input level control/status register 3	ICSR3	16	8, 16	2, 3 PCLKB	2 ICLK
0008 9000h	S12AD	A/D control register	ADCSR	16	16	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (15 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 B32Dh	SCI12	Secondary control field 1 data register	SCF1DR	8	8	2, 3 PCLKB	2 ICLK
0008 B32Eh	SCI12	Control field 1 compare enable register	CF1CR	8	8	2, 3 PCLKB	2 ICLK
0008 B32Fh	SCI12	Control field 1 receive data register	CF1RR	8	8	2, 3 PCLKB	2 ICLK
0008 B330h	SCI12	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 B331h	SCI12	Timer mode register	TMR	8	8	2, 3 PCLKB	2 ICLK
0008 B332h	SCI12	Timer prescaler register	TPRE	8	8	2, 3 PCLKB	2 ICLK
0008 B333h	SCI12	Timer count register	TCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C000h	PORT0	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C001h	PORT1	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C002h	PORT2	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C003h	PORT3	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C004h	PORT4	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C005h	PORT5	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C00Ah	PORTA	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C00Bh	PORTB	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C00Ch	PORTC	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C00Dh	PORTD	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C00Eh	PORTE	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C011h	PORTH	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C012h	PORTJ	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C020h	PORT0	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C021h	PORT1	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C022h	PORT2	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C023h	PORT3	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C024h	PORT4	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C025h	PORT5	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C02Ah	PORTA	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C02Bh	PORTB	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C02Ch	PORTC	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C02Dh	PORTD	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C02Eh	PORTE	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C031h	PORTH	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C032h	PORTJ	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C040h	PORT0	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C041h	PORT1	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C042h	PORT2	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing

Table 4.1 List of I/O Registers (Address Order) (20 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C42Eh	RTC	Time error adjustment register	RADJ	8	8	2, 3 PCLKB	2 ICLK
007F C402h	FLASH	Flash mode register	FMODR	8	8	2, 3 FCLK	2 ICLK
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2, 3 FCLK	2 ICLK
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2, 3 FCLK	2 ICLK
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2, 3 FCLK	2 ICLK
007F C440h	FLASH	E2 DataFlash read enable register 0	DFLRE0	16	16	2, 3 FCLK	2 ICLK
007F C450h	FLASH	E2 DataFlash programming/erasure enable register 0	DFLWE0	16	16	2, 3 FCLK	2 ICLK
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2, 3 FCLK	2 ICLK
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2, 3 FCLK	2 ICLK
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2, 3 FCLK	2 ICLK
007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2, 3 FCLK	2 ICLK
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2, 3 FCLK	2 ICLK
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2, 3 FCLK	2 ICLK
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2, 3 FCLK	2 ICLK
007F FFCAh	FLASH	E2 DataFlash blank check control register	DFLBCCNT	16	16	2, 3 FCLK	2 ICLK
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2, 3 FCLK	2 ICLK
007F FFCEh	FLASH	E2 DataFlash blank check status register	DFLBCSTAT	16	16	2, 3 FCLK	2 ICLK
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2, 3 FCLK	2 ICLK

Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register.
Note 2. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMOCNTL register.

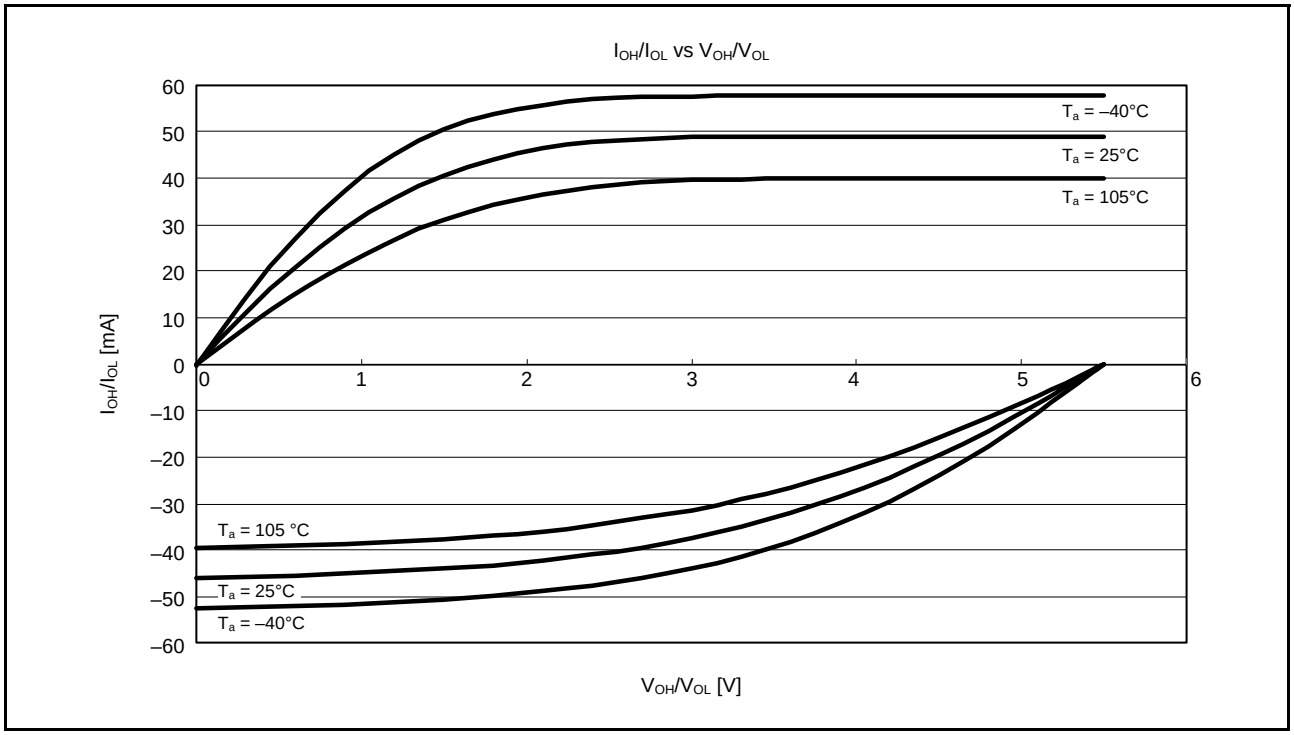


Figure 5.11 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V when Normal Output is Selected (Reference Data)

5.3.1 Clock Timing

Table 5.22 Clock Timing

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXcyc}	50	—	—	ns	Figure 5.21
EXTAL external clock input high pulse width	t_{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	20	—	—	ns	
EXTAL external clock rising time	t_{EXr}	—	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1	t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency*2	f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*2	$t_{MAINOSC}$	—	3	—	ms	Figure 5.22
Main clock oscillation stabilization time (ceramic resonator)*2	$t_{MAINOSC}$	—	50	—	µs	
Main clock oscillation stabilization wait time (crystal)*2	$t_{MAINOSCWT}$	—	6	—	ms	
Main clock oscillation stabilization wait time (ceramic resonator)*2	$t_{MAINOSCWT}$	—	100	—	µs	
LOCO clock cycle time	t_{cyc}	7.27	8	8.89	µs	
LOCO clock oscillation frequency	f_{LOCO}	112.5	125	137.5	kHz	
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	20	µs	Figure 5.23
HOCO clock oscillation frequency	f_{HOCO}	31.680	32	32.320	MHz	T_a = 0 to 50°C
		36.495	36.864	37.233		
		39.600	40	40.400		
		49.500	50	50.500		
		31.520	32	32.480		T_a = -40 to 105°C
		36.311	36.864	37.417		
		39.400	40	40.600		
		49.250	50	50.750		
HOCO clock oscillation stabilization time 1	t_{HOCO1}	—	—	50	µs	Figure 5.24
HOCO clock oscillation stabilization time 2	t_{HOCO2}	—	—	10	µs	Figure 5.25
HOCO clock oscillation stabilization wait time	t_{HOCOWT}	—	—	20	µs	Figure 5.25
HOCO clock power supply stabilization time	t_{HOCOP}	—	—	350	µs	Figure 5.26
Sub-clock oscillator oscillation frequency	f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*3	t_{SUBOSC}	2	—	—	s	Figure 5.27
Sub-clock oscillation stabilization wait time*3	$t_{SUBOSCWT}$	4	—	—	s	

Note 1. The time interval from the time P36 and P37 are configured for input and the main clock oscillator stopping bit (MOSCCR.MOSTP) is set to 0 (operating) until the clock becomes available.

Note 2. When specifying the main clock oscillator stabilization time, load MOSCWTCR register with a stabilization time value that is greater than the resonator-vendor-recommended value. When determining the main lock oscillation stabilization wait time, allow an adequate margin (2 times is recommended) for the main clock oscillation stabilization time.
Start using the main clock in the main clock oscillation stabilization wait time (tMAINOSCWT) after setting up the main clock oscillator for operation with the MOSCCR.MOSTP bit.
The indicated value is a reference value that is measured for an 8 MHz resonator.

Note 3. When specifying the sub-clock oscillation stabilization time, load SOSCWTCR register with the resonator-vendor-recommended stabilization time value minus 2 seconds. When determining the sub-clock oscillation stabilization wait time, allow an adequate margin (2 times is recommended) for the sub-clock oscillation stabilization time. Start using the sub-clock in the sub-clock oscillation stabilization wait time (tSUBOSCWT) after setting up the sub-clock oscillator for operation with the SOSCCR.SOSTP or RCR3.RTCEN bit.

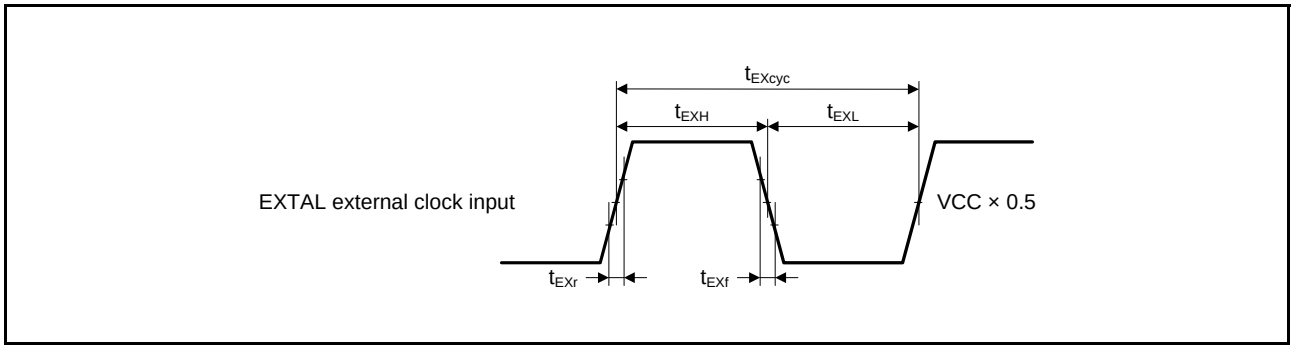


Figure 5.21 EXTAL External Clock Input Timing

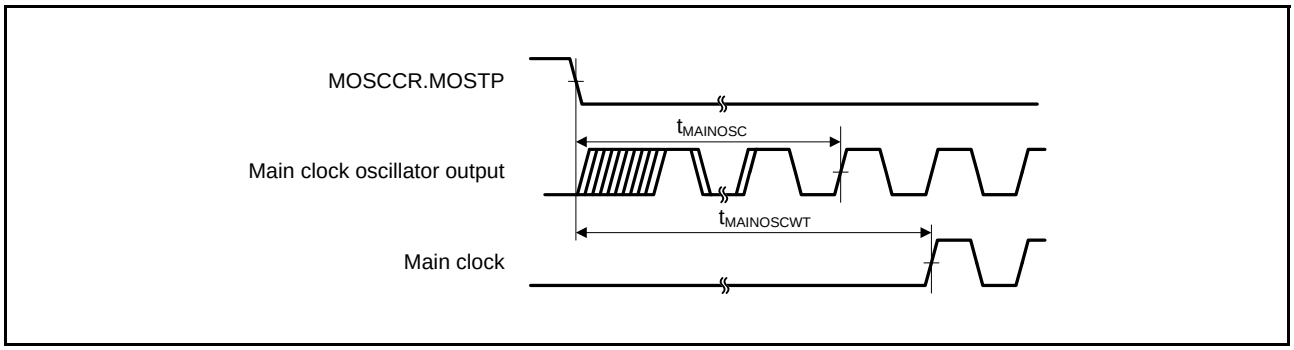


Figure 5.22 Main Clock Oscillation Start Timing

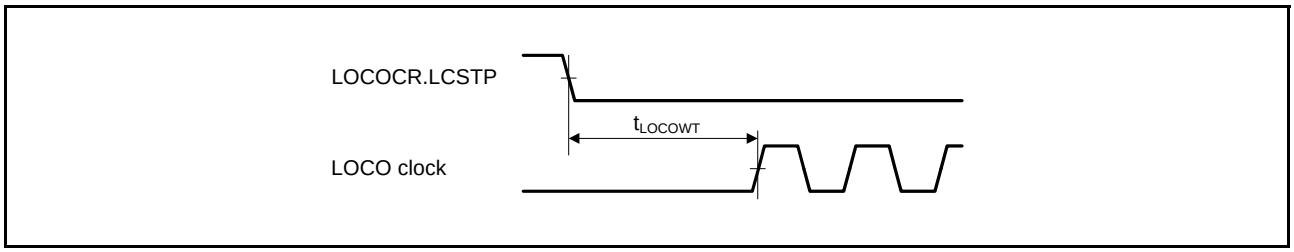


Figure 5.23 LOCO Clock Oscillation Start Timing

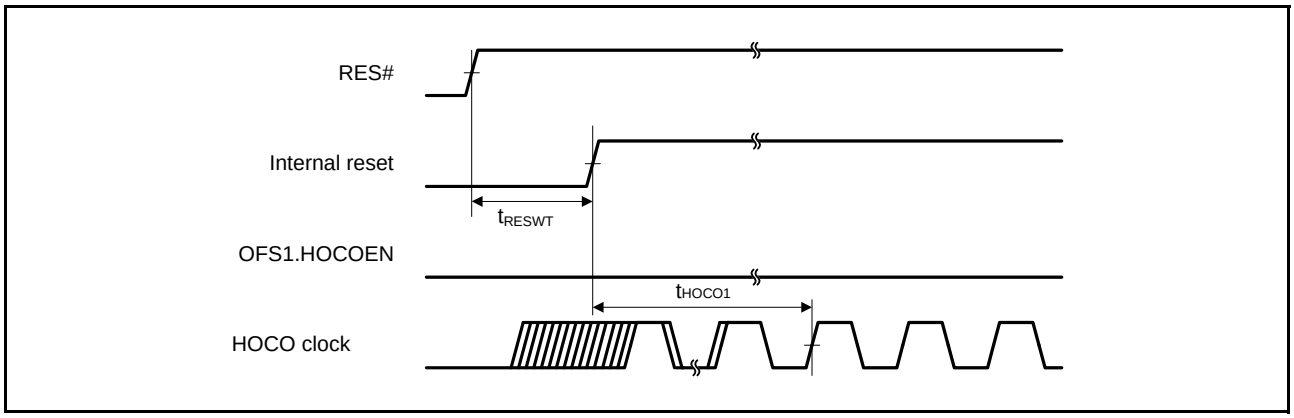


Figure 5.24 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting the OFS1.HOCOEN Bit to 0)

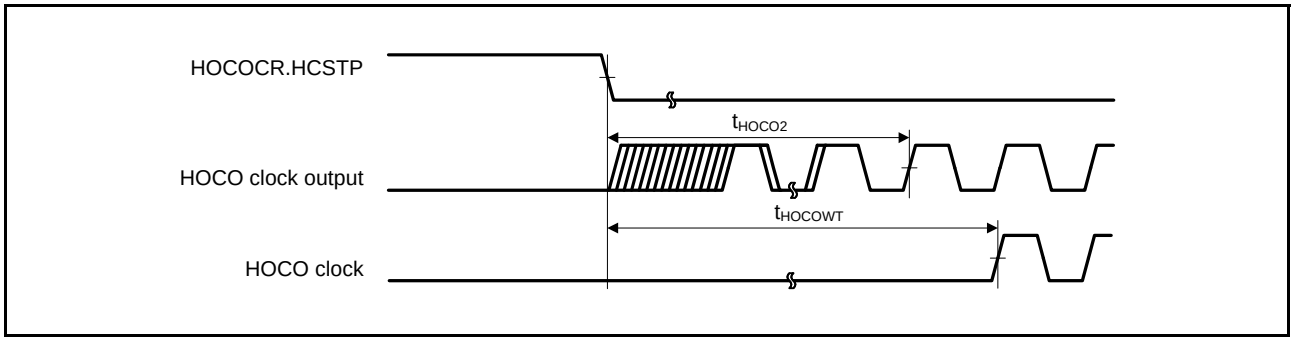


Figure 5.25 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

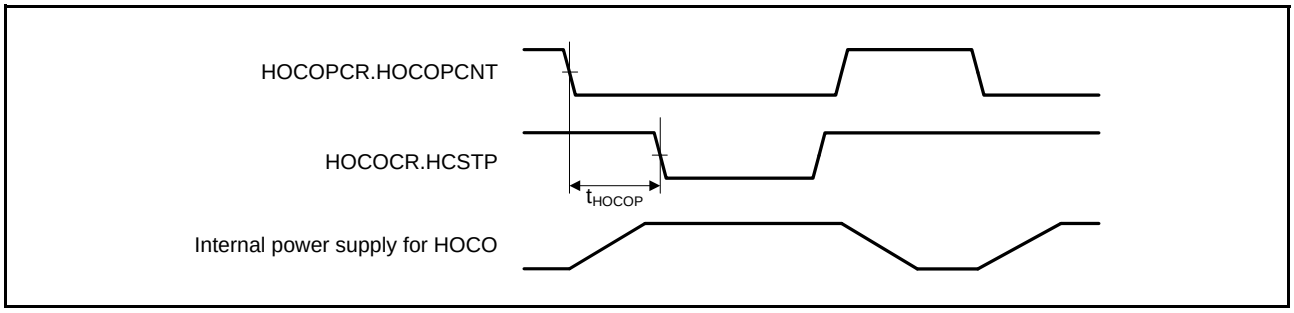


Figure 5.26 HOCO Power Control Timing

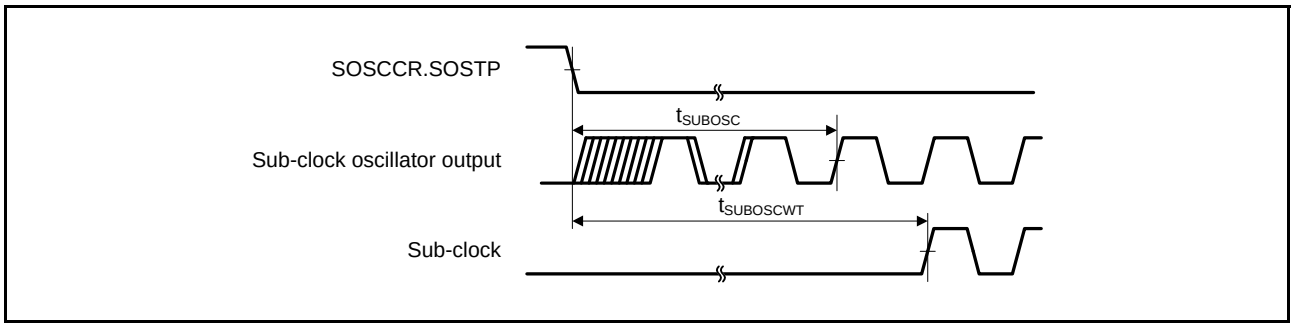


Figure 5.27 Sub-clock Oscillation Start Timing

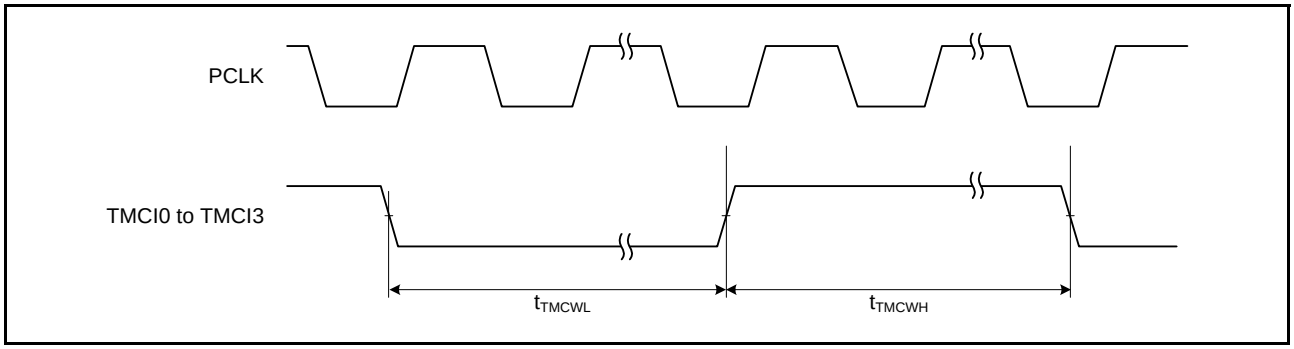


Figure 5.37 8-Bit Timer Clock Input Timing

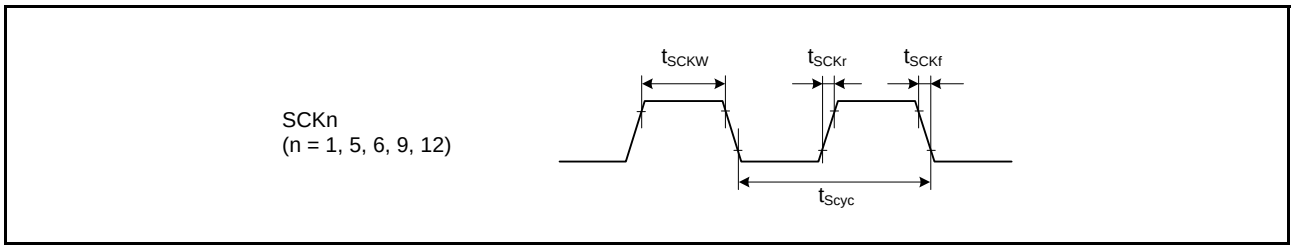


Figure 5.38 SCK Clock Input Timing

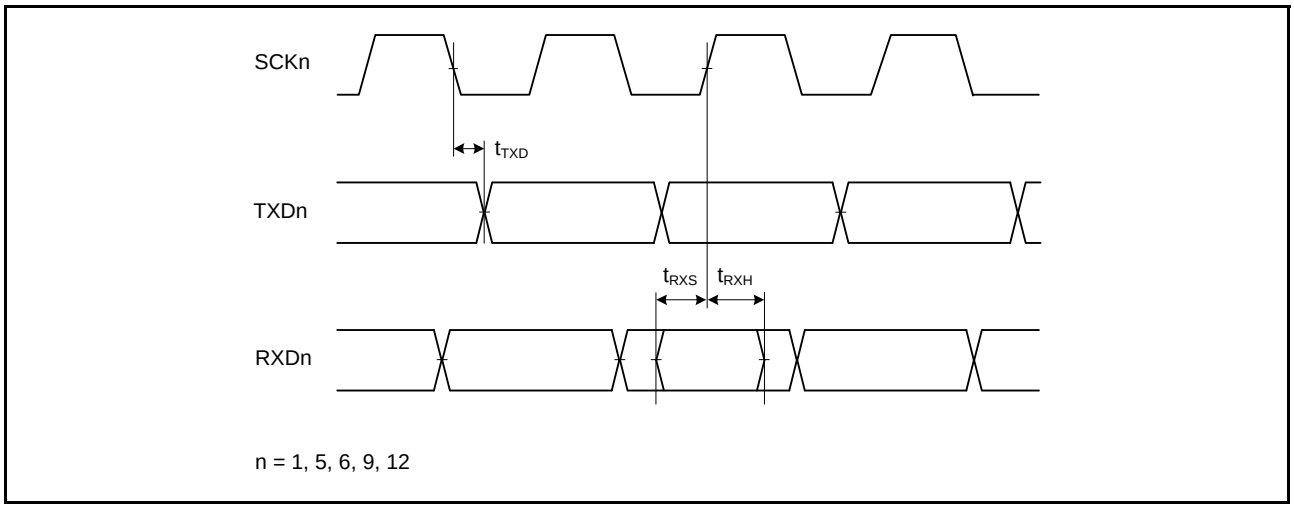


Figure 5.39 SCI Input/Output Timing: Clock Synchronous Mode

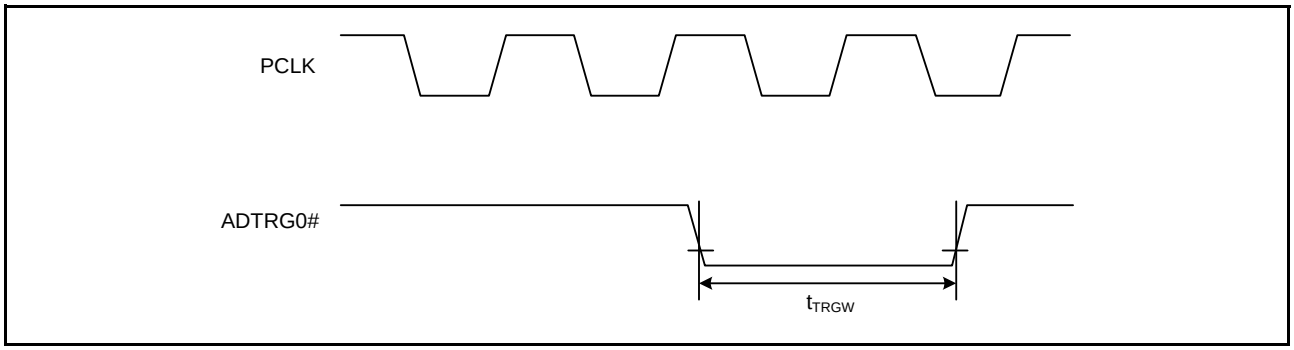


Figure 5.40 A/D Converter External Trigger Input Timing

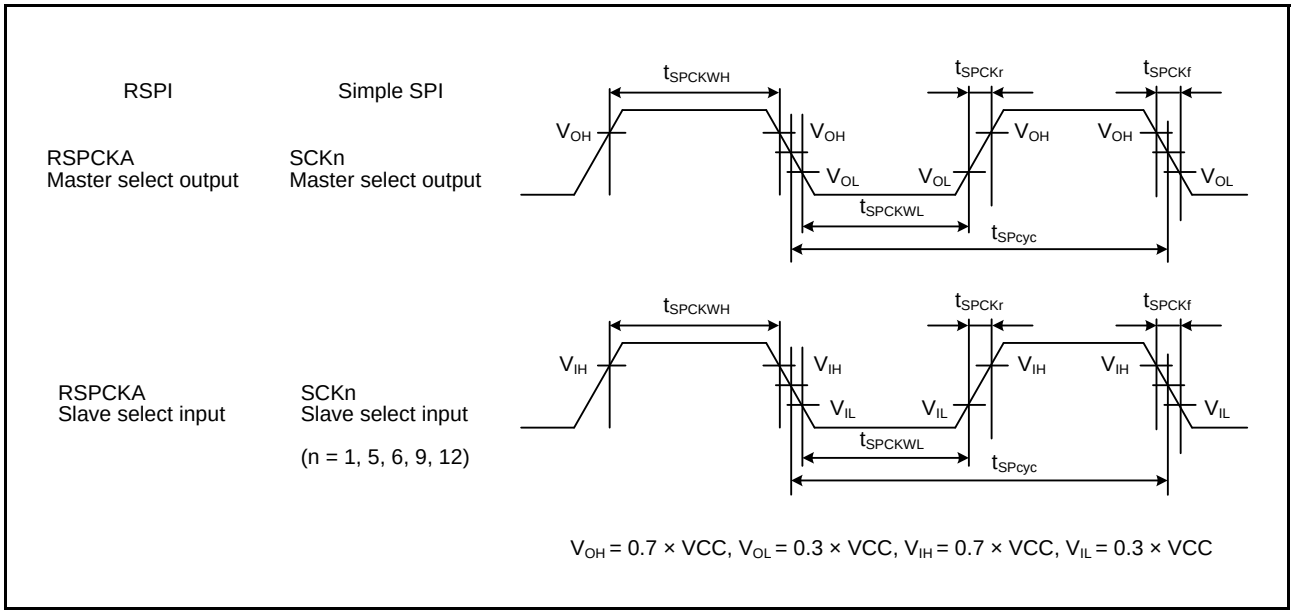


Figure 5.41 RSPI Clock Timing and Simple SPI Clock Timing

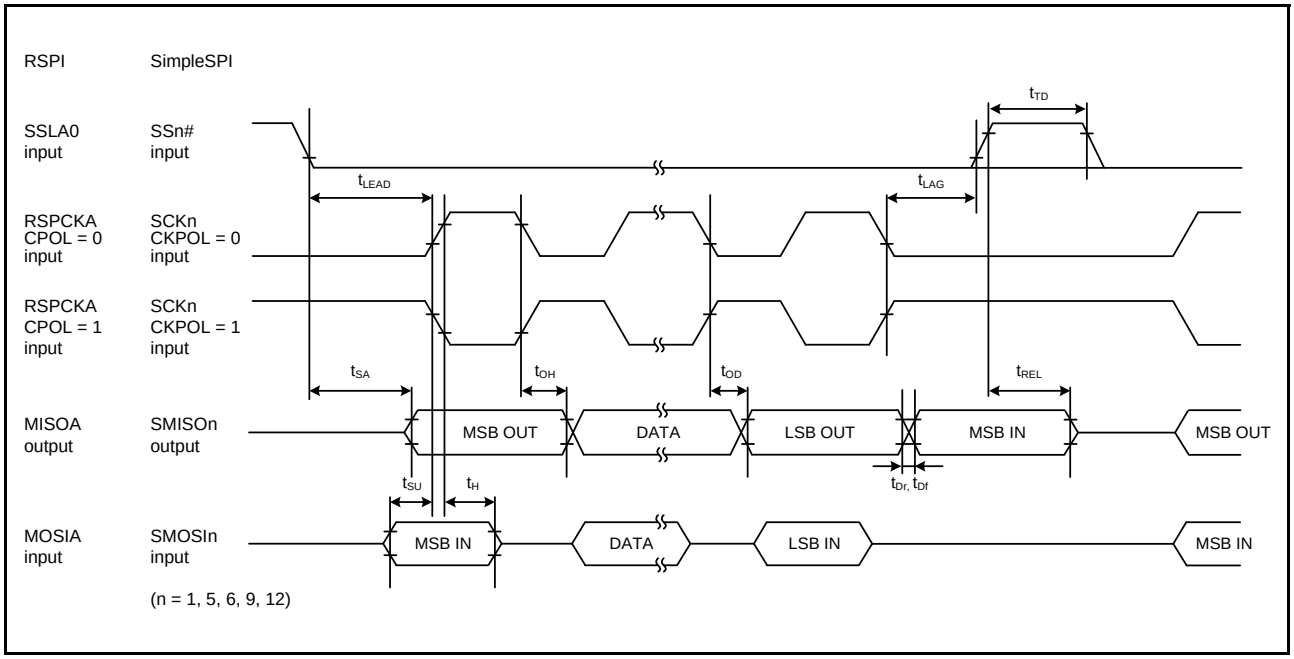


Figure 5.46 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

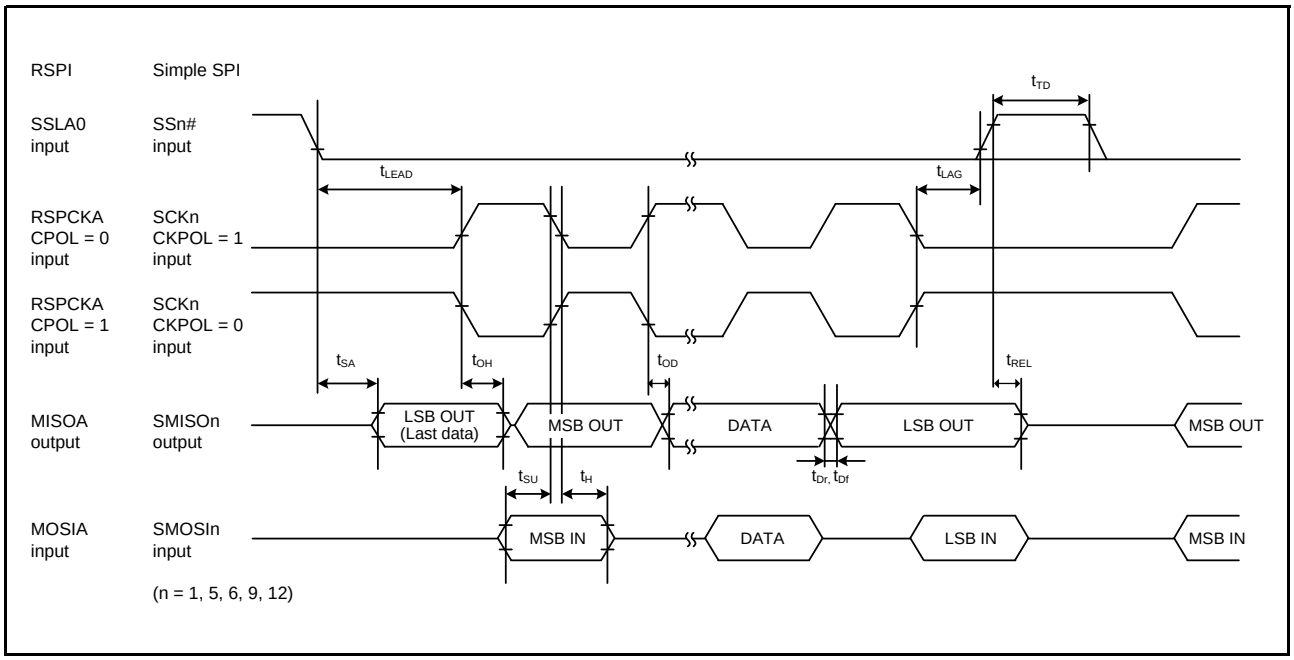


Figure 5.47 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

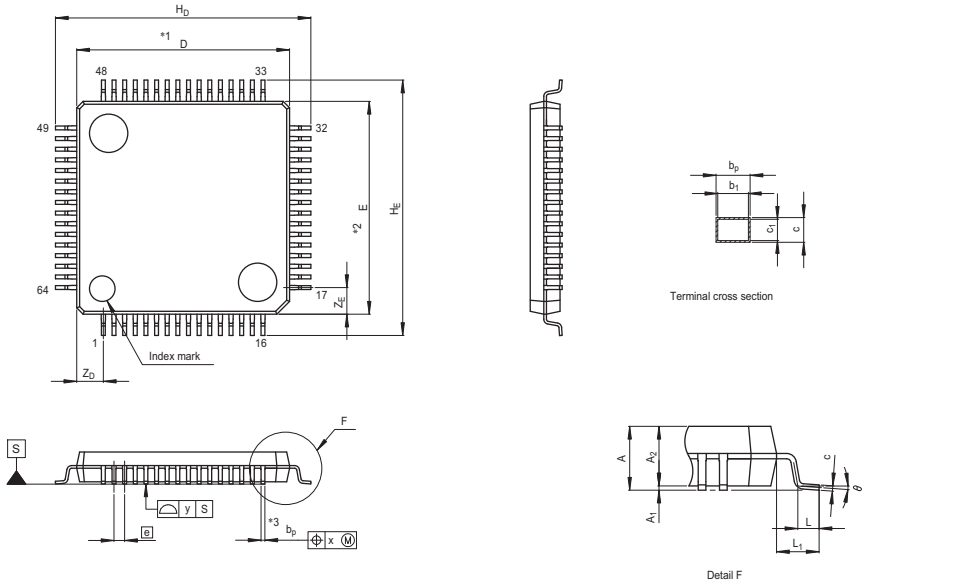
**Table 5.47 E2 DataFlash Characteristics (4)
medium-speed operating mode 1B**

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.28	5.1	—	0.20	2.8	ms
	8 bytes	t_{DP8}	—	0.32	6.0	—	0.22	3.2	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.36	7.6	—	0.25	4.2	ms
	8 bytes	t_{DP8}	—	0.40	8.8	—	0.28	4.5	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	4.8	32.3	—	4.1	12	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	5.8	51.4	—	4.9	17	ms
Blank check time	2 bytes	t_{DBC2}	—	—	110	—	—	40	µs
	2 Kbytes	t_{DBC2K}	—	—	16.3	—	—	2.6	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	1.7	—	—	1.6	ms

Note 1. The operating frequency is 8 MHz (max.) when the voltage is in the range from 1.62 V to less than 2.7 V.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g

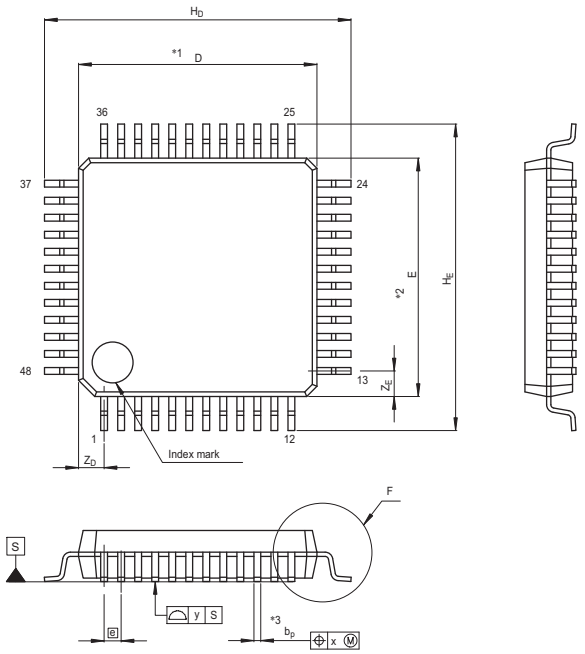


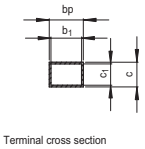
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

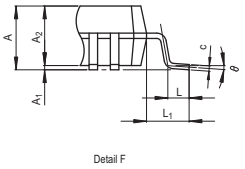
Figure B 64-Pin LQFP (PLQP0064KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure D 48-Pin LQFP (PLQP0048KB-A)