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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52205bdfl-30

Table 1.1 Outline of Specifications (3 / 3)

Classification	Module/Function	Description
Communication function	Serial communications interfaces (SCIe, SCIf)	• 5 channels (channel 1, 5, 6, and 9: SCIe, channel 12: SCIf) (including one channel for IrDA) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Average transfer rate clock can be input from TMR timers (SCI5, SCI6, and SCI12) • Simple IIC • Simple SPI • Master/slave mode supported (SCIf only) • Start frame and information frame are included (SCIf only) • Detection of a start bit in asynchronous mode: Low level or falling edge is selectable (SCIe/SCIf)
	IrDA interface (IRDA)	• 1 channel (SCI5 is used) • Supports encoding/decoding the waveforms conforming to the IrDA specification version 1.0
	I^2C bus interface (RIIC)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master/slave selectable • Supports the fast mode
	Serial peripheral interface (RSPI)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
12-bit A/D converter (S12ADb)		• 12 bits (16 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.56 μs per channel (in operation with ADCLK at 32 MHz) • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) • Sample-and-hold function • Self-diagnosis for the A/D converter • Assistance in detecting disconnected analog inputs • Double-trigger mode (duplication of A/D conversion data) • A/D conversion start conditions A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC
CRC calculator (CRC)		• CRC code generation for any desired data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator A (CMPA)		• 2 channels • Comparison of reference voltage and analog input voltage
Data Operation Circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Power supply voltage/Operating frequency		VCC = 1.62 to 2.7 V: 8 MHz, VCC = 2.7 to 5.5 V: 32 MHz
Operating temperature		D version: –40 to +85°C, G version: –40 to +105°C*1
Package		100-pin LQFP (PLQP0100KB-A) 64-pin LQFP (PLQP0064KB-A) 64-pin LQFP (PLQP0064GA-A) 48-pin LQFP (PLQP0048KB-A)

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products

Group	Part No.	Package	ROM Capacity	RAM Capacity	Operating Frequency (Max.)	Operating temperature
RX220	R5F52206BDFP	PLQP0100KB-A	256 Kbytes	16 Kbytes	32 MHz	–40 to +85°C
	R5F52206BDFM	PLQP0064KB-A				
	R5F52206BDFK	PLQP0064GA-A				
	R5F52206BDFL	PLQP0048KB-A				
	R5F52205BDFP	PLQP0100KB-A	128 Kbytes	8 Kbytes		
	R5F52205BDFM	PLQP0064KB-A				
	R5F52205BDFK	PLQP0064GA-A				
	R5F52205BDFL	PLQP0048KB-A				
	R5F52203BDFP	PLQP0100KB-A	64 Kbytes			
	R5F52203BDFM	PLQP0064KB-A				
	R5F52203BDFK	PLQP0064GA-A				
	R5F52203BDFL	PLQP0048KB-A				
	R5F52201BDFM	PLQP0064KB-A	32 Kbytes	4Kbytes		
	R5F52201BDFK	PLQP0064GA-A				
	R5F52201BDFL	PLQP0048KB-A				
	R5F52206BGFP	PLQP0100KB-A	256 Kbytes	16 Kbytes	32 MHz	–40 to +105°C
	R5F52206BGFM	PLQP0064KB-A				
	R5F52206BGFK	PLQP0064GA-A				
	R5F52206BGFL	PLQP0048KB-A				
	R5F52205BGFP	PLQP0100KB-A	128 Kbytes	8 Kbytes		
	R5F52205BGFM	PLQP0064KB-A				
	R5F52205BGFK	PLQP0064GA-A				
	R5F52205BGFL	PLQP0048KB-A				
	R5F52203BGFP	PLQP0100KB-A	64 Kbytes			
	R5F52203BGFM	PLQP0064KB-A				
	R5F52203BGFK	PLQP0064GA-A				
	R5F52203BGFL	PLQP0048KB-A				
	R5F52201BGFM	PLQP0064KB-A	32 Kbytes	4Kbytes		
	R5F52201BGFK	PLQP0064GA-A				
	R5F52201BGFL	PLQP0048KB-A				

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (2 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIe, SCIf, RSPI, RIIC)	Others
48		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/SSLA0	
49		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/IRTXD5	
50		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/IRRXD5/ SSLA3	
51		PC1	MTIOC3A	SCK5/SSLA2	
52		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1	
53		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	
54		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	
55		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	
56		PB4		CTS9#/RTS9#/SS9#	
57		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	
58		PB2		CTS6#/RTS6#/SS6#	
59		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4
60	VCC				
61		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	
62	VSS				
63		PA7		MISOA	
64		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	
65		PA5		RSPCKA	
66		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/IRTXD5/ SSLA0	IRQ5
67		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5/IRRXD5	IRQ6
68		PA2		RXD5/SMISO5/SSCL5/SSLA3/ IRRXD5	
69		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
70		PA0	MTIOC4A	SSLA1	CACREF
71		PE7			IRQ7/AN015
72		PE6			IRQ6/AN014
73		PE5	MTIOC4C/MTIOC2B		IRQ5/AN013
74		PE4	MTIOC4D/MTIOC1A		AN012/CMPA2
75		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
76		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12	IRQ7/AN010
77		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009
78		PE0		SCK12	AN008
79		PD7	MTIC5U/POE0#		IRQ7
80		PD6	MTIC5V/POE1#		IRQ6
81		PD5	MTIC5W/POE2#		IRQ5
82		PD4	POE3#		IRQ4
83		PD3	POE8#		IRQ3
84		PD2	MTIOC4D		IRQ2
85		PD1	MTIOC4B		IRQ1
86		PD0			IRQ0
87		P47			AN007
88		P46			AN006
89		P45			AN005
90		P44			AN004

Table 1.6 List of Pins and Pin Functions (64-Pin LQFP) (2 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIe, SCIf, RSPI, RIIC)	Others
44		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
45		PA0	MTIOC4A	SSLA1	CACREF
46		PE5	MTIOC4C/MTIOC2B		IRQ5/AN013
47		PE4	MTIOC4D/MTIOC1A		AN012/CMPA2
48		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
49		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12	IRQ7/AN010
50		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009
51		PE0		SCK12	AN008
52	NC (Non-Connection)				
53		P46			AN006
54	NC (Non-Connection)				
55		P44			AN004
56		P43			AN003
57		P42			AN002
58		P41			AN001
59	VREFL0				
60		P40			AN000
61	VREFH0				
62	AVCC0				
63		P05			
64	AVSS0				

Table 4.1 List of I/O Registers (Address Order) (5 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK	
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK	
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK	
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK	
0008 7167h	ICU	DTC activation enable register 103	DTCER103	8	8	2 ICLK	
0008 716Ah	ICU	DTC activation enable register 106	DTCER106	8	8	2 ICLK	
0008 7172h	ICU	DTC activation enable register 114	DTCER114	8	8	2 ICLK	
0008 7173h	ICU	DTC activation enable register 115	DTCER115	8	8	2 ICLK	
0008 7174h	ICU	DTC activation enable register 116	DTCER116	8	8	2 ICLK	
0008 7175h	ICU	DTC activation enable register 117	DTCER117	8	8	2 ICLK	
0008 7179h	ICU	DTC activation enable register 121	DTCER121	8	8	2 ICLK	
0008 717Ah	ICU	DTC activation enable register 122	DTCER122	8	8	2 ICLK	
0008 717Dh	ICU	DTC activation enable register 125	DTCER125	8	8	2 ICLK	
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8	2 ICLK	
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8	2 ICLK	
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8	2 ICLK	
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8	2 ICLK	
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8	2 ICLK	
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8	2 ICLK	
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8	2 ICLK	
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8	2 ICLK	
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8	2 ICLK	
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8	2 ICLK	
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8	2 ICLK	
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8	2 ICLK	
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8	2 ICLK	
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8	2 ICLK	
0008 71AFh	ICU	DTC activation enable register 175	DTCER175	8	8	2 ICLK	
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8	2 ICLK	
0008 71B2h	ICU	DTC activation enable register 178	DTCER178	8	8	2 ICLK	
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8	2 ICLK	
0008 71B5h	ICU	DTC activation enable register 181	DTCER181	8	8	2 ICLK	
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8	2 ICLK	
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8	2 ICLK	
0008 71C6h	ICU	DTC activation enable register 198	DTCER198	8	8	2 ICLK	
0008 71C7h	ICU	DTC activation enable register 199	DTCER199	8	8	2 ICLK	
0008 71C8h	ICU	DTC activation enable register 200	DTCER200	8	8	2 ICLK	
0008 71C9h	ICU	DTC activation enable register 201	DTCER201	8	8	2 ICLK	
0008 71DBh	ICU	DTC activation enable register 219	DTCER219	8	8	2 ICLK	
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8	2 ICLK	
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8	2 ICLK	
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8	2 ICLK	
0008 71E3h	ICU	DTC activation enable register 227	DTCER227	8	8	2 ICLK	
0008 71E4h	ICU	DTC activation enable register 228	DTCER228	8	8	2 ICLK	
0008 71EBh	ICU	DTC activation enable register 235	DTCER235	8	8	2 ICLK	
0008 71ECh	ICU	DTC activation enable register 236	DTCER236	8	8	2 ICLK	
0008 71EFh	ICU	DTC activation enable register 239	DTCER239	8	8	2 ICLK	
0008 71F0h	ICU	DTC activation enable register 240	DTCER240	8	8	2 ICLK	
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8	2 ICLK	
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8	2 ICLK	
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (13 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 A0A0h	SCI5	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A1h	SCI5	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A2h	SCI5	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A3h	SCI5	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A4h	SCI5	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A5h	SCI5	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A6h	SCI5	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A7h	SCI5	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A8h	SCI5	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A9h	SCI5	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A0AAh	SCI5	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A0ABh	SCI5	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A0ACh	SCI5	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A0ADh	SCI5	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C0h	SCI6	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C1h	SCI6	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C2h	SCI6	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C3h	SCI6	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C4h	SCI6	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C5h	SCI6	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C6h	SCI6	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C7h	SCI6	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C8h	SCI6	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C9h	SCI6	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A0CAh	SCI6	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A0CBh	SCI6	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A0CCh	SCI6	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A0CDh	SCI6	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A121h	SCI9	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A122h	SCI9	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A123h	SCI9	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A124h	SCI9	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A125h	SCI9	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A126h	SCI9	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A127h	SCI9	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A128h	SCI9	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A129h	SCI9	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ah	SCI9	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A12Bh	SCI9	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ch	SCI9	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A12Dh	SCI9	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 B000h	CAC	CAC control register 0	CACR0	8	8	2, 3 PCLKB	2 ICLK
0008 B001h	CAC	CAC control register 1	CACR1	8	8	2, 3 PCLKB	2 ICLK
0008 B002h	CAC	CAC control register 2	CACR2	8	8	2, 3 PCLKB	2 ICLK
0008 B003h	CAC	CAC interrupt control register	CAICR	8	8	2, 3 PCLKB	2 ICLK
0008 B004h	CAC	CAC status register	CASTR	8	8	2, 3 PCLKB	2 ICLK
0008 B006h	CAC	CAC upper-limit value setting register	CAULVR	16	16	2, 3 PCLKB	2 ICLK
0008 B008h	CAC	CAC lower-limit value setting register	CALLVR	16	16	2, 3 PCLKB	2 ICLK
0008 B00Ah	CAC	CAC counter buffer register	CACNTBR	16	16	2, 3 PCLKB	2 ICLK
0008 B080h	DOC	DOC control register	DOCR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (14 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 B082h	DOC	DOC data input register	DODIR	16	16	2, 3 PCLKB	2 ICLK
0008 B084h	DOC	DOC data setting register	DODSR	16	16	2, 3 PCLKB	2 ICLK
0008 B100h	ELC	Event link control register	ELCR	8	8	2, 3 PCLKB	2 ICLK
0008 B102h	ELC	Event link setting register 1	ELSR1	8	8	2, 3 PCLKB	2 ICLK
0008 B103h	ELC	Event link setting register 2	ELSR2	8	8	2, 3 PCLKB	2 ICLK
0008 B104h	ELC	Event link setting register 3	ELSR3	8	8	2, 3 PCLKB	2 ICLK
0008 B105h	ELC	Event link setting register 4	ELSR4	8	8	2, 3 PCLKB	2 ICLK
0008 B10Bh	ELC	Event link setting register 10	ELSR10	8	8	2, 3 PCLKB	2 ICLK
0008 B10Dh	ELC	Event link setting register 12	ELSR12	8	8	2, 3 PCLKB	2 ICLK
0008 B110h	ELC	Event link setting register 15	ELSR15	8	8	2, 3 PCLKB	2 ICLK
0008 B113h	ELC	Event link setting register 18	ELSR18	8	8	2, 3 PCLKB	2 ICLK
0008 B115h	ELC	Event link setting register 20	ELSR20	8	8	2, 3 PCLKB	2 ICLK
0008 B117h	ELC	Event link setting register 22	ELSR22	8	8	2, 3 PCLKB	2 ICLK
0008 B119h	ELC	Event link setting register 24	ELSR24	8	8	2, 3 PCLKB	2 ICLK
0008 B11Ah	ELC	Event link setting register 25	ELSR25	8	8	2, 3 PCLKB	2 ICLK
0008 B11Fh	ELC	Event link option setting register A	ELOPA	8	8	2, 3 PCLKB	2 ICLK
0008 B120h	ELC	Event link option setting register B	ELOPB	8	8	2, 3 PCLKB	2 ICLK
0008 B122h	ELC	Event link option setting register D	ELOPD	8	8	2, 3 PCLKB	2 ICLK
0008 B123h	ELC	Port group setting register 1	PGR1	8	8	2, 3 PCLKB	2 ICLK
0008 B125h	ELC	Port group control register 1	PGC1	8	8	2, 3 PCLKB	2 ICLK
0008 B127h	ELC	Port buffer register 1	PDBF1	8	8	2, 3 PCLKB	2 ICLK
0008 B129h	ELC	Event link port setting register 0	PEL0	8	8	2, 3 PCLKB	2 ICLK
0008 B12Ah	ELC	Event link port setting register 1	PEL1	8	8	2, 3 PCLKB	2 ICLK
0008 B12Dh	ELC	Event link software event generation register	ELSEGR	8	8	2, 3 PCLKB	2 ICLK
0008 B300h	SCI12	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 B301h	SCI12	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 B302h	SCI12	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 B303h	SCI12	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 B304h	SCI12	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 B305h	SCI12	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 B306h	SCI12	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 B307h	SCI12	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 B308h	SCI12	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 B309h	SCI12	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 B30Ah	SCI12	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 B30Bh	SCI12	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 B30Ch	SCI12	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 B30Dh	SCI12	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 B320h	SCI12	Extended serial mode enable register	ESMER	8	8	2, 3 PCLKB	2 ICLK
0008 B321h	SCI12	Control register 0	CR0	8	8	2, 3 PCLKB	2 ICLK
0008 B322h	SCI12	Control register 1	CR1	8	8	2, 3 PCLKB	2 ICLK
0008 B323h	SCI12	Control register 2	CR2	8	8	2, 3 PCLKB	2 ICLK
0008 B324h	SCI12	Control register 3	CR3	8	8	2, 3 PCLKB	2 ICLK
0008 B325h	SCI12	Port control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 B326h	SCI12	Interrupt control register	ICR	8	8	2, 3 PCLKB	2 ICLK
0008 B327h	SCI12	Status register	STR	8	8	2, 3 PCLKB	2 ICLK
0008 B328h	SCI12	Status clear register	STCR	8	8	2, 3 PCLKB	2 ICLK
0008 B329h	SCI12	Control Field 0 data register	CF0DR	8	8	2, 3 PCLKB	2 ICLK
0008 B32Ah	SCI12	Control Field 0 compare enable register	CF0CR	8	8	2, 3 PCLKB	2 ICLK
0008 B32Bh	SCI12	Control Field 0 receive data register	CF0RR	8	8	2, 3 PCLKB	2 ICLK
0008 B32Ch	SCI12	Primary control field 1 data register	PCF1DR	8	8	2, 3 PCLKB	2 ICLK

Table 5.4 DC Characteristics (3)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

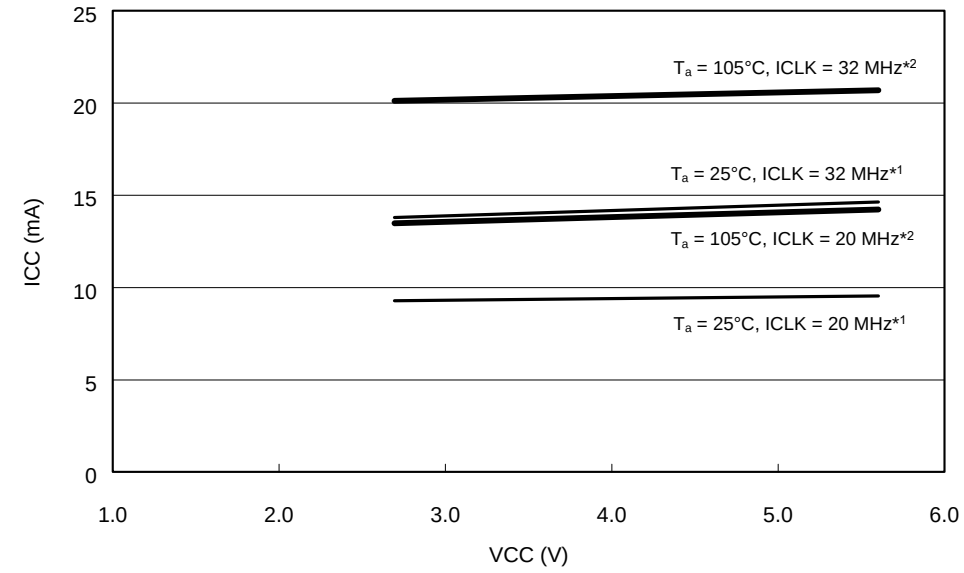
Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD pin, P35/NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Other pins except for ports for 5 V tolerant	$\lvert I_{TSI} \rvert$	—	—	0.2	µA	V_{in} = 0 V, VCC
	Ports for 5 V tolerant		—	—	1.0		V_{in} = 0 V, 5.8 V
Input capacitance	All input pins (except for XCIN and XCOUT)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	XCIN and XCOUT		—	—	3		

Table 5.5 DC Characteristics (4)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

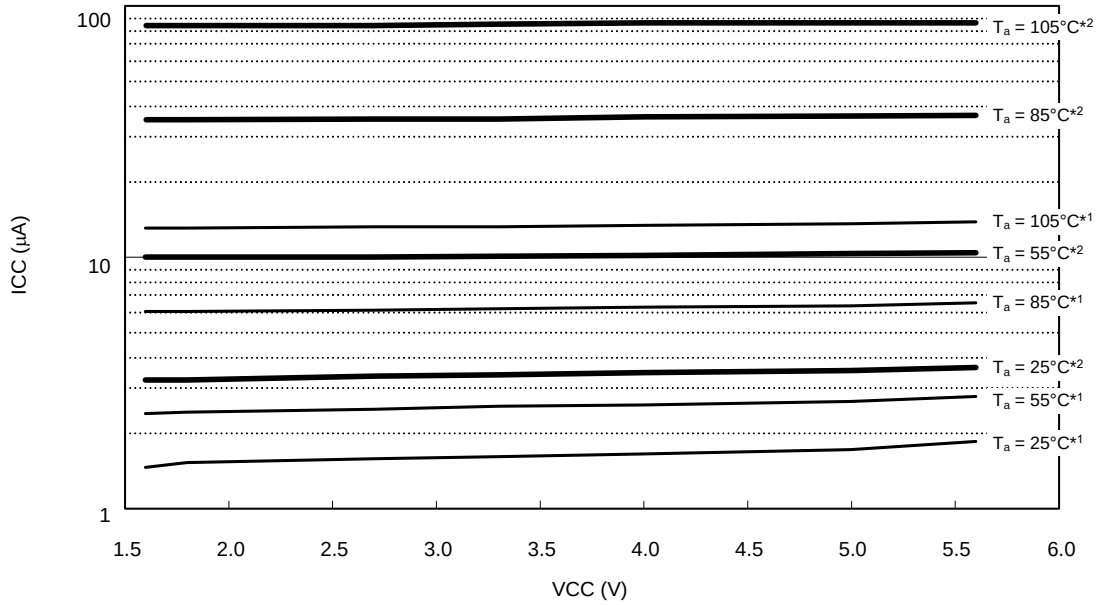
Item		Symbol	VCC						Unit	Test Conditions
			1.62 to 2.7 V		2.7 to 4.0 V		4.0 to 5.5 V			
			Min.	Max.	Min.	Max.	Min.	Max.		
Input pull-up MOS current	All ports (except for port 35)	I_p	–150	–5	–200	–10	–400	–50	µA	V_{in} = 0 V

Note 5. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO. BCLK, FCLK, and PCLK are set to divided by 64.
Note 6. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 7. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 9. VCC = 3.3 V.



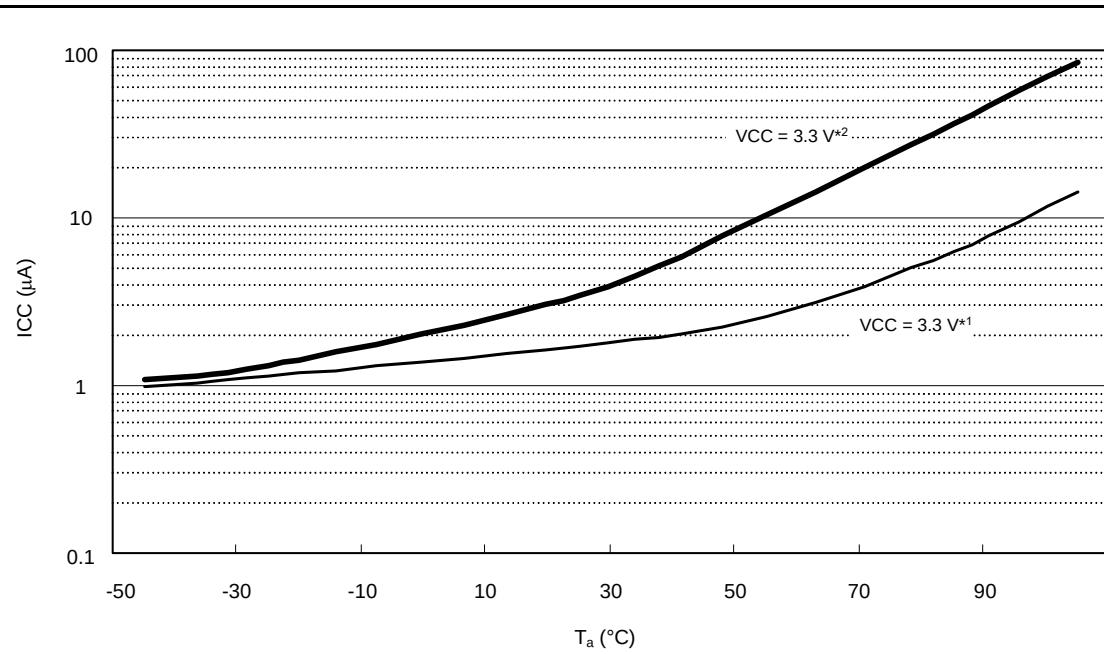
Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.1 Voltage Dependency in Medium-Speed Operating Modes 1A and 1B (Reference Data)



Note 1. Average value of the tested middle samples during product evaluation
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.4 Voltage Dependency in Software Standby Mode (SOFTCUT Bit = 11xb) (Reference Data)



Note 1. Average value of the tested middle samples during product evaluation
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.5 Temperature Dependency in Software Standby Mode (SOFTCUT Bit = 11xb) (Reference Data)

Table 5.8 DC Characteristics (7)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	Pd	—	350	mW	T_a = –40 to 85°C
		—	150		85°C < T_a ≤ 105°C

Note: • Please contact Renesas Electronics sales office for derating of operation under T_a = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.9 DC Characteristics (8)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VREFH0 = 1.62 to AVCC0, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion	Conversion time = 1.56 µs	AI_{CC}	—	1.0	3.0	mA	
	Waiting for A/D conversion (all units)			—	0.2	3.0	µA	
Reference power supply current	During A/D conversion	Conversion time = 1.56 µs	I_{REFH0}	—	0.1	0.2	mA	
	Waiting for A/D conversion (all units)			—	0.2	0.4	µA	

Table 5.10 DC Characteristics (9)

Conditions: VCC = AVCC0, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.62	—	—	V	

Table 5.11 DC Characteristics (10)

Conditions: VCC = AVCC0 = 0 to 5.5 V, VREFH0 = 0 to AVCC0, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VCC rising gradient	SrVCC	0.02	—	20	ms/V	At cold start

Table 5.12 DC Characteristics (11)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (1.62 V).

When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r(VCC)}$	—	—	10	kHz	VCC × 0.1 < $V_{r(VCC)}$ ≤ VCC × 0.2
		—	—	1	MHz	VCC × 0.05 < $V_{r(VCC)}$ ≤ VCC × 0.1
		—	—	10	MHz	$V_{r(VCC)}$ ≤ VCC × 0.05
Allowable voltage change rising/ falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

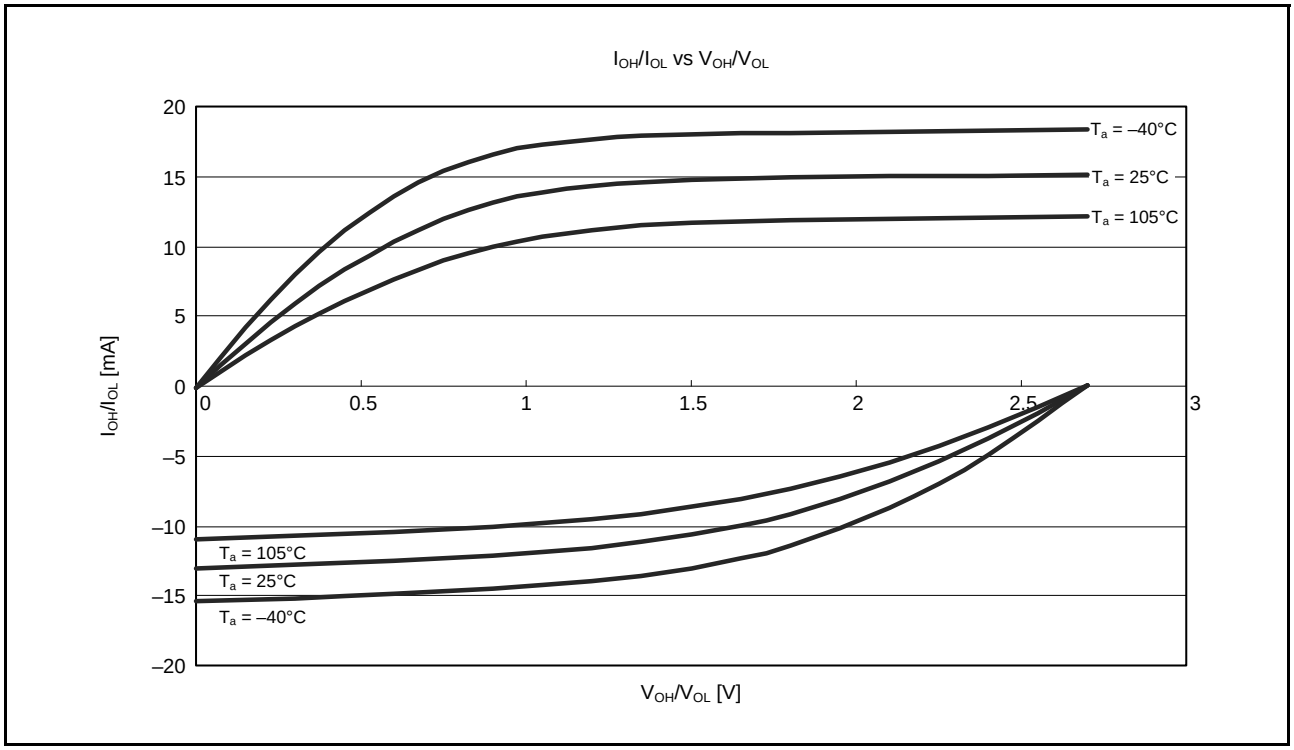


Figure 5.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V when Normal Output is Selected (Reference Data)

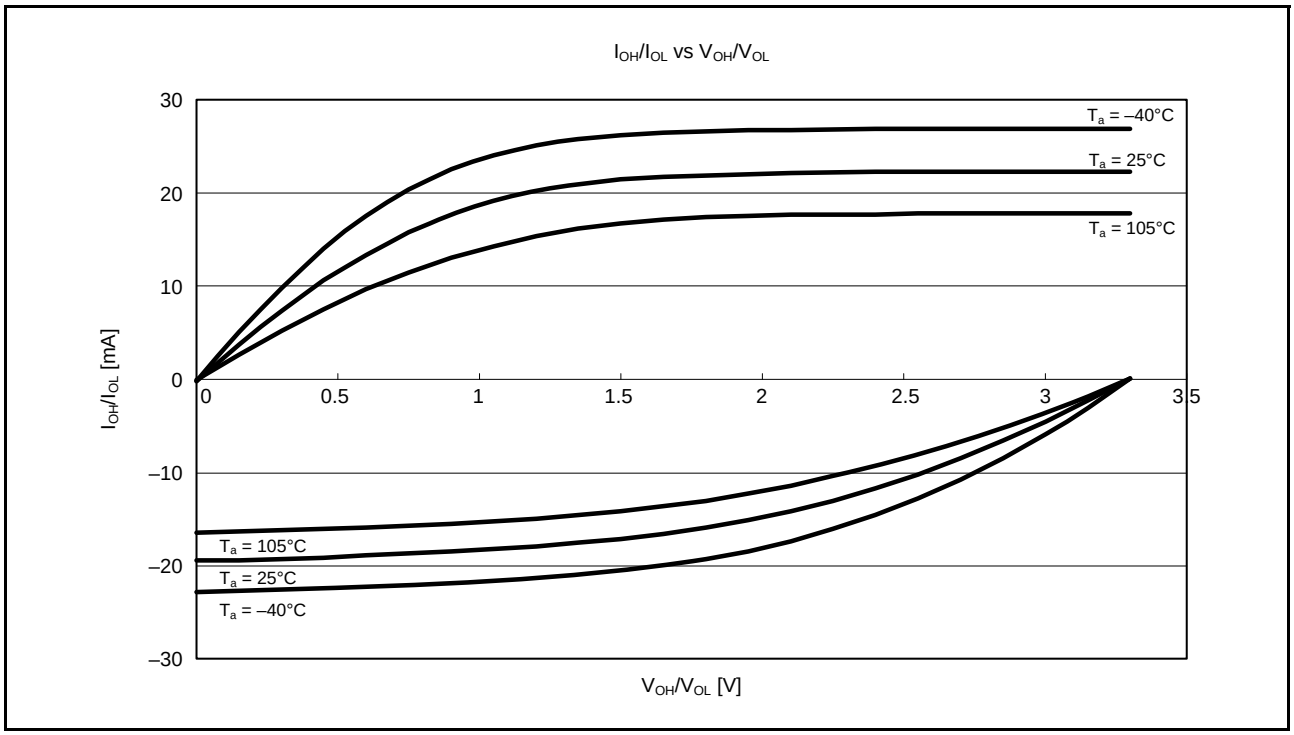


Figure 5.10 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 3.3 V when Normal Output is Selected (Reference Data)

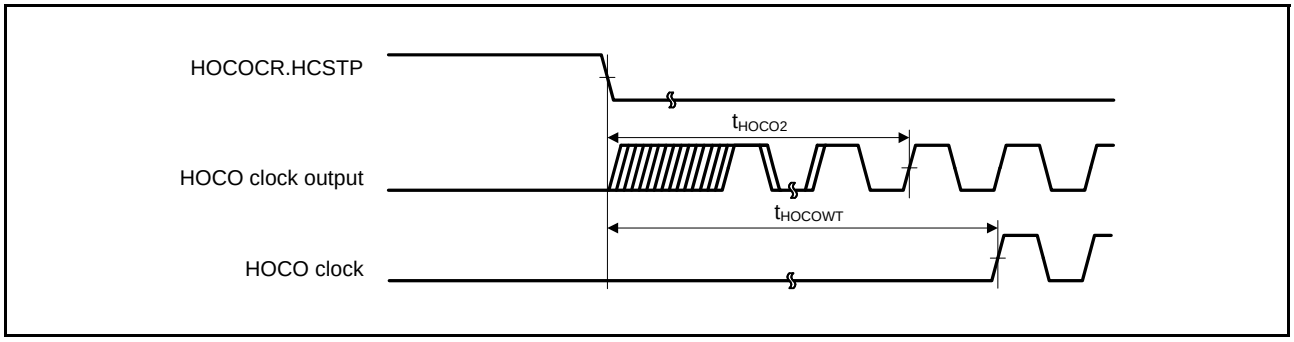


Figure 5.25 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

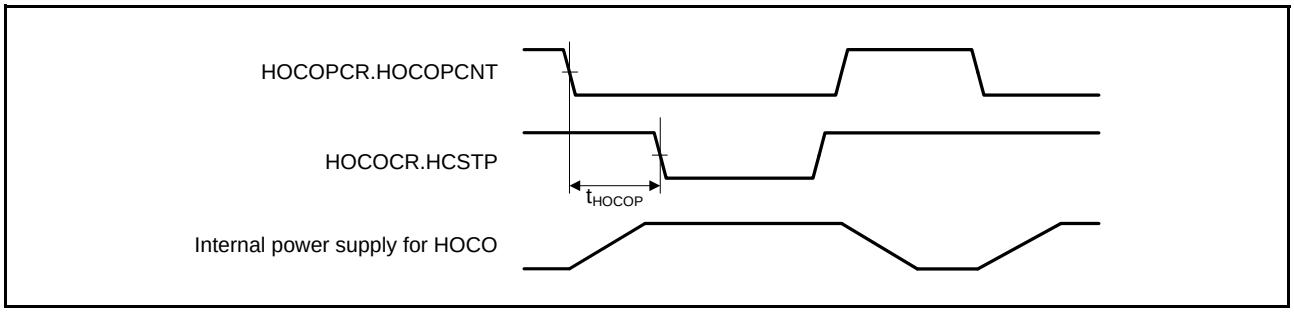


Figure 5.26 HOCO Power Control Timing

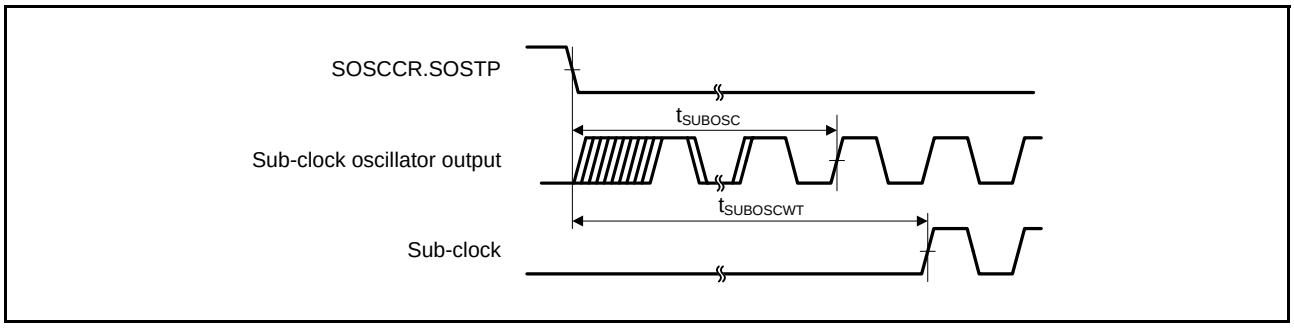


Figure 5.27 Sub-clock Oscillation Start Timing

5.3.4 Control Signal Timing

Table 5.25 Control Signal Timing

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_{c(PCLKB)} \times 2 \leq 200$ ns, Figure 5.31
		$t_{c(PCLKB)} \times 2$	—	—	ns	$t_{c(PCLKB)} \times 2 > 200$ ns, Figure 5.31
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_{c(PCLKB)} \times 2 \leq 200$ ns, Figure 5.32
		$t_{c(PCLKB)} \times 2$	—	—	ns	$t_{c(PCLKB)} \times 2 > 200$ ns, Figure 5.32

Note: • 200 ns minimum in software standby mode.

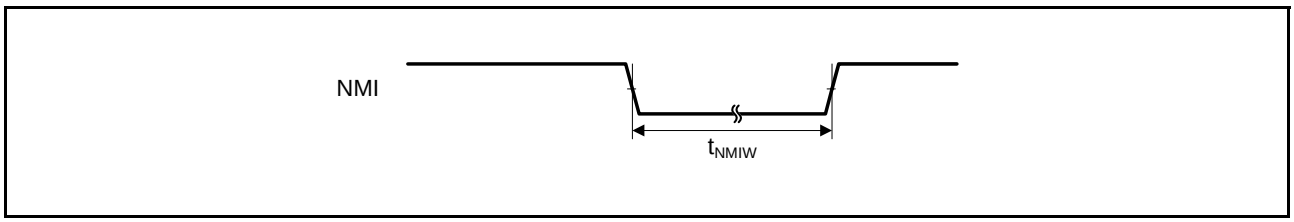


Figure 5.31 NMI Interrupt Input Timing

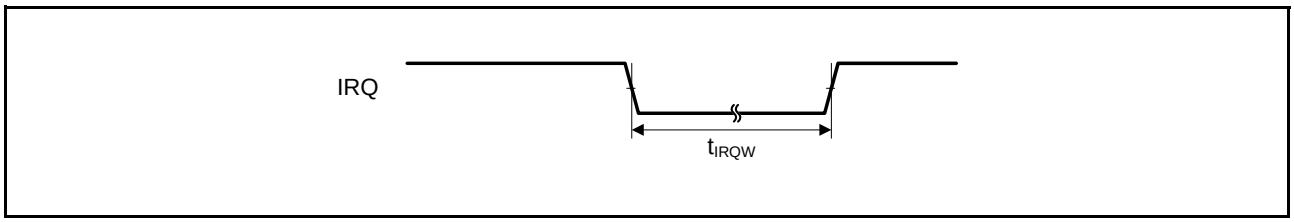


Figure 5.32 IRQ Interrupt Input Timing

Table 5.27 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle*2	Master		t_{SPcyc}	2	4096	t_{Pcyc}	C = 30 pF Figure 5.41
		Slave			8	4096		
	RSPCK clock high pulse width*2	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width*2	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time*2	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.62 V ≤ VCC < 2.7 V		—	20		
		Input			—	1	µs	
	Data input setup time	Master		t_{SU}	4	—	ns	C = 30 pF Figure 5.42 to Figure 5.47
		Slave			$20 - t_{Pcyc}$	—		
	Data input hold time	Master	PCLKB set to a division ratio other than divided by 2	t_H	t_{Pcyc}	—	ns	
			PCLKB set to divided by 2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OD}	—	14	ns	
			1.62 V ≤ VCC < 2.7 V		—	28		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		—	$3 \times t_{Pcyc} + 40$		
			1.62 V ≤ VCC < 2.7 V		—	$3 \times t_{Pcyc} + 80$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	10	ns	
			1.62 V ≤ VCC < 2.7 V		—	20		
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	20	ns	
		Input			—	1	µs	
	Slave access time			t_{SA}	—	4	t_{Pcyc}	C = 30 pF Figure 5.45 and Figure 5.47
	Slave output release time			t_{REL}	—	3	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLKB cycle
Note 2. Value when the drive capacity of clock output ports is set to normal output.

Table 5.28 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)*2		t_{SPcyc}	4	65536	t_{Pcyc}	C = 30 pF Figure 5.41
	SCK clock cycle input (slave)			6	65536		
	SCK clock high pulse width*2		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width*2		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	40	—	ns	C = 30 pF Figure 5.42 to Figure 5.47
		1.62 V ≤ VCC < 2.7 V		80	—		
	Data input hold time		t_H	40	—	ns	
	SS input setup time		t_{LEAD}	6	—	t_{Pcyc}	
	SS input hold time		t_{LAG}	6	—	t_{Pcyc}	
	Data output delay time	2.7 V ≤ VCC ≤ 5.5 V	t_{OD}	—	40	ns	
		1.62 V ≤ VCC < 2.7 V		—	80		
	Data output hold time		t_{OH}	0	—	ns	
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	5	t_{Pcyc}	C = 30 pF Figure 5.45 and Figure 5.47
	Slave output release time		t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLKB cycle
Note 2. Value when the drive capacity of clock output ports is set to normal output.

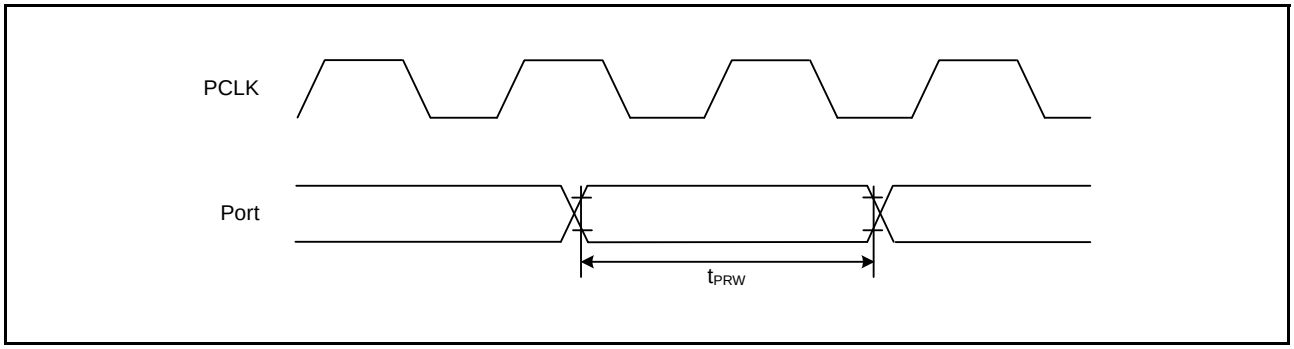


Figure 5.33 I/O Port Input Timing

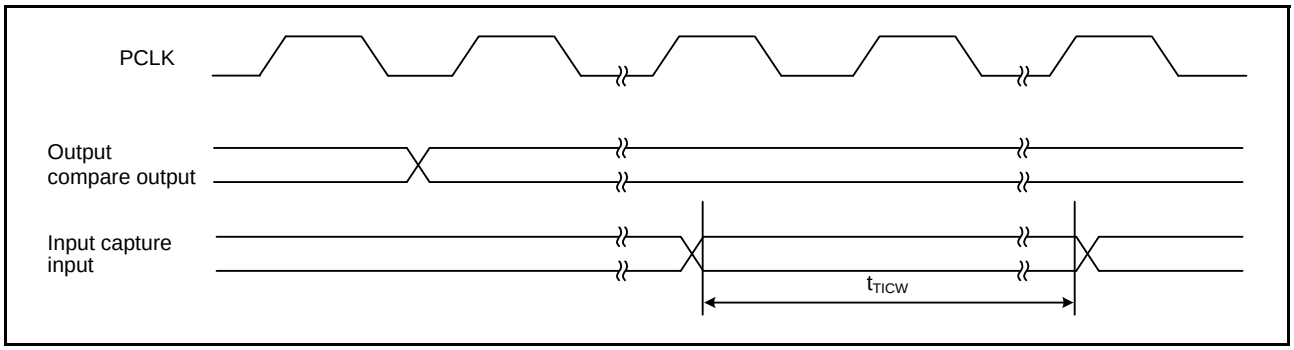


Figure 5.34 MTU Input/Output Timing

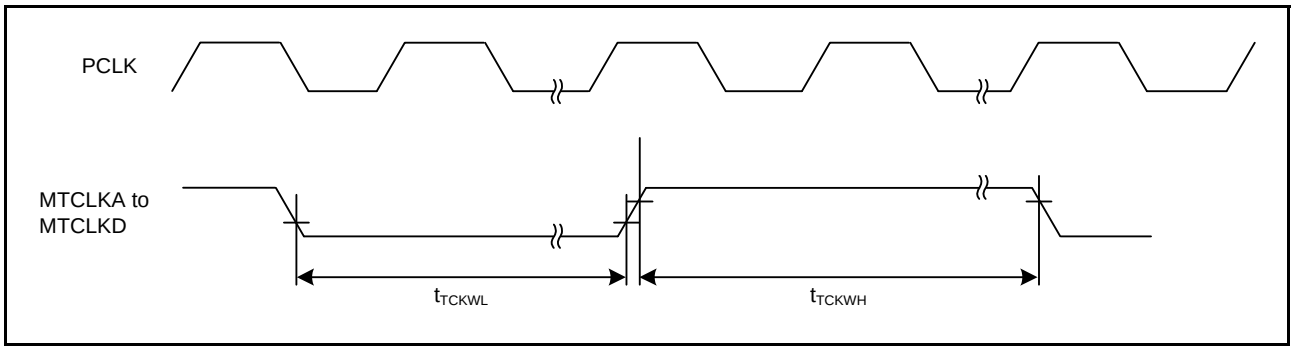


Figure 5.35 MTU Clock Input Timing

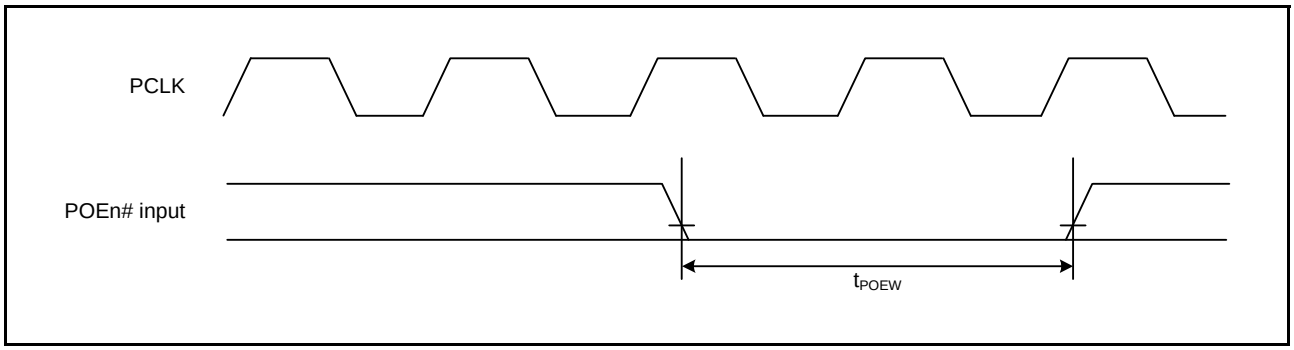


Figure 5.36 POE# Input Timing

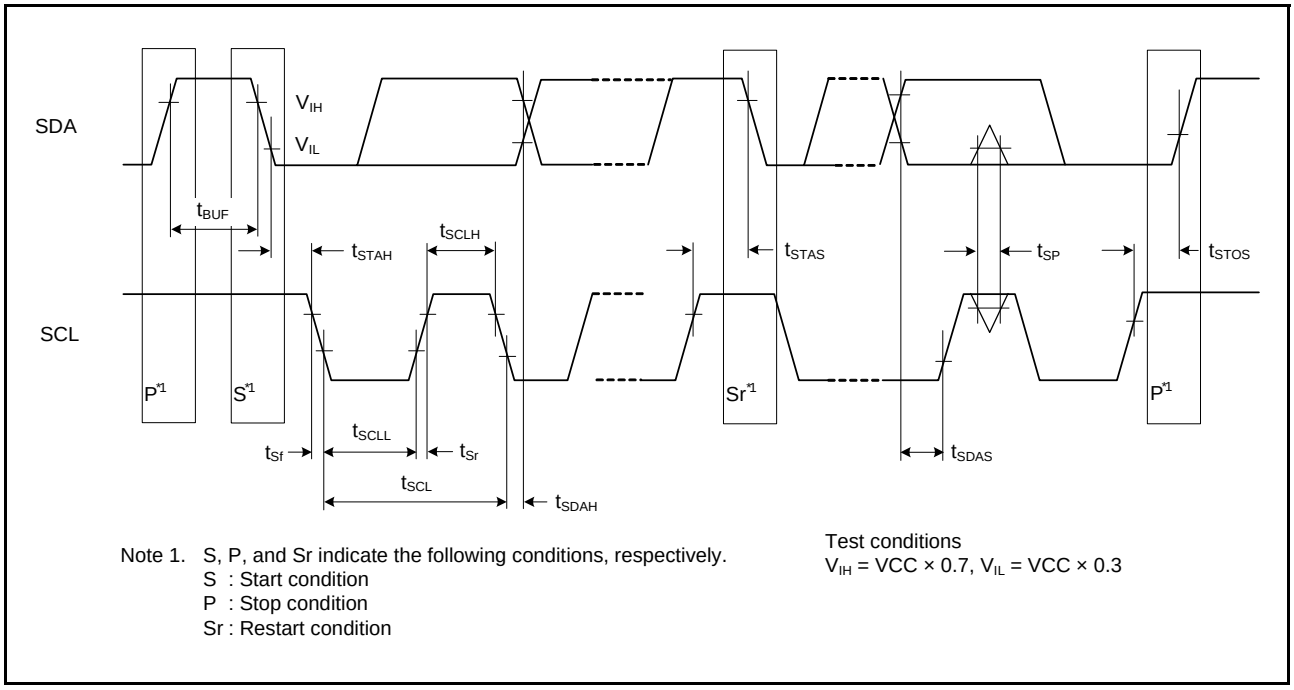


Figure 5.48 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

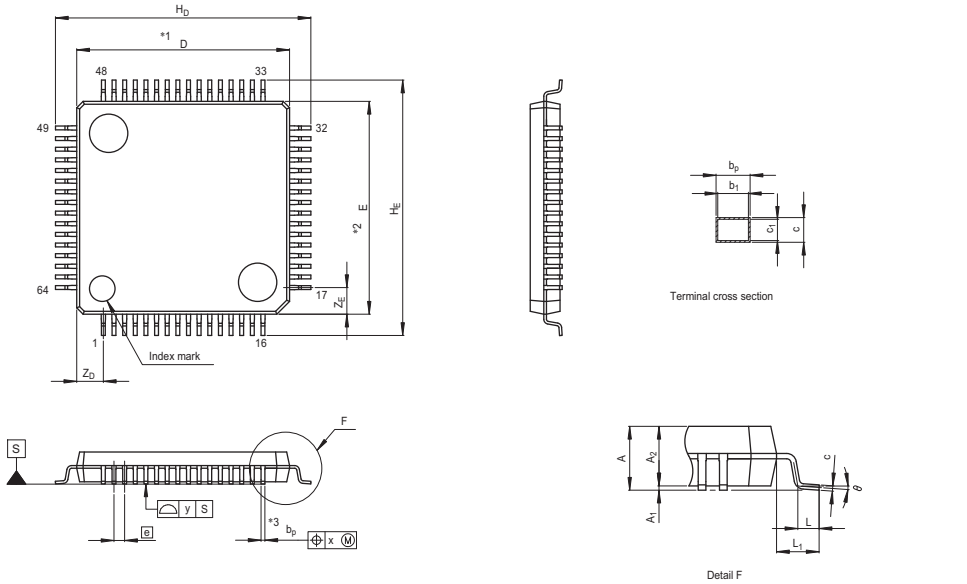
Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure B 64-Pin LQFP (PLQP0064KB-A)