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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52206bdfl-30

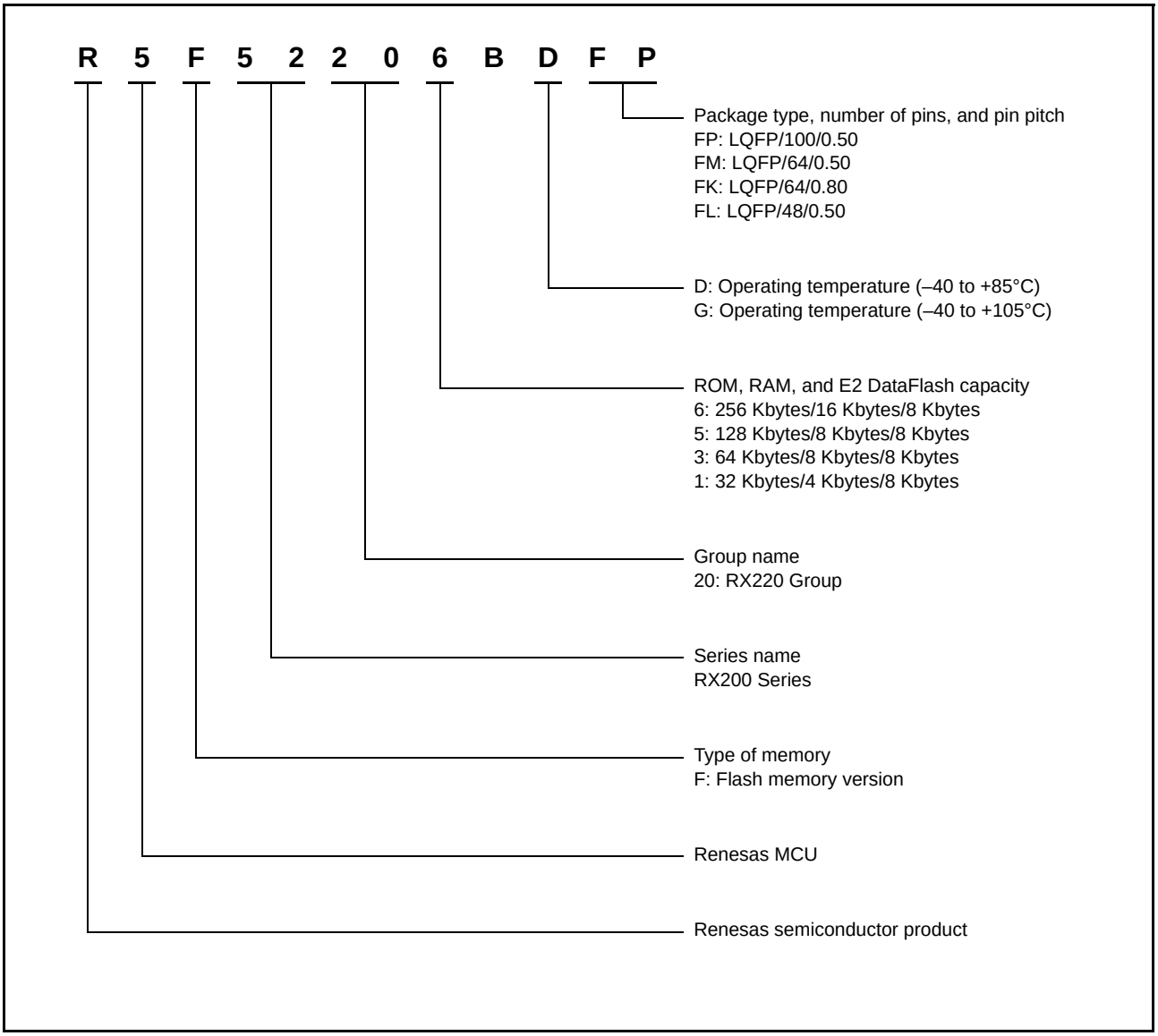
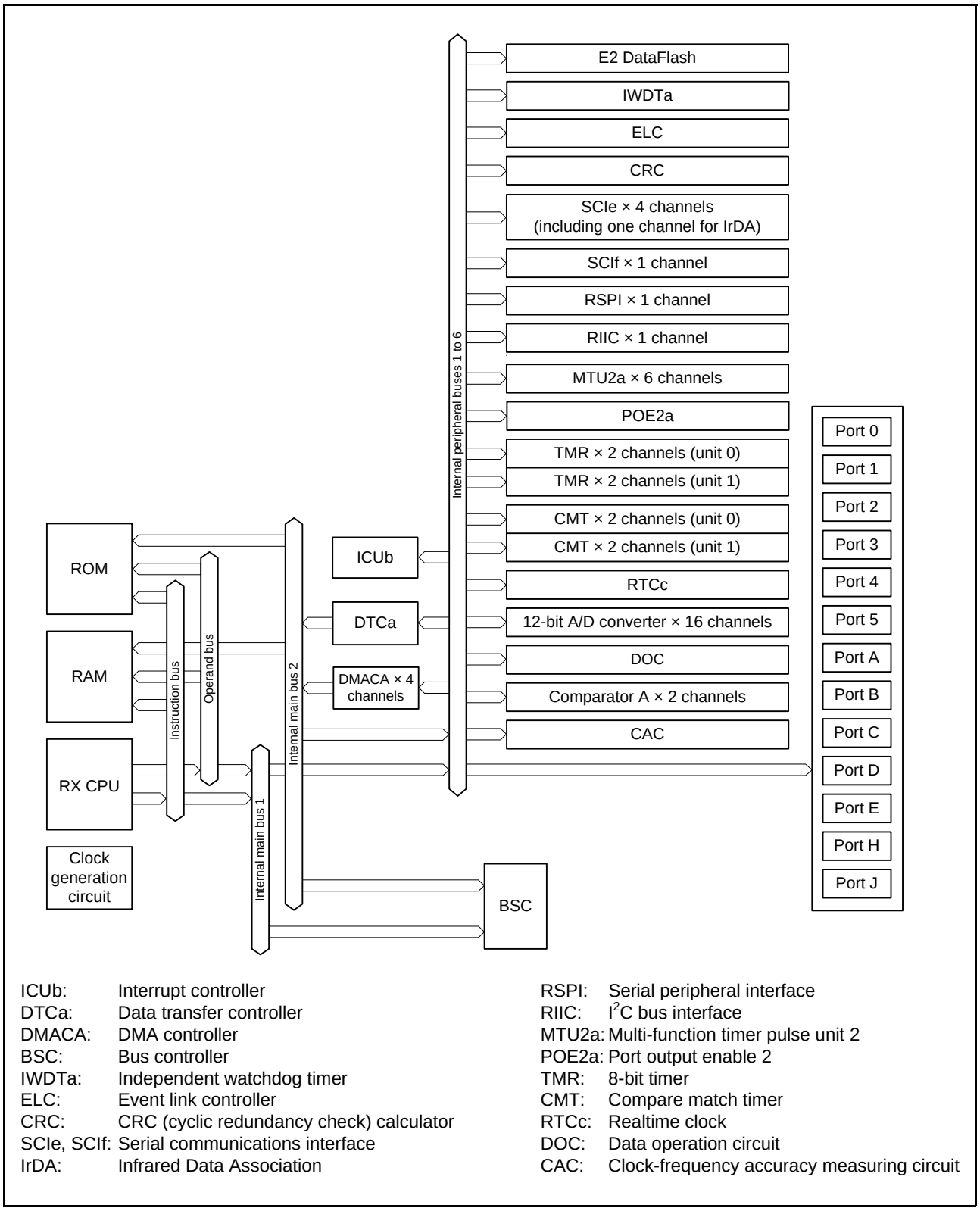


Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type

1.3 Block Diagram

Figure 1.2 shows a block diagram.



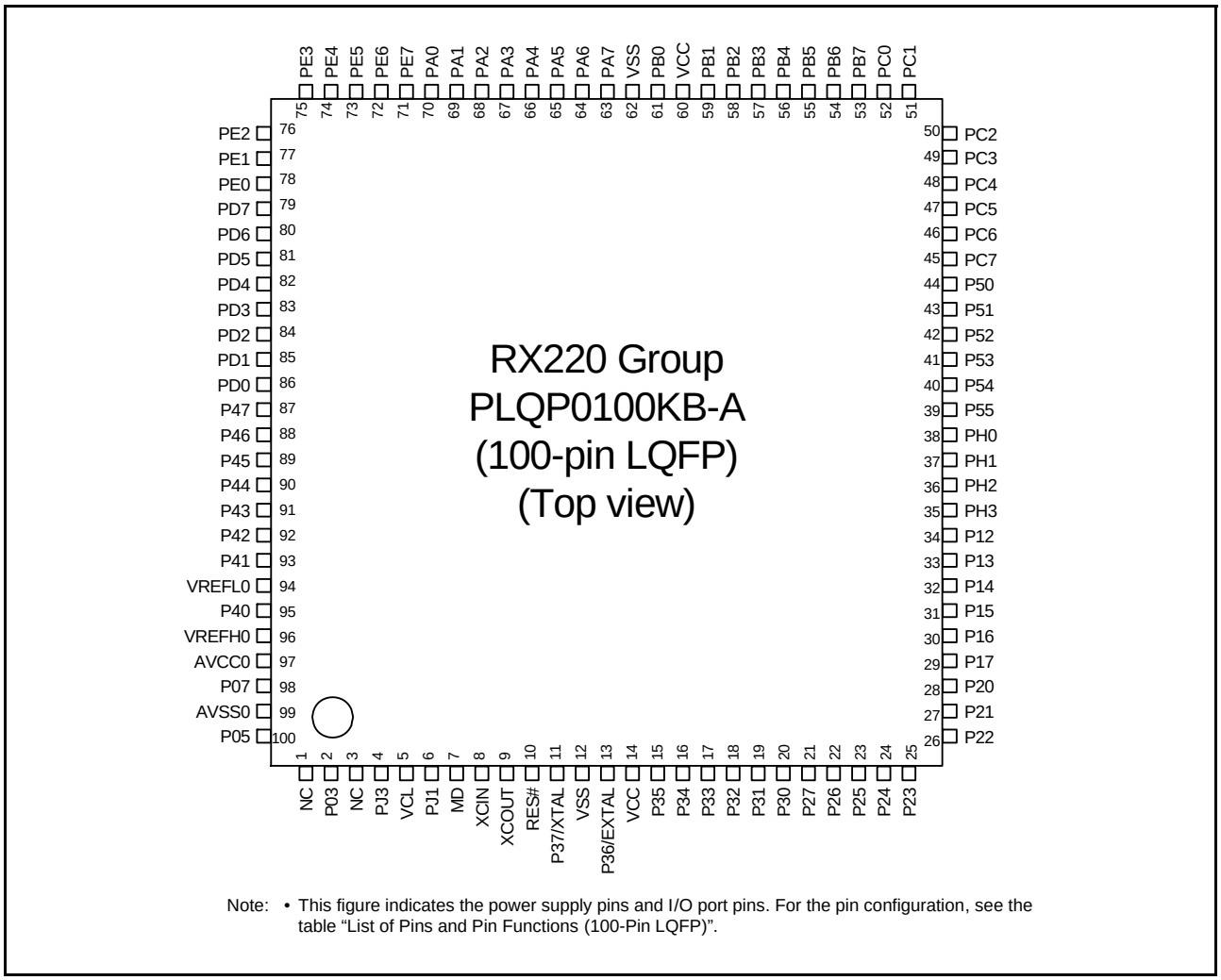
ICUb: Interrupt controller
DTCa: Data transfer controller
DMACA: DMA controller
BSC: Bus controller
IWDTa: Independent watchdog timer
ELC: Event link controller
CRC: CRC (cyclic redundancy check) calculator
SCIe, SCIf: Serial communications interface
IrDA: Infrared Data Association

RSPI: Serial peripheral interface
RIIC: I^2C bus interface
MTU2a: Multi-function timer pulse unit 2
POE2a: Port output enable 2
TMR: 8-bit timer
CMT: Compare match timer
RTCc: Realtime clock
DOC: Data operation circuit
CAC: Clock-frequency accuracy measuring circuit

Figure 1.2 Block Diagram

1.5 Pin Assignments

Figure 1.3 to Figure 1.5 show the pin assignments. Table 1.5 to Table 1.7 show the lists of pins and pin functions.



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin LQFP)”.

Figure 1.3 Pin Assignments of the 100-Pin LQFP

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIe, SCIf, RSPI, RIIC)	Others
1	NC (Non-Connection)				
2		P03			
3	NC (Non-Connection)				
4		PJ3	MTIOC3C	CTS6#/RTS6#/SS6#	
5	VCL				
6		PJ1	MTIOC3A		
7	MD				FINED
8	XCIN				
9	XCOUT				
10	RES#				
11	XTAL	P37			
12	VSS				
13	EXTAL	P36			
14	VCC				
15		P35			NMI
16		P34	MTIOC0A/TMCI3/POE2#	SCK6	IRQ4
17		P33	MTIOC0D/TMRI3/POE3#	RXD6/SMISO6/SSCL6	IRQ3
18		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2/RTCOUT
19		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1
20		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	IRQ0
21		P27	MTIOC2B/TMCI3	SCK1	
22		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
23		P25	MTIOC4C/MTCLKB		ADTRG0#
24		P24	MTIOC4A/MTCLKA/TMRI1		
25		P23	MTIOC3D/MTCLKD		
26		P22	MTIOC3B/MTCLKC/TMO0		
27		P21	MTIOC1B/TMCI0		
28		P20	MTIOC1A/TMRI0		
29		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA	IRQ7
30		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL	IRQ6/RTCOUT/ADTRG0#
31		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
32		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
33		P13	MTIOC0B/TMO3	SDA	IRQ3
34		P12	TMCI1	SCL	IRQ2
35		PH3	TMCI0		
36		PH2	TMRI0		IRQ1
37		PH1	TMO0		IRQ0
38		PH0			CACREF
39		P55	MTIOC4D/TMO3		
40		P54	MTIOC4B/TMCI1		
41		P53			
42		P52			
43		P51			
44		P50			
45		PC7	MTIOC3A/TMO2/MTCLKB	MISOA	CACREF
46		PC6	MTIOC3C/MTCLKA/TMCI2	MOSIA	
47		PC5	MTIOC3B/MTCLKD/TMRI2	RSPCKA	

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16		3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16		3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16		3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16		3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32		3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32		3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32		3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32		3 ICLK
0008 0026h	SYSTEM	System clock control register 3	SCKCR3	16	16		3 ICLK
0008 0032h	SYSTEM	Main clock oscillator control register	MOSCCR	8	8		3 ICLK
0008 0033h	SYSTEM	Sub-clock oscillator control register	SOSCCR	8	8		3 ICLK
0008 0035h	SYSTEM	IWDT-dedicated on-chip oscillator control register	ILOCOCR	8	8		3 ICLK
0008 0036h	SYSTEM	High-speed on-chip oscillator control register	HOCOCR	8	8		3 ICLK
0008 0037h	SYSTEM	High-speed on-chip oscillator control register 2	HOCOCR2	8	8		3 ICLK
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	8	8		3 ICLK
0008 0041h	SYSTEM	Oscillation stop detection status register	OSTDSR	8	8		3 ICLK
0008 00A0h	SYSTEM	Operating power control register	OPCCR	8	8		3 ICLK
0008 00A1h	SYSTEM	Sleep mode return clock source switching register	RSTCKCR	8	8		3 ICLK
0008 00A2h	SYSTEM	Main clock oscillator wait control register	MOSCWTCR	8	8		3 ICLK
0008 00A3h	SYSTEM	Sub-clock oscillator wait control register	SOSCWTCR	8	8		3 ICLK
0008 00A9h	SYSTEM	HOCO wait control register 2	HOCOWTCR2	8	8		3 ICLK
0008 00C0h	SYSTEM	Reset status register 2	RSTSR2	8	8		3 ICLK
0008 00C2h	SYSTEM	Software reset register	SWRR	16	16		3 ICLK
0008 00E0h	SYSTEM	Voltage monitoring 1 circuit/comparator A1 control register 1	LVD1CR1	8	8		3 ICLK
0008 00E1h	SYSTEM	Voltage monitoring 1 circuit/comparator A1 status register	LVD1SR	8	8		3 ICLK
0008 00E2h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 control register 1	LVD2CR1	8	8		3 ICLK
0008 00E3h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 status register	LVD2SR	8	8		3 ICLK
0008 03FEh	SYSTEM	Protect register	PRCR	16	16		3 ICLK
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8		2 ICLK
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8		2 ICLK
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8		2 ICLK
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16		2 ICLK
0008 1310h	BSC	Bus priority control register	BUSPRI	16	16		2 ICLK
0008 2000h	DMAC0	DMA source address register	DMSAR	32	32		2 ICLK
0008 2004h	DMAC0	DMA destination address register	DMDAR	32	32		2 ICLK
0008 2008h	DMAC0	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 200Ch	DMAC0	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 2010h	DMAC0	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 2013h	DMAC0	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 2014h	DMAC0	DMA address mode register	DMAMD	16	16		2 ICLK
0008 2018h	DMAC0	DMA offset register	DMOFR	32	32		2 ICLK
0008 201Ch	DMAC0	DMA transfer enable register	DMCNT	8	8		2 ICLK
0008 201Dh	DMAC0	DMA software start register	DMREQ	8	8		2 ICLK
0008 201Eh	DMAC0	DMA status register	DMSTS	8	8		2 ICLK
0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 2040h	DMAC1	DMA source address register	DMSAR	32	32		2 ICLK
0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32		2 ICLK
0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (3 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 703Fh	ICU	Interrupt request register 063	IR063	8	8	2 ICLK	
0008 7040h	ICU	Interrupt request register 064	IR064	8	8	2 ICLK	
0008 7041h	ICU	Interrupt request register 065	IR065	8	8	2 ICLK	
0008 7042h	ICU	Interrupt request register 066	IR066	8	8	2 ICLK	
0008 7043h	ICU	Interrupt request register 067	IR067	8	8	2 ICLK	
0008 7044h	ICU	Interrupt request register 068	IR068	8	8	2 ICLK	
0008 7045h	ICU	Interrupt request register 069	IR069	8	8	2 ICLK	
0008 7046h	ICU	Interrupt request register 070	IR070	8	8	2 ICLK	
0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2 ICLK	
0008 7058h	ICU	Interrupt request register 088	IR088	8	8	2 ICLK	
0008 7059h	ICU	Interrupt request register 089	IR089	8	8	2 ICLK	
0008 705Ch	ICU	Interrupt request register 092	IR092	8	8	2 ICLK	
0008 705Dh	ICU	Interrupt request register 093	IR093	8	8	2 ICLK	
0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2 ICLK	
0008 7067h	ICU	Interrupt request register 103	IR103	8	8	2 ICLK	
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8	2 ICLK	
0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2 ICLK	
0008 7073h	ICU	Interrupt request register 115	IR115	8	8	2 ICLK	
0008 7074h	ICU	Interrupt request register 116	IR116	8	8	2 ICLK	
0008 7075h	ICU	Interrupt request register 117	IR117	8	8	2 ICLK	
0008 7076h	ICU	Interrupt request register 118	IR118	8	8	2 ICLK	
0008 7077h	ICU	Interrupt request register 119	IR119	8	8	2 ICLK	
0008 7078h	ICU	Interrupt request register 120	IR120	8	8	2 ICLK	
0008 7079h	ICU	Interrupt request register 121	IR121	8	8	2 ICLK	
0008 707Ah	ICU	Interrupt request register 122	IR122	8	8	2 ICLK	
0008 707Bh	ICU	Interrupt request register 123	IR123	8	8	2 ICLK	
0008 707Ch	ICU	Interrupt request register 124	IR124	8	8	2 ICLK	
0008 707Dh	ICU	Interrupt request register 125	IR125	8	8	2 ICLK	
0008 707Eh	ICU	Interrupt request register 126	IR126	8	8	2 ICLK	
0008 707Fh	ICU	Interrupt request register 127	IR127	8	8	2 ICLK	
0008 7080h	ICU	Interrupt request register 128	IR128	8	8	2 ICLK	
0008 7081h	ICU	Interrupt request register 129	IR129	8	8	2 ICLK	
0008 7082h	ICU	Interrupt request register 130	IR130	8	8	2 ICLK	
0008 7083h	ICU	Interrupt request register 131	IR131	8	8	2 ICLK	
0008 7084h	ICU	Interrupt request register 132	IR132	8	8	2 ICLK	
0008 7085h	ICU	Interrupt request register 133	IR133	8	8	2 ICLK	
0008 7086h	ICU	Interrupt request register 134	IR134	8	8	2 ICLK	
0008 7087h	ICU	Interrupt request register 135	IR135	8	8	2 ICLK	
0008 7088h	ICU	Interrupt request register 136	IR136	8	8	2 ICLK	
0008 7089h	ICU	Interrupt request register 137	IR137	8	8	2 ICLK	
0008 708Ah	ICU	Interrupt request register 138	IR138	8	8	2 ICLK	
0008 708Bh	ICU	Interrupt request register 139	IR139	8	8	2 ICLK	
0008 708Ch	ICU	Interrupt request register 140	IR140	8	8	2 ICLK	
0008 708Dh	ICU	Interrupt request register 141	IR141	8	8	2 ICLK	
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8	2 ICLK	
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8	2 ICLK	
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8	2 ICLK	
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8	2 ICLK	
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8	2 ICLK	
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8	2 ICLK	
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (5 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK	
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK	
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK	
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK	
0008 7167h	ICU	DTC activation enable register 103	DTCER103	8	8	2 ICLK	
0008 716Ah	ICU	DTC activation enable register 106	DTCER106	8	8	2 ICLK	
0008 7172h	ICU	DTC activation enable register 114	DTCER114	8	8	2 ICLK	
0008 7173h	ICU	DTC activation enable register 115	DTCER115	8	8	2 ICLK	
0008 7174h	ICU	DTC activation enable register 116	DTCER116	8	8	2 ICLK	
0008 7175h	ICU	DTC activation enable register 117	DTCER117	8	8	2 ICLK	
0008 7179h	ICU	DTC activation enable register 121	DTCER121	8	8	2 ICLK	
0008 717Ah	ICU	DTC activation enable register 122	DTCER122	8	8	2 ICLK	
0008 717Dh	ICU	DTC activation enable register 125	DTCER125	8	8	2 ICLK	
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8	2 ICLK	
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8	2 ICLK	
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8	2 ICLK	
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8	2 ICLK	
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8	2 ICLK	
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8	2 ICLK	
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8	2 ICLK	
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8	2 ICLK	
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8	2 ICLK	
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8	2 ICLK	
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8	2 ICLK	
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8	2 ICLK	
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8	2 ICLK	
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8	2 ICLK	
0008 71AFh	ICU	DTC activation enable register 175	DTCER175	8	8	2 ICLK	
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8	2 ICLK	
0008 71B2h	ICU	DTC activation enable register 178	DTCER178	8	8	2 ICLK	
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8	2 ICLK	
0008 71B5h	ICU	DTC activation enable register 181	DTCER181	8	8	2 ICLK	
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8	2 ICLK	
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8	2 ICLK	
0008 71C6h	ICU	DTC activation enable register 198	DTCER198	8	8	2 ICLK	
0008 71C7h	ICU	DTC activation enable register 199	DTCER199	8	8	2 ICLK	
0008 71C8h	ICU	DTC activation enable register 200	DTCER200	8	8	2 ICLK	
0008 71C9h	ICU	DTC activation enable register 201	DTCER201	8	8	2 ICLK	
0008 71DBh	ICU	DTC activation enable register 219	DTCER219	8	8	2 ICLK	
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8	2 ICLK	
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8	2 ICLK	
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8	2 ICLK	
0008 71E3h	ICU	DTC activation enable register 227	DTCER227	8	8	2 ICLK	
0008 71E4h	ICU	DTC activation enable register 228	DTCER228	8	8	2 ICLK	
0008 71EBh	ICU	DTC activation enable register 235	DTCER235	8	8	2 ICLK	
0008 71ECh	ICU	DTC activation enable register 236	DTCER236	8	8	2 ICLK	
0008 71EFh	ICU	DTC activation enable register 239	DTCER239	8	8	2 ICLK	
0008 71F0h	ICU	DTC activation enable register 240	DTCER240	8	8	2 ICLK	
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8	2 ICLK	
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8	2 ICLK	
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (9 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK
0008 8300h	RIIC0	I2C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK
0008 8301h	RIIC0	I2C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8302h	RIIC0	I2C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK
0008 8303h	RIIC0	I2C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK
0008 8304h	RIIC0	I2C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK
0008 8305h	RIIC0	I2C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK
0008 8306h	RIIC0	I2C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK
0008 8307h	RIIC0	I2C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK
0008 8308h	RIIC0	I2C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK
0008 8309h	RIIC0	I2C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK
0008 830Ah	RIIC0	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK
0008 830Ah	RIIC0	Timeout internal counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK
0008 830Bh	RIIC0	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK
0008 830Bh	RIIC0	Timeout internal counter U	TMOCNTU	8	8*2	2, 3 PCLKB	2 ICLK
0008 830Ch	RIIC0	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK
0008 8310h	RIIC0	I2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK
0008 8311h	RIIC0	I2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK
0008 8312h	RIIC0	I2C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK
0008 8313h	RIIC0	I2C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK
0008 8380h	RSPI0	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK
0008 8381h	RSPI0	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK
0008 8382h	RSPI0	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK
0008 8383h	RSPI0	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK
0008 8384h	RSPI0	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK
0008 8388h	RSPI0	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK
0008 8389h	RSPI0	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK
0008 838Ah	RSPI0	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK
0008 838Bh	RSPI0	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK
0008 838Ch	RSPI0	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK
0008 838Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK
0008 838Eh	RSPI0	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK
0008 838Fh	RSPI0	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8390h	RSPI0	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK
0008 8392h	RSPI0	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK
0008 8394h	RSPI0	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK
0008 8396h	RSPI0	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK
0008 8398h	RSPI0	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK
0008 839Ah	RSPI0	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK
0008 839Ch	RSPI0	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK
0008 839Eh	RSPI0	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK
0008 8410h	IRDA	IrDA control register	IRCR	8	8	2, 3 PCLKB	2 ICLK
0008 8600h	MTU3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8601h	MTU4	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8602h	MTU3	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8603h	MTU4	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8604h	MTU3	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (18 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C152h	MPC	P22 pin function control register	P22PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C153h	MPC	P23 pin function control register	P23PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C154h	MPC	P24 pin function control register	P24PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C155h	MPC	P25 pin function control register	P25PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C156h	MPC	P26 pin function control register	P26PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C157h	MPC	P27 pin function control register	P27PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C158h	MPC	P30 pin function control register	P30PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C159h	MPC	P31 pin function control register	P31PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Ah	MPC	P32 pin function control register	P32PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Bh	MPC	P33 pin function control register	P33PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Ch	MPC	P34 pin function control register	P34PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C160h	MPC	P40 pin function control register	P40PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C161h	MPC	P41 pin function control register	P41PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C162h	MPC	P42 pin function control register	P42PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C163h	MPC	P43 pin function control register	P43PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C164h	MPC	P44 pin function control register	P44PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C165h	MPC	P45 pin function control register	P45PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C166h	MPC	P46 pin function control register	P46PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C167h	MPC	P47 pin function control register	P47PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C16Ch	MPC	P54 pin function control register	P54PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C16Dh	MPC	P55 pin function control register	P55PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C190h	MPC	PA0 pin function control register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C191h	MPC	PA1 pin function control register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C192h	MPC	PA2 pin function control register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C193h	MPC	PA3 pin function control register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C194h	MPC	PA4 pin function control register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C195h	MPC	PA5 pin function control register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C196h	MPC	PA6 pin function control register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C197h	MPC	PA7 pin function control register	PA7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C198h	MPC	PB0 pin function control register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C199h	MPC	PB1 pin function control register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Ah	MPC	PB2 pin function control register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Bh	MPC	PB3 pin function control register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Ch	MPC	PB4 pin function control register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Dh	MPC	PB5 pin function control register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Eh	MPC	PB6 pin function control register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Fh	MPC	PB7 pin function control register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A0h	MPC	PC0 pin function control register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A1h	MPC	PC1 pin function control register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A2h	MPC	PC2 pin function control register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A3h	MPC	PC3 pin function control register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A4h	MPC	PC4 pin function control register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A5h	MPC	PC5 pin function control register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A6h	MPC	PC6 pin function control register	PC6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A7h	MPC	PC7 pin function control register	PC7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A8h	MPC	PD0 pin function control register	PD0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A9h	MPC	PD1 pin function control register	PD1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1AAh	MPC	PD2 pin function control register	PD2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1ABh	MPC	PD3 pin function control register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1ACh	MPC	PD4 pin function control register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1ADh	MPC	PD5 pin function control register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (20 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C42Eh	RTC	Time error adjustment register	RADJ	8	8	2, 3 PCLKB	2 ICLK
007F C402h	FLASH	Flash mode register	FMODR	8	8	2, 3 FCLK	2 ICLK
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2, 3 FCLK	2 ICLK
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2, 3 FCLK	2 ICLK
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2, 3 FCLK	2 ICLK
007F C440h	FLASH	E2 DataFlash read enable register 0	DFLRE0	16	16	2, 3 FCLK	2 ICLK
007F C450h	FLASH	E2 DataFlash programming/erasure enable register 0	DFLWE0	16	16	2, 3 FCLK	2 ICLK
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2, 3 FCLK	2 ICLK
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2, 3 FCLK	2 ICLK
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2, 3 FCLK	2 ICLK
007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2, 3 FCLK	2 ICLK
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2, 3 FCLK	2 ICLK
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2, 3 FCLK	2 ICLK
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2, 3 FCLK	2 ICLK
007F FFCAh	FLASH	E2 DataFlash blank check control register	DFLBCCNT	16	16	2, 3 FCLK	2 ICLK
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2, 3 FCLK	2 ICLK
007F FFCEh	FLASH	E2 DataFlash blank check status register	DFLBCSTAT	16	16	2, 3 FCLK	2 ICLK
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2, 3 FCLK	2 ICLK

Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register.
Note 2. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMOCNTL register.

Table 5.6 DC Characteristics (5)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.*9	Max.	Unit	Test Conditions
Supply current*1	Medium-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz	I_{CC}	4.6	—	mA	
				ICLK = 20 MHz		3.2	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		14	—		
				ICLK = 20 MHz		9.5	—		
			All peripheral operation: Max.*3	ICLK = 32 MHz		—	25		
				ICLK = 20 MHz		—	19		
		Sleep mode	No peripheral operation*2	ICLK = 32 MHz		3.8	—		
				ICLK = 20 MHz		3.0	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		10	—		
				ICLK = 20 MHz		7	—		
		All-module clock stop mode		ICLK = 32 MHz		2.5	—		
				ICLK = 20 MHz		2.0	—		
		Increase during BGO operation*4	Medium-speed operating mode 1A			17	—		
			Medium-speed operating mode 1B			17	—		
	Low-speed operating mode 1	Normal operating mode	No peripheral operation*5	ICLK = 8 MHz		1.4	—		
				ICLK = 4 MHz		0.9	—		
				ICLK = 2 MHz		0.7	—		
			All peripheral operation: Normal*6	ICLK = 8 MHz		4.2	—		
				ICLK = 4 MHz		2.6	—		
				ICLK = 2 MHz		1.8	—		
			All peripheral operation: Max.*6	ICLK = 8 MHz		—	6.5		
				ICLK = 4 MHz		—	3.7		
				ICLK = 2 MHz		—	2.4		
		Sleep mode	No peripheral operation*5	ICLK = 8 MHz		1.5	—		
				ICLK = 4 MHz		1.2	—		
				ICLK = 2 MHz		1.1	—		
			All peripheral operation: Normal*6	ICLK = 8 MHz		3.1	—		
				ICLK = 4 MHz		2.1	—		
				ICLK = 2 MHz		1.5	—		
		All-module clock stop mode		ICLK = 8 MHz		1.4	—		
				ICLK = 4 MHz		1.1	—		
				ICLK = 2 MHz		1.0	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*7	ICLK = 32 kHz		0.027	—		
			All peripheral operation: Normal*8	ICLK = 32 kHz		0.04	—		
			All peripheral operation: Max.*8	ICLK = 32 kHz		—	0.23		
		Sleep mode	No peripheral operation*7	ICLK = 32 kHz		0.024	—		
			All peripheral operation: Normal*8	ICLK = 32 kHz		0.034	—		
		All-module clock stop mode				0.016	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO. BCLK, FCLK, and PCLK are ICLK divided by 1.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.

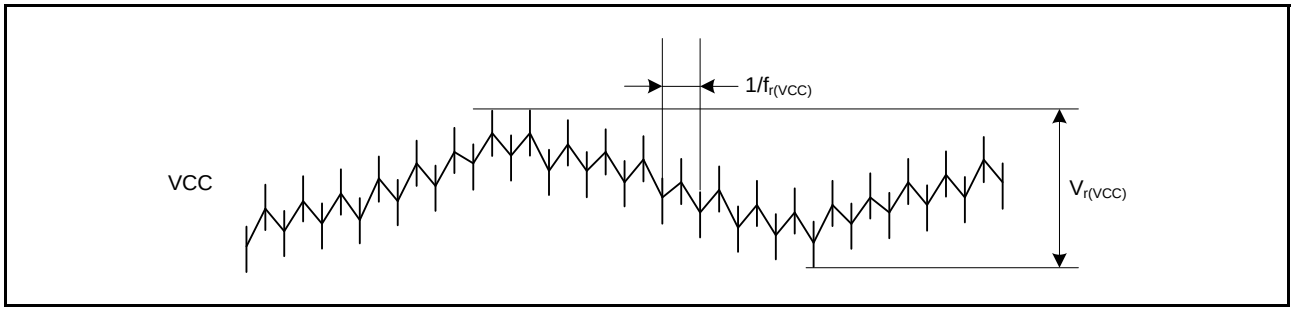


Figure 5.6 Ripple Waveform

Table 5.13 Permissible Output Currents (1)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, when total power (mW) < 1000 – 10 × T_a

Item			Symbol	Max.	Unit
Permissible output low current (average value per 1 pin)		Normal output mode	I_{OL}	4.0	mA
		High-drive output mode		16.0	
Permissible output low current (maximum value per 1 pin)		Normal output mode		4.0	mA
		High-drive output mode		16.0	
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	80	mA
Permissible output high current (average value per 1 pin)		Normal output mode	I_{OH}	–4.0	mA
		High-drive output mode		–8.0	
Permissible output high current (maximum value per 1 pin)		Normal output mode		–4.0	mA
		High-drive output mode		–8.0	
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	–60	mA

Table 5.14 Permissible Output Currents (2)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, when total power (mW) ≥ 1000 – 10 × T_a

Item			Symbol	Max.	Unit
Permissible output low current (average value per 1 pin)		Normal output mode	I_{OL}	2.0	mA
		High-drive output mode		8.0	
Permissible output low current (maximum value per 1 pin)		Normal output mode		2.0	mA
		High-drive output mode		8.0	
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	40	mA
Permissible output high current (average value per 1 pin)		Normal output mode	I_{OH}	–2.0	mA
		High-drive output mode		–4.0	
Permissible output high current (maximum value per 1 pin)		Normal output mode		–2.0	mA
		High-drive output mode		–4.0	
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	–30	mA

Table 5.15 Output Values of Voltage (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, when total power (mW) < 1000 – 10 × T_a

Item			Symbol	Min.	Max.	Unit	Test Conditions	
							VCC = 2.7 to 4.0 V	VCC = 4.0 to 5.5 V
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	1.0	V	I_{OL} = 3.0 mA	I_{OL} = 4.0 mA
		High-drive output mode		—	1.0		I_{OL} = 8.0 mA	I_{OL} = 16.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA	
				—	0.6		I_{OL} = 6.0 mA	
Output high	All output pins	Normal output mode	V_{OH}	VCC – 1.0	—	V	I_{OH} = – 3.0 mA	I_{OH} = – 4.0 mA
		High-drive output mode		VCC – 1.0	—		I_{OH} = – 5.0 mA	I_{OH} = – 8.0 mA

Table 5.16 Output Values of Voltage (2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, when total power (mW) ≥ 1000 – 10 × T_a

Item			Symbol	Min.	Max.	Unit	Test Conditions	
							VCC = 2.7 to 4.0 V	VCC = 4.0 to 5.5 V
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	1.0	V	I_{OL} = 2.0 mA	I_{OL} = 2.0 mA
		High-drive output mode		—	1.0		I_{OL} = 8.0 mA	I_{OL} = 8.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA	
				—	0.6		I_{OL} = 6.0 mA	
Output high	All output pins	Normal output mode	V_{OH}	VCC – 1.0	—	V	I_{OH} = – 2.0 mA	I_{OH} = – 2.0 mA
		High-drive output mode		VCC – 1.0	—		I_{OH} = – 4.0 mA	I_{OH} = – 4.0 mA

Table 5.17 Output Values of Voltage (3)

Conditions: VCC = AVCC0 = 1.62 to 2.7 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	0.4	V	I_{OL} = 0.5 mA
		High-drive output mode		—	0.4		I_{OL} = 2.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 0.4	—	V	I_{OH} = –0.5 mA
		High-drive output mode		VCC – 0.4	—		I_{OH} = –1.0 mA

5.3.2 Reset Timing

Table 5.23 Reset Timing

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	8	—	—	ms	Figure 5.28
	Software standby mode, low-speed operating modes 1 and 2	t_{RESWS}	1	—	—	ms	Figure 5.29
	Programming or erasure of the ROM or E2 DataFlash memory or blank checking of the E2 DataFlash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Wait time after RES# cancellation		t_{RESWT}	—	—	912	µs	Figure 5.28
Internal reset time (independent watchdog timer reset, software reset)		t_{RESW2}	—	—	1.4	ms	

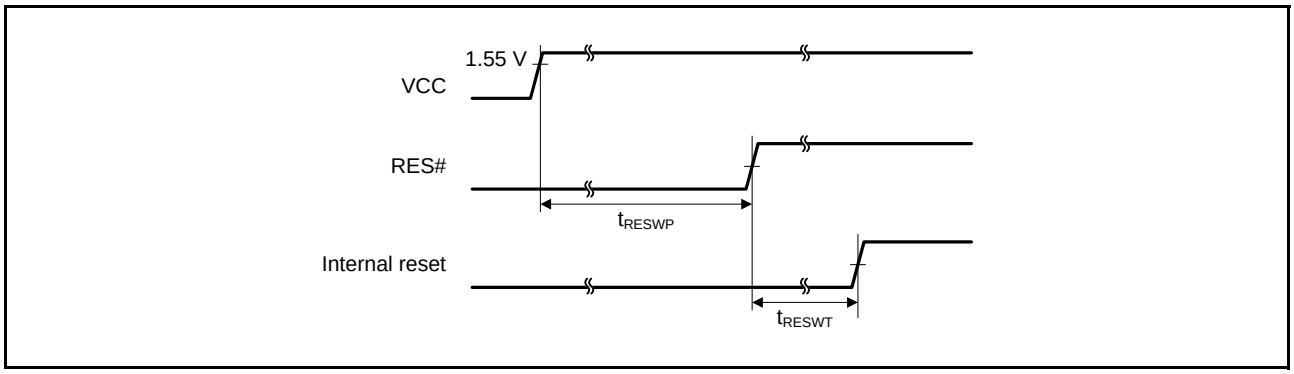


Figure 5.28 Reset Input Timing at Power-On

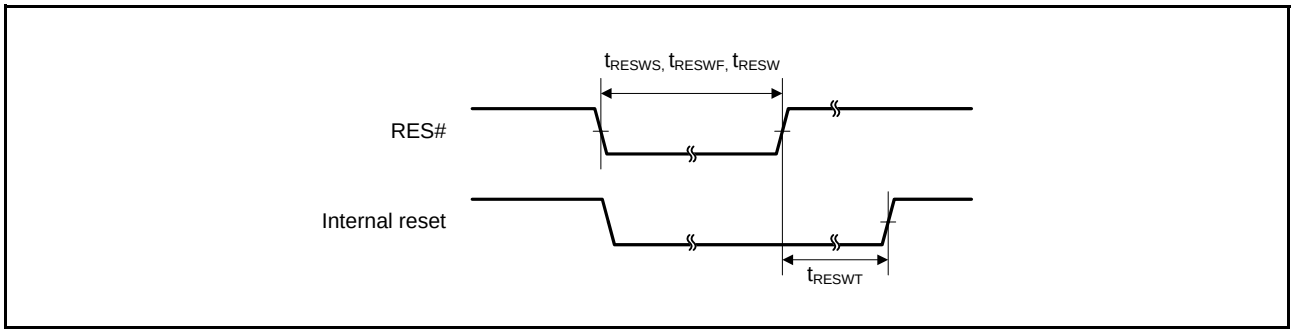


Figure 5.29 Reset Input Timing

Table 5.27 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle*2	Master		t_{SPcyc}	2	4096	t_{Pcyc}	C = 30 pF Figure 5.41
		Slave			8	4096		
	RSPCK clock high pulse width*2	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width*2	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time*2	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.62 V ≤ VCC < 2.7 V		—	20		
		Input			—	1	µs	
	Data input setup time	Master		t_{SU}	4	—	ns	C = 30 pF Figure 5.42 to Figure 5.47
		Slave			$20 - t_{Pcyc}$	—		
	Data input hold time	Master	PCLKB set to a division ratio other than divided by 2	t_H	t_{Pcyc}	—	ns	
			PCLKB set to divided by 2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OD}	—	14	ns	
			1.62 V ≤ VCC < 2.7 V		—	28		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		—	$3 \times t_{Pcyc} + 40$		
			1.62 V ≤ VCC < 2.7 V		—	$3 \times t_{Pcyc} + 80$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	10	ns	
			1.62 V ≤ VCC < 2.7 V		—	20		
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	20	ns	
		Input			—	1	µs	
	Slave access time			t_{SA}	—	4	t_{Pcyc}	C = 30 pF Figure 5.45 and Figure 5.47
	Slave output release time			t_{REL}	—	3	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLKB cycle
Note 2. Value when the drive capacity of clock output ports is set to normal output.

Table 5.29 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, fPCLKB = up to 32 MHz, T_a = –40 to +105°C

Item		Symbol	Min.*1,*2	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 5.48
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (5) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 5.48
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: • t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle
Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. C_b indicates the total capacity of the bus line.

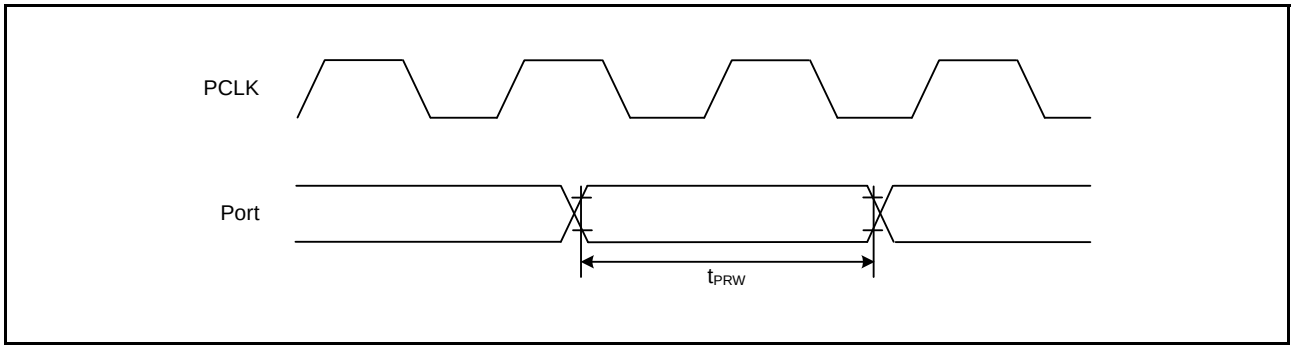


Figure 5.33 I/O Port Input Timing

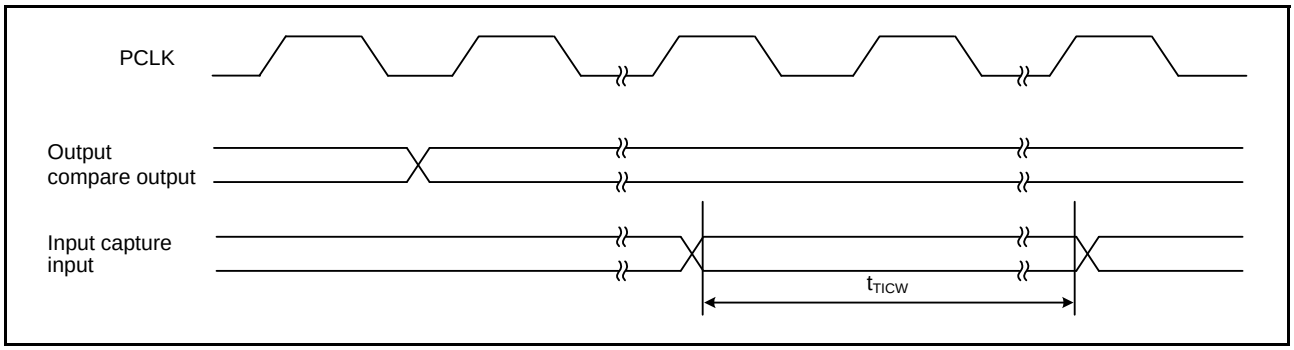


Figure 5.34 MTU Input/Output Timing

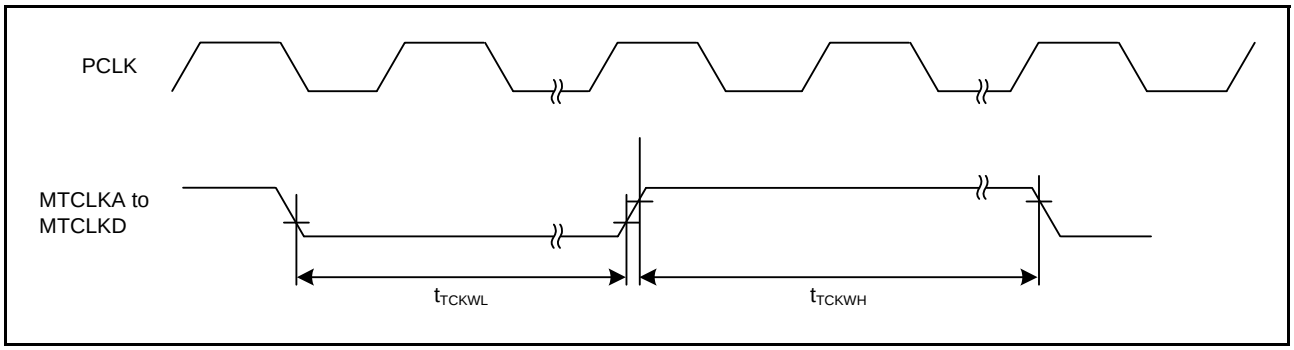


Figure 5.35 MTU Clock Input Timing

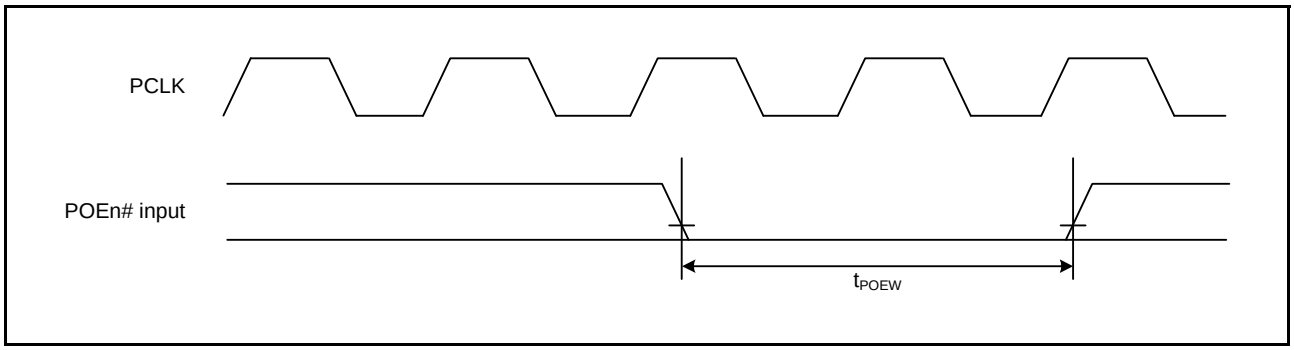


Figure 5.36 POE# Input Timing

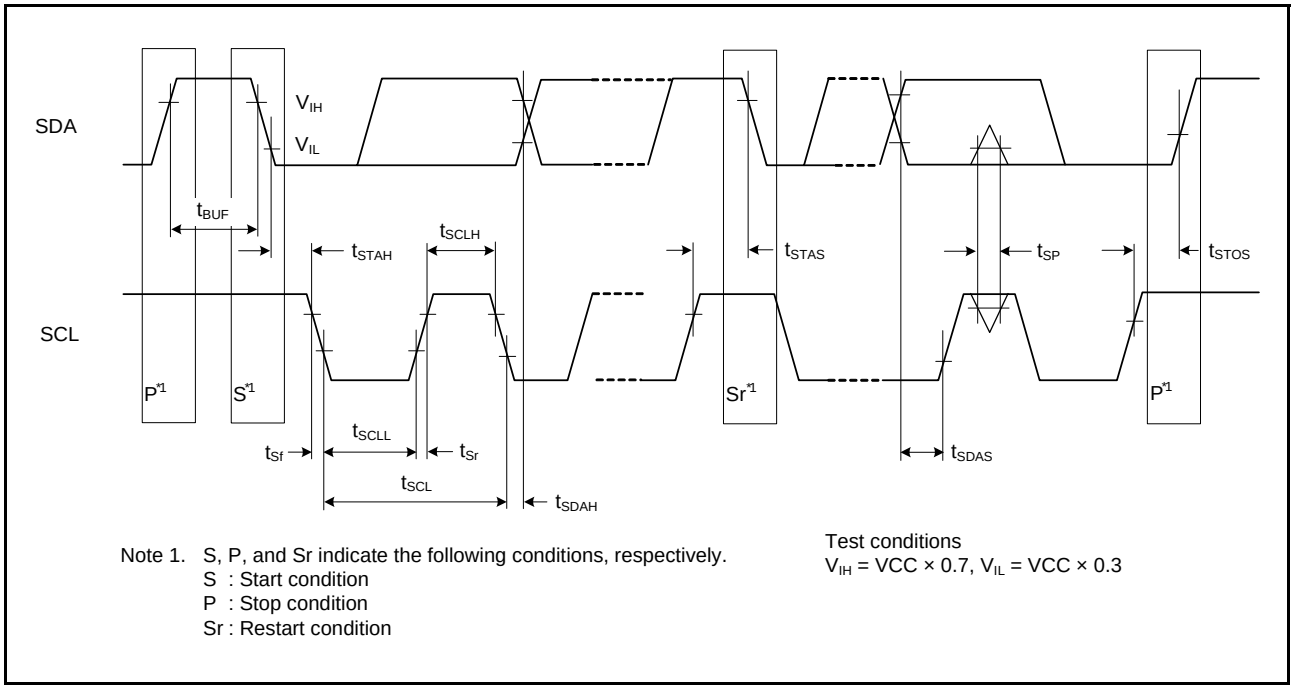


Figure 5.48 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

Table 5.34 A/D Conversion Characteristics (2)

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, 1.62 ≤ VREFH0 ≤ 2.7 V, AVCC0 – 0.9 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
A/D conversion clock frequency (fPCLKD)		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at fPCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 1 kΩ	5.25 (1.5)*2	—	—	µs	Sampling in 12 states
	Permissible signal source impedance (Max.) = 5 kΩ	6.25 (2.5)*2	—	—		Sampling in 20 states
Analog input capacitance		—	—	30	pF	
Offset error		—	±0.5	±7.5	LSB	
Full-scale error		—	±1.25	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±1.25	—	LSB	
INL integral nonlinearity error		—	±1.5	±5.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.35 Sampling Time

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Typ.	Unit	Test Conditions
Sampling time	High-precision channel	Ts	0.208 + 0.417 × R0 (kΩ)	µs	Figure 5.49
	Normal-precision channel				

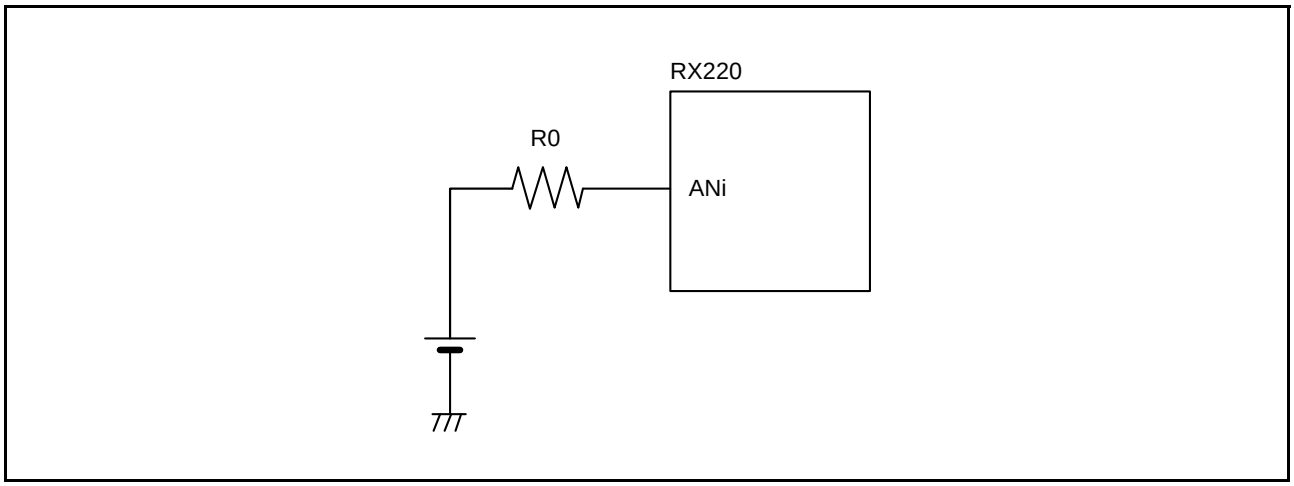


Figure 5.49 Internal Equivalent Circuit of Analog Input Pin