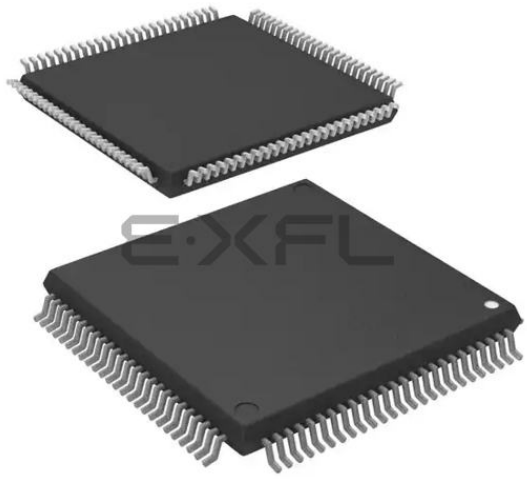

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52206bdfp-30

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products

Group	Part No.	Package	ROM Capacity	RAM Capacity	Operating Frequency (Max.)	Operating temperature
RX220	R5F52206BDFP	PLQP0100KB-A	256 Kbytes	16 Kbytes	32 MHz	–40 to +85°C
	R5F52206BDFM	PLQP0064KB-A				
	R5F52206BDFK	PLQP0064GA-A				
	R5F52206BDFL	PLQP0048KB-A				
	R5F52205BDFP	PLQP0100KB-A	128 Kbytes	8 Kbytes		
	R5F52205BDFM	PLQP0064KB-A				
	R5F52205BDFK	PLQP0064GA-A				
	R5F52205BDFL	PLQP0048KB-A				
	R5F52203BDFP	PLQP0100KB-A	64 Kbytes			
	R5F52203BDFM	PLQP0064KB-A				
	R5F52203BDFK	PLQP0064GA-A				
	R5F52203BDFL	PLQP0048KB-A				
	R5F52201BDFM	PLQP0064KB-A	32 Kbytes	4Kbytes		
	R5F52201BDFK	PLQP0064GA-A				
	R5F52201BDFL	PLQP0048KB-A				
	R5F52206BGFP	PLQP0100KB-A	256 Kbytes	16 Kbytes	32 MHz	–40 to +105°C
	R5F52206BGFM	PLQP0064KB-A				
	R5F52206BGFK	PLQP0064GA-A				
	R5F52206BGFL	PLQP0048KB-A				
	R5F52205BGFP	PLQP0100KB-A	128 Kbytes	8 Kbytes		
	R5F52205BGFM	PLQP0064KB-A				
	R5F52205BGFK	PLQP0064GA-A				
	R5F52205BGFL	PLQP0048KB-A				
	R5F52203BGFP	PLQP0100KB-A	64 Kbytes			
	R5F52203BGFM	PLQP0064KB-A				
	R5F52203BGFK	PLQP0064GA-A				
	R5F52203BGFL	PLQP0048KB-A				
	R5F52201BGFM	PLQP0064KB-A	32 Kbytes	4Kbytes		
	R5F52201BGFK	PLQP0064GA-A				
	R5F52201BGFL	PLQP0048KB-A				

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (2 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIe, SCIf, RSPI, RIIC)	Others
48		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/SSLA0	
49		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/IRTXD5	
50		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/IRRXD5/ SSLA3	
51		PC1	MTIOC3A	SCK5/SSLA2	
52		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1	
53		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	
54		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	
55		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	
56		PB4		CTS9#/RTS9#/SS9#	
57		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	
58		PB2		CTS6#/RTS6#/SS6#	
59		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4
60	VCC				
61		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	
62	VSS				
63		PA7		MISOA	
64		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	
65		PA5		RSPCKA	
66		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/IRTXD5/ SSLA0	IRQ5
67		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5/IRRXD5	IRQ6
68		PA2		RXD5/SMISO5/SSCL5/SSLA3/ IRRXD5	
69		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
70		PA0	MTIOC4A	SSLA1	CACREF
71		PE7			IRQ7/AN015
72		PE6			IRQ6/AN014
73		PE5	MTIOC4C/MTIOC2B		IRQ5/AN013
74		PE4	MTIOC4D/MTIOC1A		AN012/CMPA2
75		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
76		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12	IRQ7/AN010
77		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009
78		PE0		SCK12	AN008
79		PD7	MTIC5U/POE0#		IRQ7
80		PD6	MTIC5V/POE1#		IRQ6
81		PD5	MTIC5W/POE2#		IRQ5
82		PD4	POE3#		IRQ4
83		PD3	POE8#		IRQ3
84		PD2	MTIOC4D		IRQ2
85		PD1	MTIOC4B		IRQ1
86		PD0			IRQ0
87		P47			AN007
88		P46			AN006
89		P45			AN005
90		P44			AN004

4. I/O Registers

This section provides information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to registers are also given below.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

Table 4.1 List of I/O Registers (Address Order) (5 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK	
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK	
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK	
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK	
0008 7167h	ICU	DTC activation enable register 103	DTCER103	8	8	2 ICLK	
0008 716Ah	ICU	DTC activation enable register 106	DTCER106	8	8	2 ICLK	
0008 7172h	ICU	DTC activation enable register 114	DTCER114	8	8	2 ICLK	
0008 7173h	ICU	DTC activation enable register 115	DTCER115	8	8	2 ICLK	
0008 7174h	ICU	DTC activation enable register 116	DTCER116	8	8	2 ICLK	
0008 7175h	ICU	DTC activation enable register 117	DTCER117	8	8	2 ICLK	
0008 7179h	ICU	DTC activation enable register 121	DTCER121	8	8	2 ICLK	
0008 717Ah	ICU	DTC activation enable register 122	DTCER122	8	8	2 ICLK	
0008 717Dh	ICU	DTC activation enable register 125	DTCER125	8	8	2 ICLK	
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8	2 ICLK	
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8	2 ICLK	
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8	2 ICLK	
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8	2 ICLK	
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8	2 ICLK	
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8	2 ICLK	
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8	2 ICLK	
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8	2 ICLK	
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8	2 ICLK	
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8	2 ICLK	
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8	2 ICLK	
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8	2 ICLK	
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8	2 ICLK	
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8	2 ICLK	
0008 71AFh	ICU	DTC activation enable register 175	DTCER175	8	8	2 ICLK	
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8	2 ICLK	
0008 71B2h	ICU	DTC activation enable register 178	DTCER178	8	8	2 ICLK	
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8	2 ICLK	
0008 71B5h	ICU	DTC activation enable register 181	DTCER181	8	8	2 ICLK	
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8	2 ICLK	
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8	2 ICLK	
0008 71C6h	ICU	DTC activation enable register 198	DTCER198	8	8	2 ICLK	
0008 71C7h	ICU	DTC activation enable register 199	DTCER199	8	8	2 ICLK	
0008 71C8h	ICU	DTC activation enable register 200	DTCER200	8	8	2 ICLK	
0008 71C9h	ICU	DTC activation enable register 201	DTCER201	8	8	2 ICLK	
0008 71DBh	ICU	DTC activation enable register 219	DTCER219	8	8	2 ICLK	
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8	2 ICLK	
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8	2 ICLK	
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8	2 ICLK	
0008 71E3h	ICU	DTC activation enable register 227	DTCER227	8	8	2 ICLK	
0008 71E4h	ICU	DTC activation enable register 228	DTCER228	8	8	2 ICLK	
0008 71EBh	ICU	DTC activation enable register 235	DTCER235	8	8	2 ICLK	
0008 71ECh	ICU	DTC activation enable register 236	DTCER236	8	8	2 ICLK	
0008 71EFh	ICU	DTC activation enable register 239	DTCER239	8	8	2 ICLK	
0008 71F0h	ICU	DTC activation enable register 240	DTCER240	8	8	2 ICLK	
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8	2 ICLK	
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8	2 ICLK	
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (6 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8		2 ICLK
0008 7204h	ICU	Interrupt request enable register 04	IER04	8	8		2 ICLK
0008 7205h	ICU	Interrupt request enable register 05	IER05	8	8		2 ICLK
0008 7207h	ICU	Interrupt request enable register 07	IER07	8	8		2 ICLK
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8		2 ICLK
0008 720Bh	ICU	Interrupt request enable register 0B	IER0B	8	8		2 ICLK
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8		2 ICLK
0008 720Dh	ICU	Interrupt request enable register 0D	IER0D	8	8		2 ICLK
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8		2 ICLK
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8		2 ICLK
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8		2 ICLK
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8		2 ICLK
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8		2 ICLK
0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8		2 ICLK
0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8		2 ICLK
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8		2 ICLK
0008 7219h	ICU	Interrupt request enable register 19	IER19	8	8		2 ICLK
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8		2 ICLK
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8		2 ICLK
0008 721Dh	ICU	Interrupt request enable register 1D	IER1D	8	8		2 ICLK
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8		2 ICLK
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8		2 ICLK
0008 72E0h	ICU	Software interrupt activation register	SWINTR	8	8		2 ICLK
0008 72F0h	ICU	Fast interrupt set register	FIR	16	16		2 ICLK
0008 7300h	ICU	Interrupt source priority register 000	IPR000	8	8		2 ICLK
0008 7301h	ICU	Interrupt source priority register 001	IPR001	8	8		2 ICLK
0008 7302h	ICU	Interrupt source priority register 002	IPR002	8	8		2 ICLK
0008 7303h	ICU	Interrupt source priority register 003	IPR003	8	8		2 ICLK
0008 7304h	ICU	Interrupt source priority register 004	IPR004	8	8		2 ICLK
0008 7305h	ICU	Interrupt source priority register 005	IPR005	8	8		2 ICLK
0008 7306h	ICU	Interrupt source priority register 006	IPR006	8	8		2 ICLK
0008 7307h	ICU	Interrupt source priority register 007	IPR007	8	8		2 ICLK
0008 7320h	ICU	Interrupt source priority register 032	IPR032	8	8		2 ICLK
0008 7321h	ICU	Interrupt source priority register 033	IPR033	8	8		2 ICLK
0008 7322h	ICU	Interrupt source priority register 034	IPR034	8	8		2 ICLK
0008 732Ch	ICU	Interrupt source priority register 044	IPR044	8	8		2 ICLK
0008 7339h	ICU	Interrupt source priority register 057	IPR057	8	8		2 ICLK
0008 733Fh	ICU	Interrupt source priority register 063	IPR063	8	8		2 ICLK
0008 7340h	ICU	Interrupt source priority register 064	IPR064	8	8		2 ICLK
0008 7341h	ICU	Interrupt source priority register 065	IPR065	8	8		2 ICLK
0008 7342h	ICU	Interrupt source priority register 066	IPR066	8	8		2 ICLK
0008 7343h	ICU	Interrupt source priority register 067	IPR067	8	8		2 ICLK
0008 7344h	ICU	Interrupt source priority register 068	IPR068	8	8		2 ICLK
0008 7345h	ICU	Interrupt source priority register 069	IPR069	8	8		2 ICLK
0008 7346h	ICU	Interrupt source priority register 070	IPR070	8	8		2 ICLK
0008 7347h	ICU	Interrupt source priority register 071	IPR071	8	8		2 ICLK
0008 7358h	ICU	Interrupt source priority register 088	IPR088	8	8		2 ICLK
0008 7359h	ICU	Interrupt source priority register 089	IPR089	8	8		2 ICLK
0008 735Ch	ICU	Interrupt source priority register 092	IPR092	8	8		2 ICLK
0008 735Dh	ICU	Interrupt source priority register 093	IPR093	8	8		2 ICLK
0008 7366h	ICU	Interrupt source priority register 102	IPR102	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (9 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK
0008 8300h	RIIC0	I2C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK
0008 8301h	RIIC0	I2C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8302h	RIIC0	I2C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK
0008 8303h	RIIC0	I2C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK
0008 8304h	RIIC0	I2C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK
0008 8305h	RIIC0	I2C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK
0008 8306h	RIIC0	I2C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK
0008 8307h	RIIC0	I2C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK
0008 8308h	RIIC0	I2C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK
0008 8309h	RIIC0	I2C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK
0008 830Ah	RIIC0	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK
0008 830Ah	RIIC0	Timeout internal counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK
0008 830Bh	RIIC0	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK
0008 830Bh	RIIC0	Timeout internal counter U	TMOCNTU	8	8*2	2, 3 PCLKB	2 ICLK
0008 830Ch	RIIC0	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK
0008 8310h	RIIC0	I2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK
0008 8311h	RIIC0	I2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK
0008 8312h	RIIC0	I2C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK
0008 8313h	RIIC0	I2C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK
0008 8380h	RSPI0	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK
0008 8381h	RSPI0	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK
0008 8382h	RSPI0	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK
0008 8383h	RSPI0	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK
0008 8384h	RSPI0	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK
0008 8388h	RSPI0	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK
0008 8389h	RSPI0	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK
0008 838Ah	RSPI0	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK
0008 838Bh	RSPI0	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK
0008 838Ch	RSPI0	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK
0008 838Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK
0008 838Eh	RSPI0	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK
0008 838Fh	RSPI0	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8390h	RSPI0	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK
0008 8392h	RSPI0	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK
0008 8394h	RSPI0	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK
0008 8396h	RSPI0	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK
0008 8398h	RSPI0	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK
0008 839Ah	RSPI0	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK
0008 839Ch	RSPI0	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK
0008 839Eh	RSPI0	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK
0008 8410h	IRDA	IrDA control register	IRCR	8	8	2, 3 PCLKB	2 ICLK
0008 8600h	MTU3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8601h	MTU4	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8602h	MTU3	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8603h	MTU4	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8604h	MTU3	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (18 / 20)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C152h	MPC	P22 pin function control register	P22PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C153h	MPC	P23 pin function control register	P23PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C154h	MPC	P24 pin function control register	P24PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C155h	MPC	P25 pin function control register	P25PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C156h	MPC	P26 pin function control register	P26PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C157h	MPC	P27 pin function control register	P27PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C158h	MPC	P30 pin function control register	P30PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C159h	MPC	P31 pin function control register	P31PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Ah	MPC	P32 pin function control register	P32PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Bh	MPC	P33 pin function control register	P33PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Ch	MPC	P34 pin function control register	P34PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C160h	MPC	P40 pin function control register	P40PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C161h	MPC	P41 pin function control register	P41PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C162h	MPC	P42 pin function control register	P42PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C163h	MPC	P43 pin function control register	P43PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C164h	MPC	P44 pin function control register	P44PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C165h	MPC	P45 pin function control register	P45PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C166h	MPC	P46 pin function control register	P46PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C167h	MPC	P47 pin function control register	P47PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C16Ch	MPC	P54 pin function control register	P54PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C16Dh	MPC	P55 pin function control register	P55PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C190h	MPC	PA0 pin function control register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C191h	MPC	PA1 pin function control register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C192h	MPC	PA2 pin function control register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C193h	MPC	PA3 pin function control register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C194h	MPC	PA4 pin function control register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C195h	MPC	PA5 pin function control register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C196h	MPC	PA6 pin function control register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C197h	MPC	PA7 pin function control register	PA7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C198h	MPC	PB0 pin function control register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C199h	MPC	PB1 pin function control register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Ah	MPC	PB2 pin function control register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Bh	MPC	PB3 pin function control register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Ch	MPC	PB4 pin function control register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Dh	MPC	PB5 pin function control register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Eh	MPC	PB6 pin function control register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Fh	MPC	PB7 pin function control register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A0h	MPC	PC0 pin function control register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A1h	MPC	PC1 pin function control register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A2h	MPC	PC2 pin function control register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A3h	MPC	PC3 pin function control register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A4h	MPC	PC4 pin function control register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A5h	MPC	PC5 pin function control register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A6h	MPC	PC6 pin function control register	PC6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A7h	MPC	PC7 pin function control register	PC7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A8h	MPC	PD0 pin function control register	PD0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A9h	MPC	PD1 pin function control register	PD1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1AAh	MPC	PD2 pin function control register	PD2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1ABh	MPC	PD3 pin function control register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1ACh	MPC	PD4 pin function control register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1ADh	MPC	PD5 pin function control register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = 0 V

Item	Symbol	Value	Unit
Power supply voltage	VCC	–0.3 to +6.5	V
Input voltage (except for ports for 5V tolerant*1 and port 4)	V_{in}	–0.3 to VCC +0.3*3	V
Input voltage (port 4)	V_{in}	–0.3 to AVCC0 +0.3*3	V
Input voltage (ports for 5 V tolerant*1)	V_{in}	–0.3 to +6.5	V
Analog power supply voltage	AVCC0*2	–0.3 to +6.5	V
Reference power supply voltage	VREFH0*2	–0.3 to AVCC0 +0.3*3	V
Analog input voltage (except for port 4)	V_{AN}	–0.3 to VCC +0.3*3	V
Analog input voltage (port 4)	V_{AN}	–0.3 to AVCC0 +0.3*3	V
Operating temperature	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interferences, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, and between the VREFH0 and VREFL0 pins. Place capacitors of 0.1 µF or so as close to every power pin and use the shortest and heaviest possible traces.

Connect the VCL pin to a VSS pin via a 0.1 µF (±20% accuracy) capacitor. The capacitor must be placed as close to the pin as possible.

Note 1. Ports 12, 13, 16, and 17 are 5 V tolerant.

Note 2. Set to the same potential as VCC. When the A/D converter is not used, do not leave the AVCC0, VREFH0, AVSS0, and VREFL0 pins open. Connect the AVCC0 and VREFH0 pins to VCC, and the AVSS0 and VREFL0 pins to VSS, respectively.

Note 3. The maximum value is 6.5 V.

Table 5.4 DC Characteristics (3)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD pin, P35/NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Other pins except for ports for 5 V tolerant	$\lvert I_{TSI} \rvert$	—	—	0.2	µA	V_{in} = 0 V, VCC
	Ports for 5 V tolerant		—	—	1.0		V_{in} = 0 V, 5.8 V
Input capacitance	All input pins (except for XCIN and XCOUT)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	XCIN and XCOUT		—	—	3		

Table 5.5 DC Characteristics (4)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC						Unit	Test Conditions
			1.62 to 2.7 V		2.7 to 4.0 V		4.0 to 5.5 V			
			Min.	Max.	Min.	Max.	Min.	Max.		
Input pull-up MOS current	All ports (except for port 35)	I_p	–150	–5	–200	–10	–400	–50	µA	V_{in} = 0 V

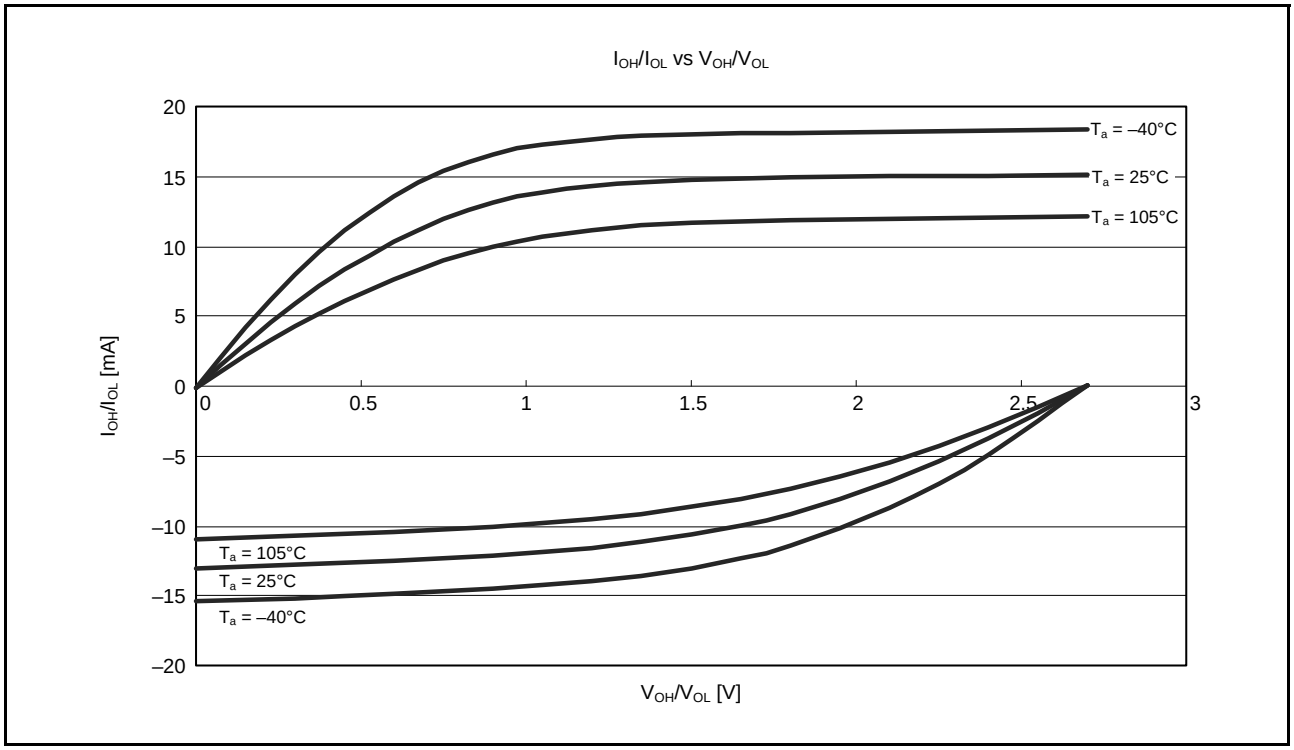

Figure 5.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V when Normal Output is Selected (Reference Data)

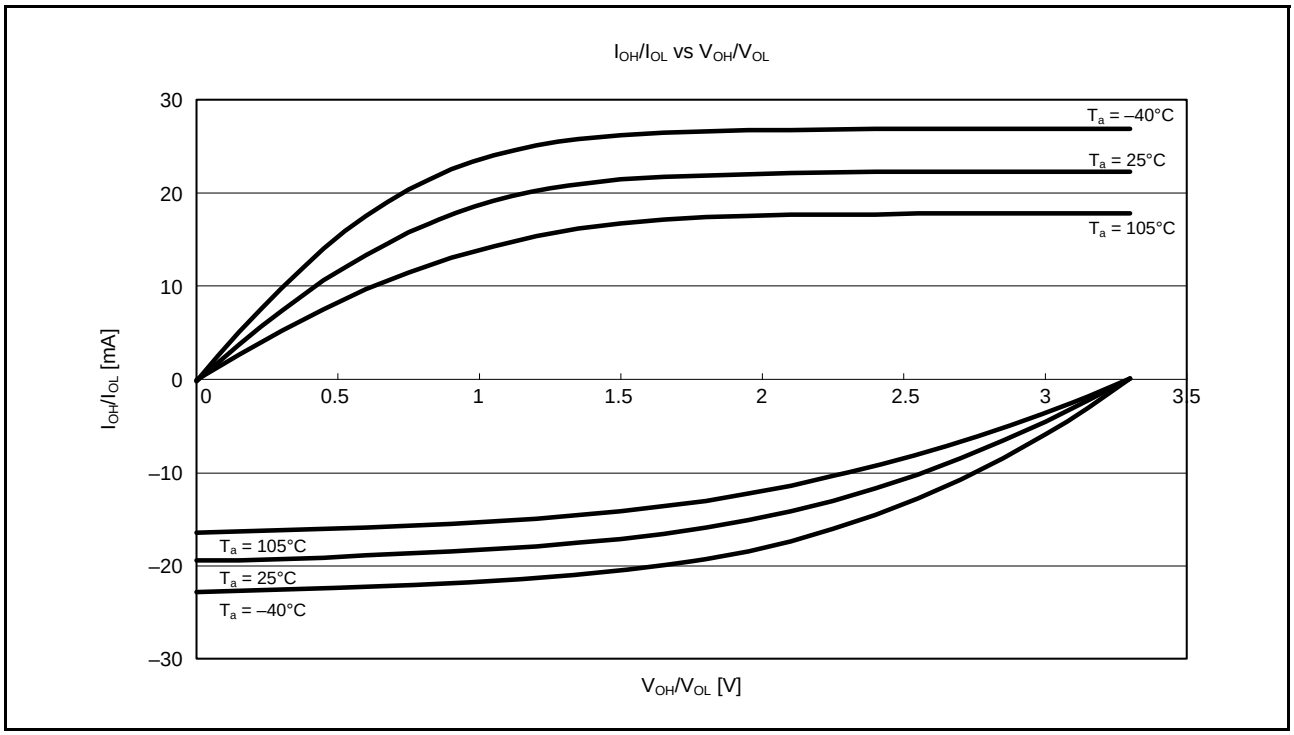

Figure 5.10 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 3.3 V when Normal Output is Selected (Reference Data)

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.24 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode (HOCO power supplied) (SOFTCUT[2:0] bits = 000b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.30
	External clock input to main clock oscillator*4	Main clock oscillator operating	t_{SBYEX}	7	—	—	µs	
	Sub-clock oscillator operating*5		t_{SBYSC}	2*3	—	—	s	
	HOCO clock oscillator operating*6		t_{SBYHO}	—	—	50	µs	
	LOCO clock oscillator operating*5		t_{SBYLO}	—	—	90	µs	
Recovery time after cancellation of software standby mode (HOCO power not supplied) (SOFTCUT[2:0] bits = 11xb)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.30
	External clock input to main clock oscillator*4	Main clock oscillator operating	t_{SBYEX}	40	—	—	µs	
	Sub-clock oscillator operating*5		t_{SBYSC}	2*3	—	—	s	
	HOCO clock oscillator operating*6		t_{SBYHO}	—	—	0.8	ms	
	LOCO clock oscillator operating*5		t_{SBYLO}	—	—	90	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source, and depends on the time set in the wait control registers corresponding to the oscillators.
Note 2. The indicated value is measured for an 8 MHz crystal resonator. ICLK is set to divided by 1.
Note 3. When RCR3.RTCEN = 1, the time will be the time set in the SOSCWTCR register minus 2 s.
Note 4. When the external clock frequency is 20 MHz. ICLK is set to divided by 1.
Note 5. ICLK is set to divided by 1.
Note 6. When the frequency is 50 MHz, HOCOWTCR2.HSTS2[4:0] = 10101b and ICLK is set to divided by 2.
When the frequency is 32 MHz, HOCOWTCR2.HSTS2[4:0] = 10100b and ICLK is set to divided by 1.

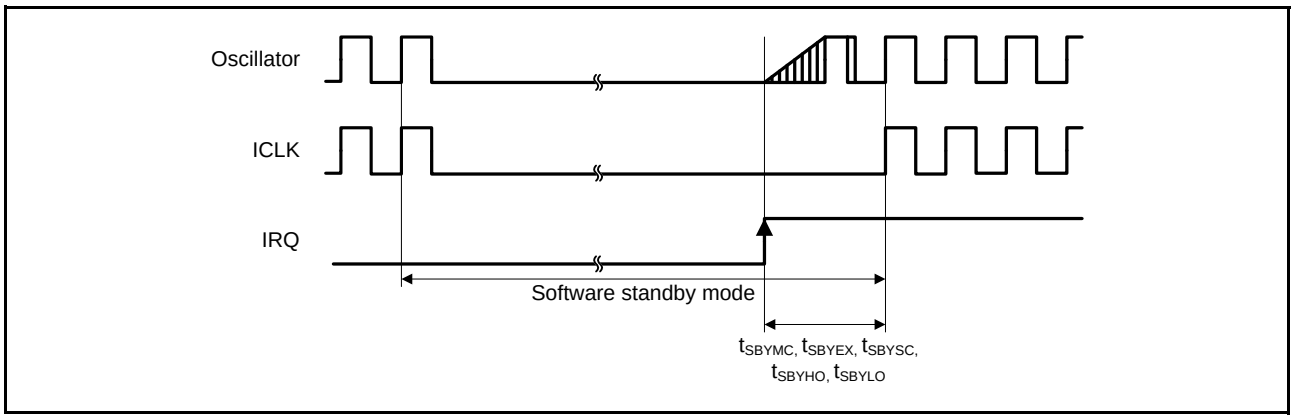

Figure 5.30 Software Standby Mode Cancellation Timing

5.3.5 Timing of On-Chip Peripheral Modules

Table 5.26 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width			t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.33
MTU	Input capture input pulse width		Single-edge setting	t_{TICW}	1.5	—	t_{Pcyc}	Figure 5.34
			Both-edge setting		2.5	—		
	Timer clock pulse width		Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{Pcyc}	Figure 5.35
			Both-edge setting		2.5	—		
			Phase counting mode		2.5	—		
POE	POE# input pulse width			t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.36
8-bit timer	Timer clock pulse width		Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 5.37
			Both-edge setting		2.5	—		
SCI	Input clock cycle		Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 5.38
			Clock synchronous		6	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle*2		Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	C = 30 pF Figure 5.39
			Clock synchronous		4	—		
	Output clock pulse width*2			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time*2			t_{SCKr}	—	20	ns	
	Output clock fall time*2			t_{SCKf}	—	20	ns	
	Transmit data delay time*3	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{TXD}	—	40	ns	
			1.62 V ≤ VCC < 2.7 V		—	80		
	Receive data setup time	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{RXS}	40	—	ns	
			1.62 V ≤ VCC < 2.7 V		80	—		
	Receive data hold time		Clock synchronous	t_{RXH}	40	—	ns	
A/D converter	Trigger input pulse width			t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.40
CAC	CACREF input pulse width		$t_{Pcyc} \le t_{cac}$*4	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
			$t_{Pcyc} > t_{cac}$*4		5 t_{cac} + 6.5 t_{Pcyc}			

Note 1. t_{Pcyc}: PCLKB cycle
Note 2. Value when the drive capacity of clock output ports is set to normal output.
Note 3. Value when the drive capacity of data output ports is set to normal output.
Note 4. t_{cac}: CAC count clock source cycle

Table 5.28 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)*2		t_{SPcyc}	4	65536	t_{Pcyc}	C = 30 pF Figure 5.41
	SCK clock cycle input (slave)			6	65536		
	SCK clock high pulse width*2		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width*2		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	40	—	ns	C = 30 pF Figure 5.42 to Figure 5.47
		1.62 V ≤ VCC < 2.7 V		80	—		
	Data input hold time		t_H	40	—	ns	
	SS input setup time		t_{LEAD}	6	—	t_{Pcyc}	
	SS input hold time		t_{LAG}	6	—	t_{Pcyc}	
	Data output delay time	2.7 V ≤ VCC ≤ 5.5 V	t_{OD}	—	40	ns	
		1.62 V ≤ VCC < 2.7 V		—	80		
	Data output hold time		t_{OH}	0	—	ns	
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	5	t_{Pcyc}	C = 30 pF Figure 5.45 and Figure 5.47
	Slave output release time		t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLKB cycle
Note 2. Value when the drive capacity of clock output ports is set to normal output.

Table 5.29 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, fPCLKB = up to 32 MHz, T_a = –40 to +105°C

Item		Symbol	Min.*1,*2	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 5.48
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (5) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 5.48
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: • t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle
Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. C_b indicates the total capacity of the bus line.

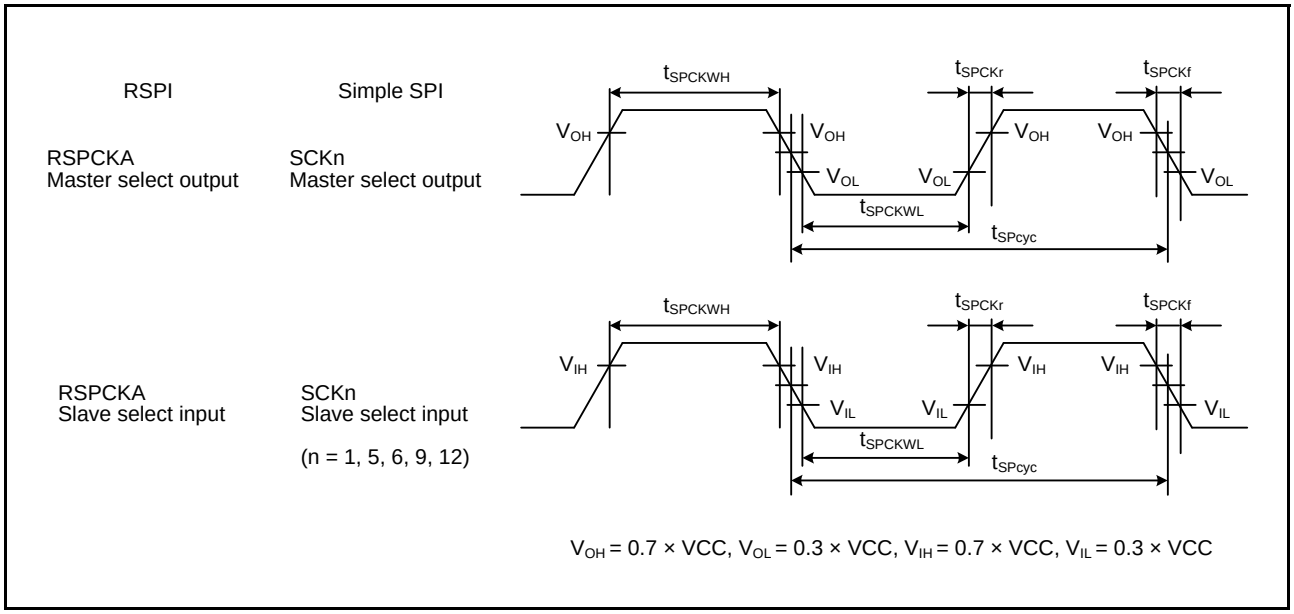

Figure 5.41 RSPI Clock Timing and Simple SPI Clock Timing

5.4 A/D Conversion Characteristics

Table 5.31 A/D Conversion Characteristics (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, 2.7 ≤ VREFH0 ≤ 5.5 V, AVCC0 – 0.9 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
A/D conversion clock frequency (fPCLKD)		1	—	32	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at fPCLKD = 32 MHz)	Permissible signal source impedance (Max.) = 1 kΩ	1.56 (0.652)*2	—	—	µs	Sampling in 20 states
	Permissible signal source impedance (Max.) = 5 kΩ	3.29 (2.35)*2	—	—		Sampling in 75 states
Analog input capacitance		—	—	30	pF	
Offset error		—	±0.5	±4.5	LSB	High-precision channel
				±7.5		Normal-precision channel
Full-scale error		—	±0.75	±4.5	LSB	High-precision channel
				±7.5		Normal-precision channel
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
		—	±1.25	±8.0	LSB	Normal-precision channel
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±3.0	LSB	High-precision channel
		—	±1.0	±5.0	LSB	Normal-precision channel

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.32 Channel Classification for A/D Converter

Classification	Channel	
High-precision channel	AN000 to AN007	It is disallowed to use pins AN000 to AN007 as digital outputs when the A/D converter is used.
Normal-precision channel	AN008 to AN015	

Table 5.33 A/D Internal Reference Voltage Characteristics

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D internal reference voltage	1.35	1.50	1.65	V	

Table 5.34 A/D Conversion Characteristics (2)

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, 1.62 ≤ VREFH0 ≤ 2.7 V, AVCC0 – 0.9 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
A/D conversion clock frequency (fPCLKD)		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at fPCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 1 kΩ	5.25 (1.5)*2	—	—	µs	Sampling in 12 states
	Permissible signal source impedance (Max.) = 5 kΩ	6.25 (2.5)*2	—	—		Sampling in 20 states
Analog input capacitance		—	—	30	pF	
Offset error		—	±0.5	±7.5	LSB	
Full-scale error		—	±1.25	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±1.25	—	LSB	
INL integral nonlinearity error		—	±1.5	±5.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.35 Sampling Time

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Typ.	Unit	Test Conditions
Sampling time	High-precision channel	Ts	0.208 + 0.417 × R0 (kΩ)	µs	Figure 5.49
	Normal-precision channel				

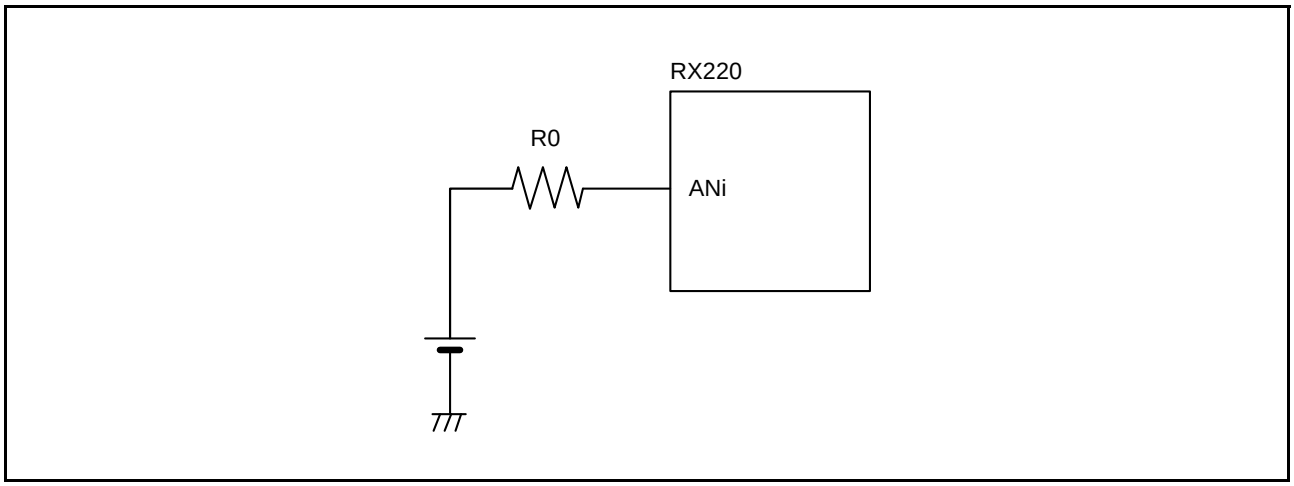

Figure 5.49 Internal Equivalent Circuit of Analog Input Pin

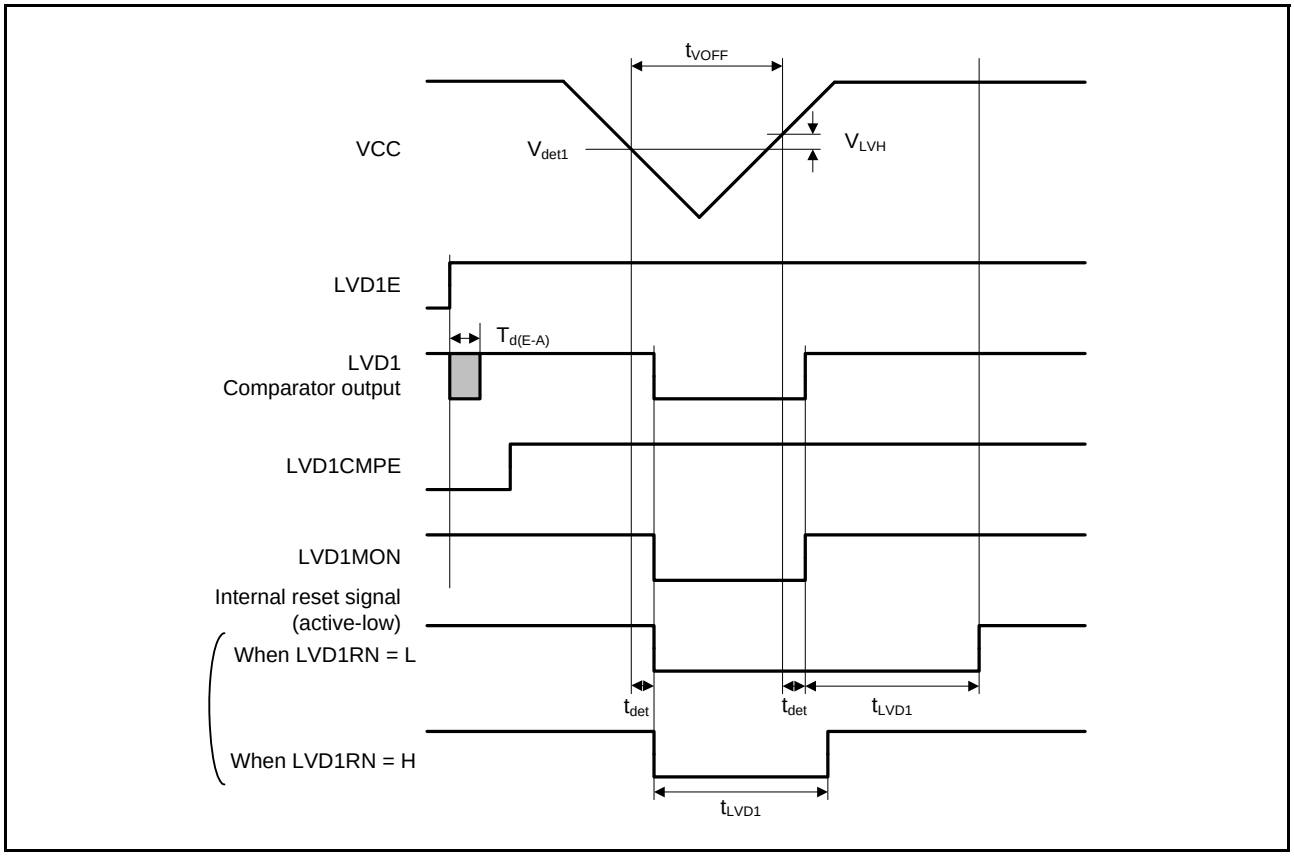

Figure 5.54 Voltage Detection Circuit Timing (V_{det1})

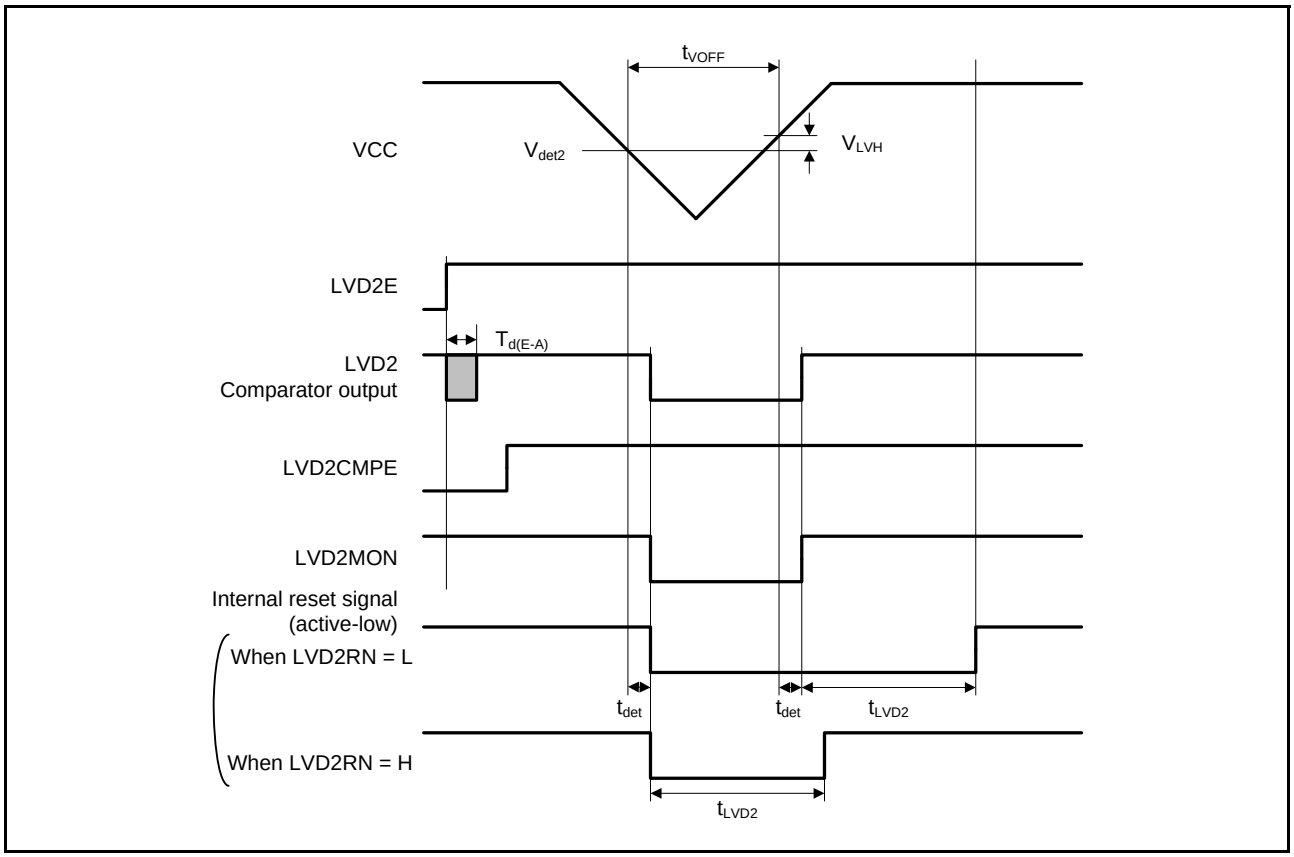

Figure 5.55 Voltage Detection Circuit Timing (V_{det2})

Table 5.42 ROM (Flash Memory for Code Storage) Characteristics (3) medium-speed operating mode 1A

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.19	4.3	—	0.12	2.0	ms
	8 bytes	t_{P8}	—	0.19	4.4	—	0.12	2.0	
	128 bytes	t_{P128}	—	0.67	10.7	—	0.41	4.8	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.23	5.3	—	0.15	2.5	ms
	8 bytes	t_{P8}	—	0.23	5.4	—	0.15	2.5	
	128 bytes	t_{P128}	—	0.80	13.2	—	0.48	6.0	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	13.0	92.8	—	10.5	29	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	15.9	176.9	—	12.8	60	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	0.9	—	—	0.8	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	0.9	—	—	0.8	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	0.9	—	—	0.8	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	0.9	—	—	0.8	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

**Table 5.47 E2 DataFlash Characteristics (4)
medium-speed operating mode 1B**

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VSS = AVSS0 = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.28	5.1	—	0.20	2.8	ms
	8 bytes	t_{DP8}	—	0.32	6.0	—	0.22	3.2	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.36	7.6	—	0.25	4.2	ms
	8 bytes	t_{DP8}	—	0.40	8.8	—	0.28	4.5	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	4.8	32.3	—	4.1	12	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	5.8	51.4	—	4.9	17	ms
Blank check time	2 bytes	t_{DBC2}	—	—	110	—	—	40	µs
	2 Kbytes	t_{DBC2K}	—	—	16.3	—	—	2.6	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	1.7	—	—	1.6	ms

Note 1. The operating frequency is 8 MHz (max.) when the voltage is in the range from 1.62 V to less than 2.7 V.