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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21284sdsp-u0

1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C CPU core, and are packaged in a 20-pin molded-plastic LSSOP. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.

Furthermore, the R8C/29 Group has on-chip data flash (1 KB × 2 blocks).

The difference between the R8C/28 Group and R8C/29 Group is only the presence or absence of data flash. Their peripheral functions are the same.

1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer products, automotive, etc.

1.4 Product Information

Table 1.3 lists the Product Information for R8C/28 Group and Table 1.4 lists the Product Information for R8C/29 Group.

Table 1.3 Product Information for R8C/28 Group

Current of Sep. 2008

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks	
R5F21282SNSP	8 Kbytes	512 bytes	PLSP0020JB-A	N version	
R5F21284SNSP	16 Kbytes	1 Kbyte	PLSP0020JB-A		
R5F21282SDSP	8 Kbytes	512 bytes	PLSP0020JB-A	D version	
R5F21284SDSP	16 Kbytes	1 Kbyte	PLSP0020JB-A		
R5F21284JSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	J version	
R5F21286JSP	32 Kbytes	1.5 Kbyte	PLSP0020JB-A		
R5F21284KSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	K version	
R5F21286KSP	32 Kbytes	1.5 Kbyte	PLSP0020JB-A		
R5F21282SNXXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	N version	Factory programming product ⁽¹⁾
R5F21284SNXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A		
R5F21282SDXXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	D version	
R5F21284SDXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A		
R5F21284JXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	J version	
R5F21286JXXXSP	32 Kbytes	1.5 Kbyte	PLSP0020JB-A		
R5F21284KXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	K version	
R5F21286KXXXSP	32 Kbytes	1.5 Kbyte	PLSP0020JB-A		

NOTE:

1. The user ROM is programmed before shipment.

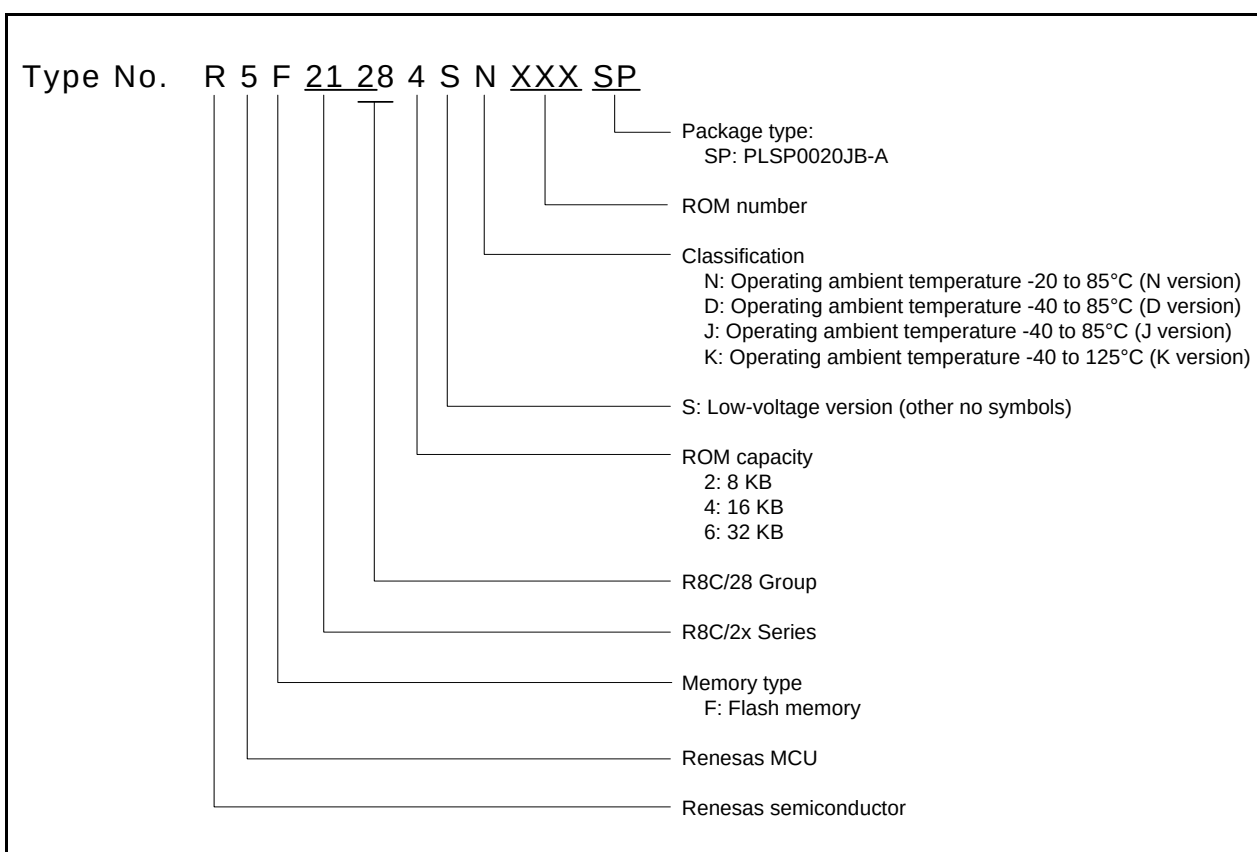


Figure 1.2 Type Number, Memory Size, and Package of R8C/28 Group

Table 1.4 Product Information for R8C/29 Group

Current of Sep. 2008

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F21292SNSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	N version	
R5F21294SNSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A		
R5F21292SDSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	D version	
R5F21294SDSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A		
R5F21294JSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	J version	
R5F21296JSP	32 Kbytes	1 Kbyte × 2	1.5 Kbyte	PLSP0020JB-A		
R5F21294KSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	K version	
R5F21296KSP	32 Kbytes	1 Kbyte × 2	1.5 Kbyte	PLSP0020JB-A		
R5F21292SNXXXSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	N version	Factory programming product ⁽¹⁾
R5F21294SNXXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A		
R5F21292SDXXXSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	D version	
R5F21294SDXXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A		
R5F21294JXXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	J version	
R5F21296JXXXSP	32 Kbytes	1 Kbyte × 2	1.5 Kbyte	PLSP0020JB-A		
R5F21294KXXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	K version	
R5F21296KXXXSP	32 Kbytes	1 Kbyte × 2	1.5 Kbyte	PLSP0020JB-A		

NOTE:

1. The user ROM is programmed before shipment.

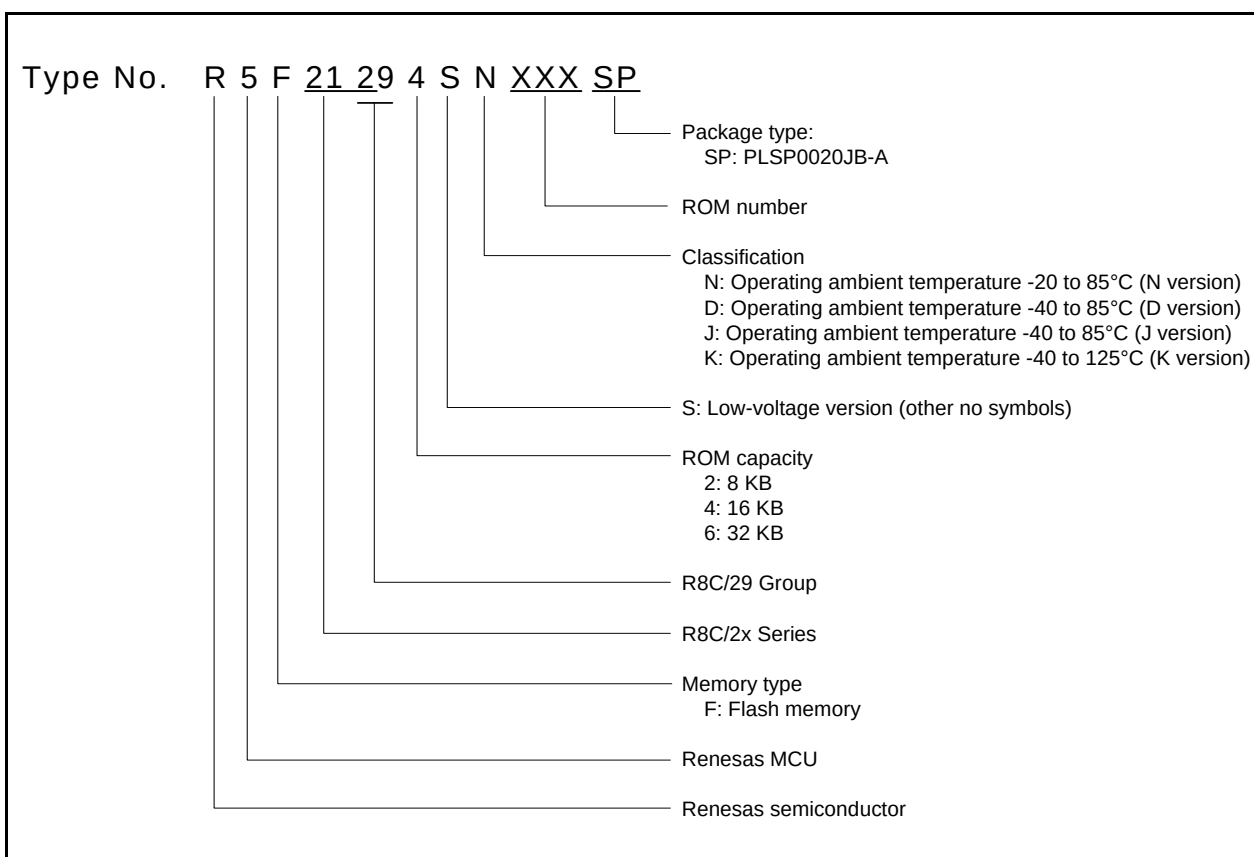


Figure 1.3 Type Number, Memory Size, and Package of R8C/29 Group

1.5 Pin Assignments

Figure 1.4 shows Pin Assignments (Top View).

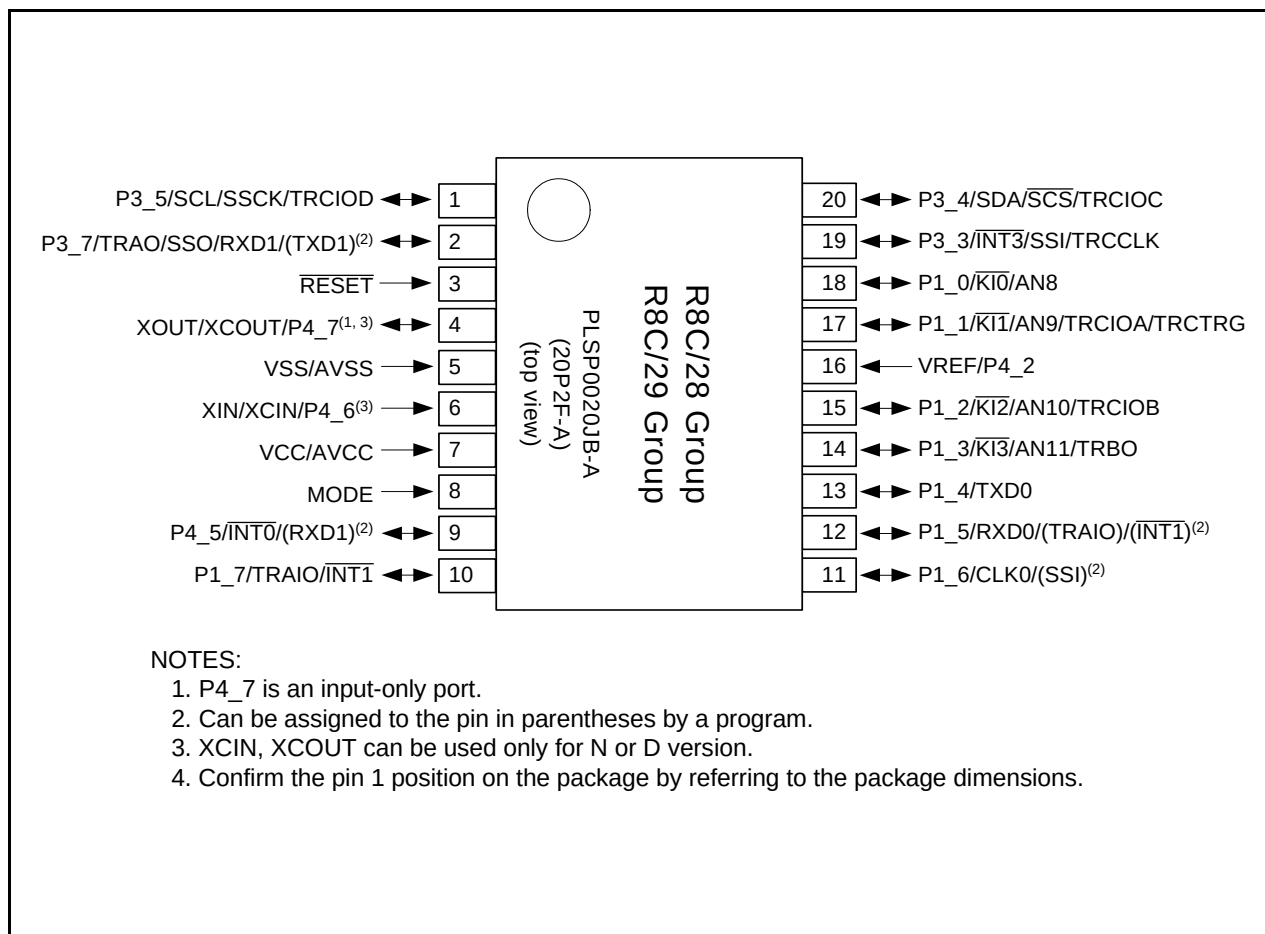


Figure 1.4 Pin Assignments (Top View)

1.6 Pin Functions

Table 1.5 lists Pin Functions.

Table 1.5 Pin Functions

Type	Symbol	I/O Type	Description
Power supply input	VCC, VSS	I	Apply 2.2 to 5.5 V (J, K version are 2.7 to 5.5 V) to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	O	
XCIN clock input (N, D version)	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOU pins. To use an external clock, input it to the XCIN pin and leave the XCOU pin open.
XCIN clock output (N, D version)	XCOU	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRA0	O	Timer RA output pin
	TRAIO	I/O	Timer RA I/O pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCLK	I	External clock input pin
	TRCTR	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIO, TRCIOD	I/O	Sharing output-compare output / input-capture input / PWM / PWM2 output pins
Serial interface	CLK0	I/O	Clock I/O pin
	RXD0, RXD1	I	Receive data input pin
	TXD0, TXD1	O	Transmit data output pin
I ² C bus interface	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
Clock synchronous serial I/O with chip select	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN8 to AN11	I	Analog input pins to A/D converter
I/O port	P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P1_0 to P1_7 also function as LED drive ports (N, D version).
Input port	P4_2, P4_6, P4_7	I	Input-only ports

I: Input O: Output I/O: Input and output

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I ² C bus Interface	A/D Converter
1		P3_5		TRCIOD		SSCK	SCL	
2		P3_7		TRAO	RXD1/(TXD1) ⁽¹⁾	SSO		
3	RESET							
4	XOUT/XCOUT ⁽²⁾	P4_7						
5	VSS/AVSS							
6	XIN/XCIN ⁽²⁾	P4_6						
7	VCC/AVCC							
8	MODE							
9		P4_5	INT0		(RXD1) ⁽¹⁾			
10		P1_7	INT1	TRAIO				
11		P1_6			CLK0	(SSI) ⁽¹⁾		
12		P1_5	(INT1) ⁽¹⁾	(TRAIO) ⁽¹⁾	RXD0			
13		P1_4			TXD0			
14		P1_3	KI3	TRBO				AN11
15		P1_2	KI2	TRCIOB				AN10
16	VRFF	P4_2						
17		P1_1	KI1	TRCIOA/TRCTRG				AN9
18		P1_0	KI0					AN8
19		P3_3	INT3	TRCCLK		SSI		
20		P3_4		TRCIOC		SCS	SDA	

NOTES:

1. This can be assigned to the pin in parentheses by a program.
2. XCIN, XCOUT can be used only for N or D version.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

Table 4.5 SFR Information (5)⁽¹⁾

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRES	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register ⁽²⁾	TREHR	00h
011Bh	Timer RE Day of Week Data Register ⁽²⁾	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011111b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. In J, K version these regions are reserved. Do not access locations in these regions.

5. Electrical Characteristics

5.1 N, D Version

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V _{CC} /AV _{CC}	Supply voltage		-0.3 to 6.5	V
V _I	Input voltage		-0.3 to V _{CC} + 0.3	V
V _O	Output voltage		-0.3 to V _{CC} + 0.3	V
P _d	Power dissipation	T _{opr} = 25°C	500	mW
T _{opr}	Operating ambient temperature		-20 to 85 (N version) / -40 to 85 (D version)	°C
T _{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V _{CC} /AV _{CC}	Supply voltage			2.2	–	5.5	V
V _{SS} /AV _{SS}	Supply voltage			–	0	–	V
V _{IH}	Input "H" voltage			0.8 V _{CC}	–	V _{CC}	V
V _{IL}	Input "L" voltage			0	–	0.2 V _{CC}	V
I _{OH} (sum)	Peak sum output "H" current	Sum of all pins I _{OH} (peak)		–	–	-160	mA
I _{OH} (sum)	Average sum output "H" current	Sum of all pins I _{OH} (avg)		–	–	-80	mA
I _{OH} (peak)	Peak output "H" current	Except P1_0 to P1_7		–	–	-10	mA
		P1_0 to P1_7		–	–	-40	mA
I _{OH} (avg)	Average output "H" current	Except P1_0 to P1_7		–	–	-5	mA
		P1_0 to P1_7		–	–	-20	mA
I _{OL} (sum)	Peak sum output "L" currents	Sum of all pins I _{OL} (peak)		–	–	160	mA
I _{OL} (sum)	Average sum output "L" currents	Sum of all pins I _{OL} (avg)		–	–	80	mA
I _{OL} (peak)	Peak output "L" currents	Except P1_0 to P1_7		–	–	10	mA
		P1_0 to P1_7		–	–	40	mA
I _{OL} (avg)	Average output "L" current	Except P1_0 to P1_7		–	–	5	mA
		P1_0 to P1_7		–	–	20	mA
f _(XIN)	XIN clock input oscillation frequency		3.0 V ≤ V _{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V _{CC} < 3.0 V	0	–	10	MHz
			2.2 V ≤ V _{CC} < 2.7 V	0	–	5	MHz
f _(XCIN)	XCIN clock input oscillation frequency		2.2 V ≤ V _{CC} ≤ 5.5 V	0	–	70	kHz
–	System clock	OCD2 = 0 XIN clock selected	3.0 V ≤ V _{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V _{CC} < 3.0 V	0	–	10	MHz
			2.2 V ≤ V _{CC} < 2.7 V	0	–	5	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	–	125	–	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 3.0 V ≤ V _{CC} ≤ 5.5 V	–	–	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.7 V ≤ V _{CC} ≤ 5.5 V	–	–	10	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.2 V ≤ V _{CC} ≤ 5.5 V	–	–	5	MHz

NOTES:

1. V_{CC} = 2.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics⁽⁴⁾

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		10,000 ⁽³⁾	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	50	400	μs
—	Byte program time (program/erase endurance > 1,000 times)		—	65	—	μs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	9	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	97 + CPU clock × 6 cycles	μs
—	Interval from erase start/restart until following suspend request		650	—	—	μs
—	Interval from program start/restart until following suspend request		0	—	—	ns
—	Time from suspend until program/erase restart		—	—	3 + CPU clock × 4 cycles	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		2.2	—	5.5	V
—	Program, erase temperature		-20 ⁽⁸⁾	—	85	°C
—	Data hold time ⁽⁹⁾	Ambient temperature = 55°C	20	—	—	year

NOTES:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. -40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.13 Timing Requirements of Clock Synchronous Serial I/O with Chip Select⁽¹⁾

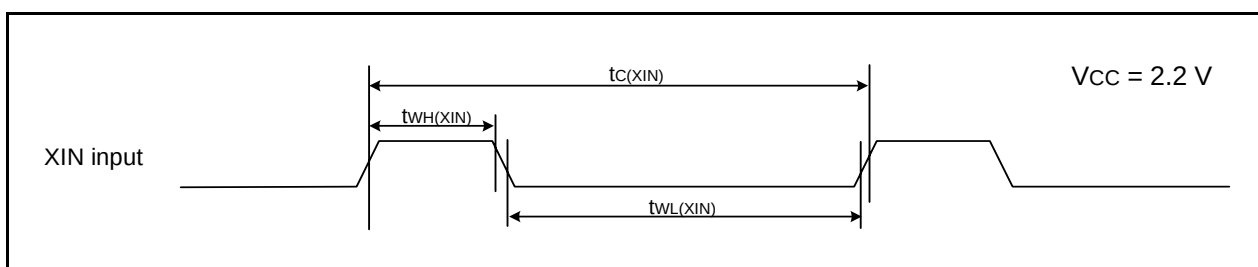
Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc ⁽²⁾
t _{HI}	SSCK clock "H" width			0.4	–	0.6	tsucyc
t _{LO}	SSCK clock "L" width			0.4	–	0.6	tsucyc
trise	SSCK clock rising time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tfall	SSCK clock falling time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
t _H	SSO, SSI data input hold time			1	–	–	tcyc ⁽²⁾
t _{LEAD}	$\overline{\text{SCS}}$ setup time	Slave		1tcyc + 50	–	–	ns
t _{LAG}	$\overline{\text{SCS}}$ hold time	Slave		1tcyc + 50	–	–	ns
t _{OD}	SSO, SSI data output delay time			–	–	1	tcyc ⁽²⁾
tsa	SSI slave access time		2.7 V ≤ V _{CC} ≤ 5.5 V	–	–	1.5tcyc + 100	ns
			2.2 V ≤ V _{CC} < 2.7 V	–	–	1.5tcyc + 200	ns
tor	SSI slave out open time		2.7 V ≤ V _{CC} ≤ 5.5 V	–	–	1.5tcyc + 100	ns
			2.2 V ≤ V _{CC} < 2.7 V	–	–	1.5tcyc + 200	ns

NOTES:

1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1tcyc = 1/f₁(s)

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 2.2\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 2.2\text{ V}$]****Table 5.30 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.16 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.31 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	–	ns

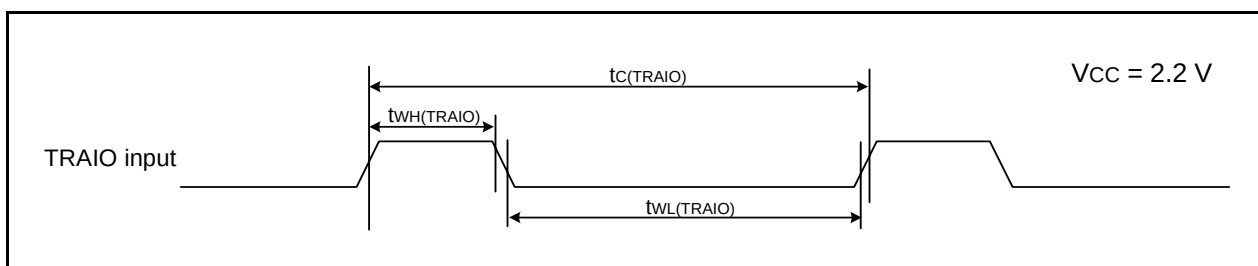
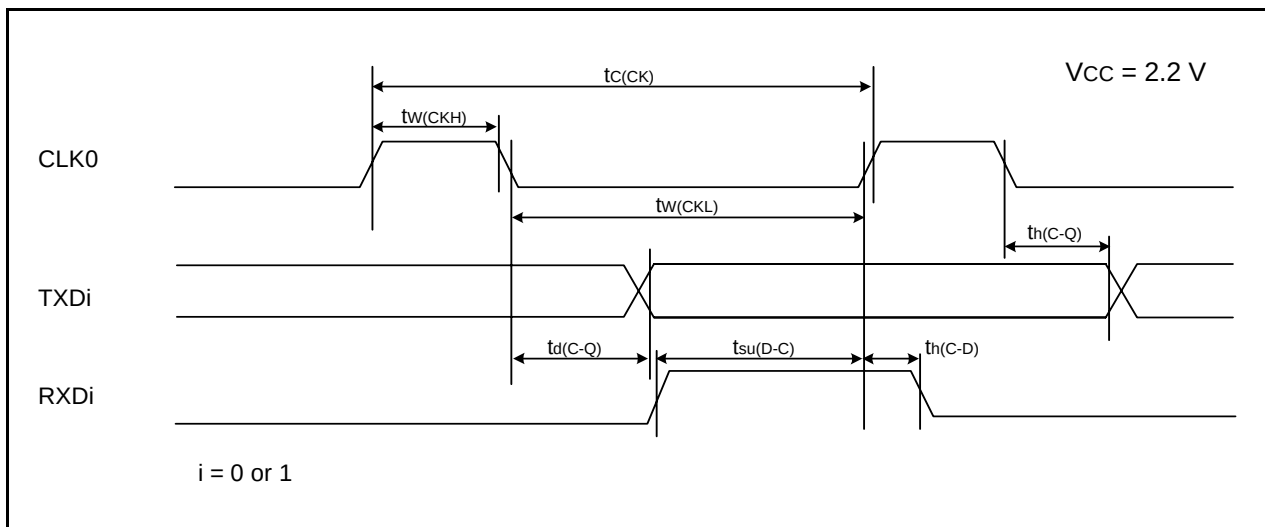
**Figure 5.17 TRAIO Input Timing Diagram when $V_{CC} = 2.2\text{ V}$**

Table 5.32 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	800	—	ns
$t_{w(CKH)}$	CLK0 input "H" width	400	—	ns
$t_{w(CKL)}$	CLK0 input "L" width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 or 1

**Figure 5.18 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.33 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	1000 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	1000 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

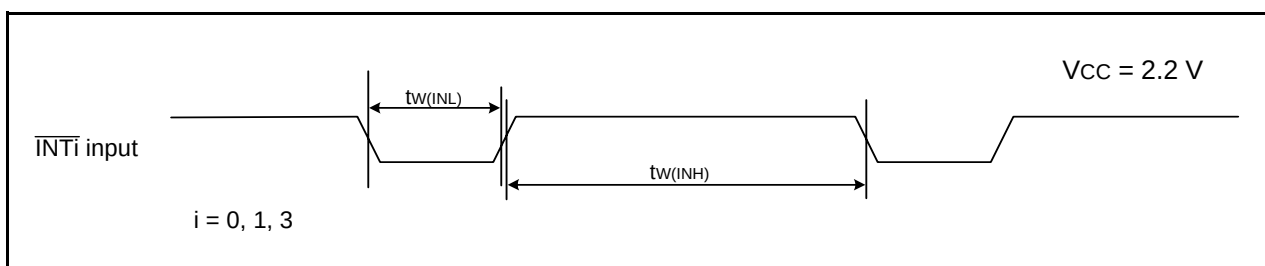
**Figure 5.19 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 2.2 V**

Table 5.37 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance ⁽²⁾	R8C/28 Group	100 ⁽³⁾	–	–	times
		R8C/29 Group	1,000 ⁽³⁾	–	–	times
–	Byte program time		–	50	400	μs
–	Block erase time		–	0.4	9	s
t _d (SR-SUS)	Time delay from suspend request until suspend		–	–	97 + CPU clock × 6 cycles	μs
–	Interval from erase start/restart until following suspend request		650	–	–	μs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycles	μs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	–	–	year

NOTES:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

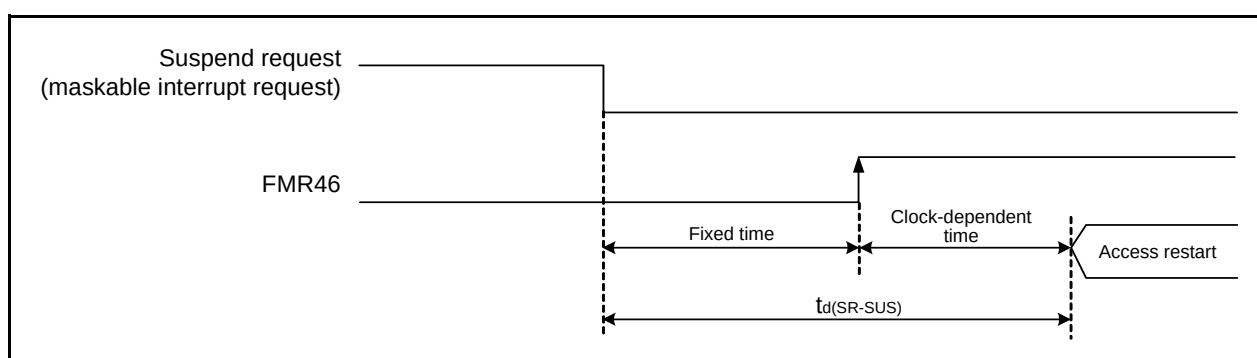


Figure 5.21 Time delay until Suspend

Table 5.39 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet1	Voltage detection level ^(2, 4)		2.70	2.85	3.0	V
td(Vdet1-A)	Voltage monitor 1 reset generation time ⁽⁵⁾		—	40	200	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	0.6	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs
Vccmin	MCU operating voltage minimum value		2.70	—	—	V

NOTES:

1. The measurement condition is Vcc = 2.7 to 5.5 V and Topr = -40 to 85°C (J version) / -40 to 125°C (K version).
2. Hold Vdet2 > Vdet1.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.
5. Time until the voltage monitor 1 reset is generated after the voltage passes Vdet1 when Vcc falls. When using the digital filter, its sampling time is added to td(Vdet1-A). When using the voltage monitor 1 reset, maintain this time until Vcc = 2.0 V after the voltage passes Vdet1 when the power supply falls.

Table 5.40 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level ⁽²⁾		3.3	3.6	3.9	V
td(Vdet2-A)	Voltage monitor 2 reset/interrupt request generation time ^(3, 5)		—	40	200	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	0.6	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽⁴⁾		—	—	100	μs

NOTES:

1. The measurement condition is Vcc = 2.7 to 5.5 V and Topr = -40 to 85°C (J version) / -40 to 125°C (K version).
2. Hold Vdet2 > Vdet1.
3. Time until the voltage monitor 2 reset/interrupt request is generated after the voltage passes Vdet2.
4. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
5. When using the digital filter, its sampling time is added to td(Vdet2-A). When using the voltage monitor 2 reset, maintain this time until Vcc = 2.0 V after the voltage passes Vdet2 when the power supply falls.

Table 5.47 Electrical Characteristics (1) [V_{CC} = 5 V]

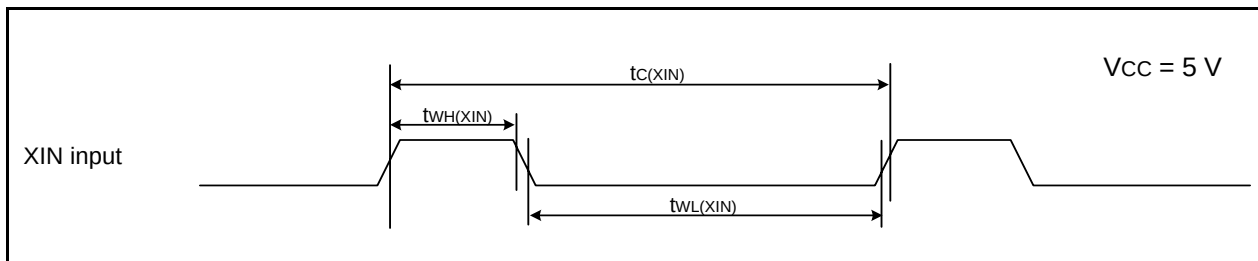
Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except XOUT	I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
			I _{OH} = -200 μA	V _{CC} - 0.3	—	V _{CC}	V
		XOUT	Drive capacity HIGH I _{OH} = -1 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity LOW I _{OH} = -500 μA	V _{CC} - 2.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except XOUT	I _{OL} = 5 mA	—	—	2.0	V
			I _{OL} = 200 μA	—	—	0.45	V
		XOUT	Drive capacity HIGH I _{OL} = 1 mA	—	—	2.0	V
			Drive capacity LOW I _{OL} = 500 μA	—	—	2.0	V
V _{T+} -V _{T-}	Hysteresis	$\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT3}},$ KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO		0.1	0.5	—	V
		$\overline{\text{RESET}}$		0.1	1.0	—	V
I _{IH}	Input "H" current		V _I = 5 V, V _{CC} = 5V	—	—	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 5V	—	—	-5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 5V	30	50	167	kΩ
R _{fXIN}	Feedback resistance	XIN		—	1.0	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode	2.0	—	—	V

NOTE:

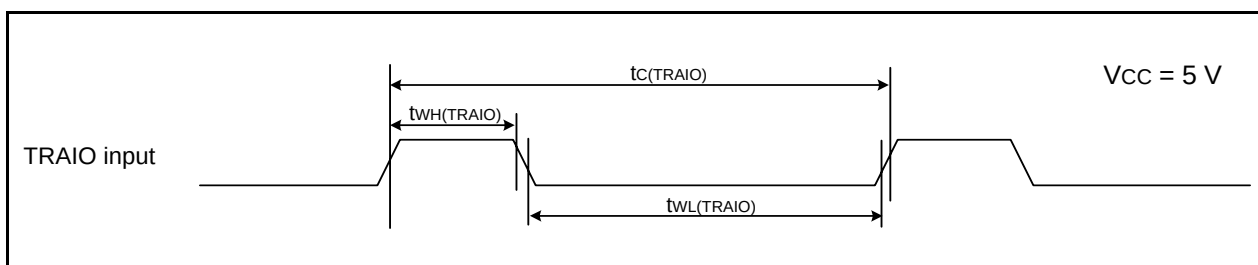
1. V_{CC} = 4.2 to 5.5 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 5\text{ V}$]****Table 5.49 XIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input "H" width	25	–	ns
$t_{WL(XIN)}$	XIN input "L" width	25	–	ns

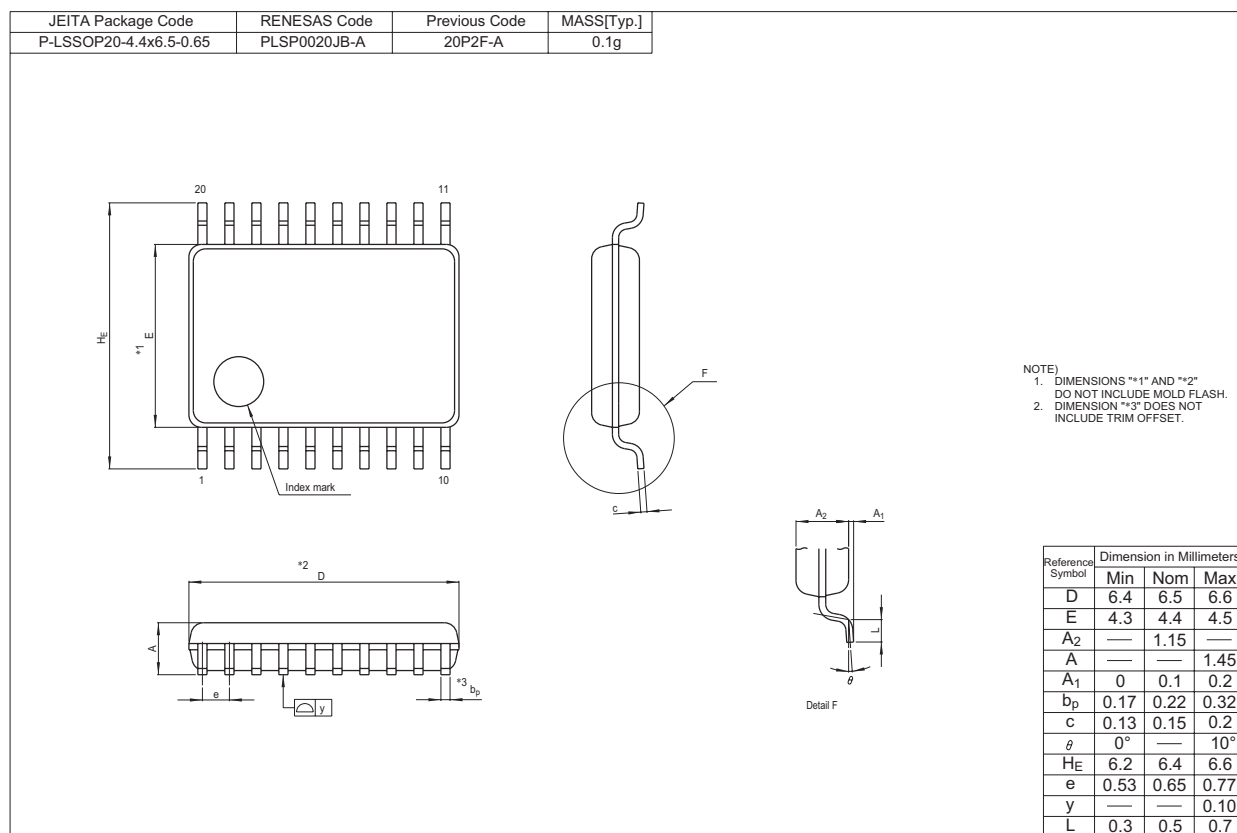
**Figure 5.27 XIN Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.50 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	40	–	ns

**Figure 5.28 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.



REVISION HISTORY	R8C/28 Group, R8C/29 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.10	Nov 14, 2005	–	First Edition issued
0.30	Feb 28, 2006	all pages	“J, K version” added
		1	1.1 Applications revised
		2	Table 1.1 Functions and Specifications for R8C/28 Group revised
		3	Table 1.2 Functions and Specifications for R8C/29 Group revised
		4	Figure 1.1 Block Diagram; NOTE3 added
		5	Table 1.3 Product Information for R8C/28 Group and Figure 1.2 Type Number, Memory Size, and Package of R8C/28 Group revised
		6	Table 1.4 Product Information for R8C/29 Group and Figure 1.3 Type Number, Memory Size, and Package of R8C/29 Group revised
		7	Figure 1.4 Pin Assignments (Top View); NOTE3 added
		8	Table 1.5 Pin Functions revised
		9	Table 1.6 Pin Name Information by Pin Number; “XOUT” → “XOUT/XCOUT”, “XIN” → “XIN/XCIN” revised and NOTE2 added
		13	Figure 3.1 Memory Map of R8C/28 Group; “R5F21284JSP, R5F21284KSP” added
		14	Figure 3.2 Memory Map of R8C/29 Group; “R5F21294JSP, R5F21294KSP” added
		15	Table 4.1 SFR Information (1); NOTE6 added
		18	Table 4.4 SFR Information (4); 00FEh: “DRR” → “P1DRR” symbol name revised
		22 to 66	5. Electrical Characteristics added
0.40	Mar 29, 2006	2	Table 1.1 Functions and Specifications for R8C/28 Group revised
		3	Table 1.2 Functions and Specifications for R8C/29 Group revised
		15	Table 4.1 SFR Information (1); - 0032h, 0036h, 0038h revised - NOTES 2 to 6 revised and NOTES 7 to 8 added
		19	Table 4.5 SFR Information (5); NOTE2 added
0.50	Apr 27, 2006	18	Table 4.4; 00FDh: revised
		46	Table 5.35; System clock Conditions: revised
1.00	Nov 08, 2006	All pages	“PRELIMINARY” deleted
		1	1 “J and K versions are under development...notice.” added
		2	Table 1.1 revised
		3	Table 1.2 revised
		4	Figure 1.1 revised
		5	Table 1.3 revised
		6	Table 1.4 revised

REVISION HISTORY

R8C/28 Group, R8C/29 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.10	May 17, 2007	13	Figure 3.1 revised
		14	Figure 3.2 revised
		18	Table 4.4 NOTE2 added
		28	Table 20.10 revised
		51	Table 20.39 NOTE4 added
		53	Table 20.42 revised
1.20a	Jun 11, 2007	1	1 "J and K versions are under development. Specifications may be changed without prior notice." deleted
		5, 6	Table 1.3 and Table 1.4 "(D): Under development" and NOTE1 deleted
		47	5.2 "J and K versions are under development. Specifications may be changed without prior notice." deleted
2.00	Mar 14, 2008	5	Table 1.3, Figure 1.2 revised
		6	Table 1.4, Figure 1.3 revised
		13, 14	Figure 3.1, Figure 3.2 revised
		15	Table 4.1 "002Ch" added
		16	Table 4.2 "0036h"; J, K version "0100X000b" → "0100X001b"
		22, 47	Table 5.2, Table 5.35; NOTE2 revised
2.10	Sep 26, 2008	28	Table 5.10 revised, NOTE4 added
		–	"RENESAS TECHNICAL UP DATE" reflected: TN-16C-A172A/E
		24, 49	Table 5.4, Table 5.37 NOTE2, NOTE4 revised
		25, 50	Table 5.5, Table 5.38 NOTE2, NOTE5 revised
		51	Table 5.39 Parameter: Voltage monitor 1 reset generation time added NOTE5 added
		52	Table 5.40 revised Table 5.41 revised Figure 5.22 revised

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