



Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, LINbus, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21286jsp-w4

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### Notice

- 1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
- Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
- 3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
- 4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
- 5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
- 6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
- 7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.
  - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
  - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anticrime systems; safety equipment; and medical equipment not specifically designed for life support.
  - "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
- 8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
- 9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
- 10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
- 11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
- 12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.
- (Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majorityowned subsidiaries.
- (Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

#### **1.2 Performance Overview**

Table 1.1 outlines the Functions and Specifications for R8C/28 Group and Table 1.2 outlines the Functions and Specifications for R8C/29 Group.

CPU         Number of fundamental instructions         89 instructions           Minimum instruction execution time         50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) (diversion) (22.5 ns (f(XIN) = 16 MHz, VCC = 2.2 to 5.5 V) 200 ns (f(XIN) = 10 MHz, VCC = 2.2 to 5.5 V) (N. D version)           Operating mode         Single-chip           Address space         1 Mbyte           Memory capacity         Refer to Table 1.3 Product Information for R8C/28 Group           Peripheral         Ports           Functions         ICD ports: 13 pins, Input port: 3 pins           Timer Rs: B bits x 1 channel (ICD ports: 15 bits x 1 channel (Input capture and output compare match function (For J, K version, compare match function (For J, K version, compare match function (For J, K version, compare match function (IQART0): Clock synchronous serial I/O, UART 1           Clock synchronous serial interface         1 channel (UART0): Clock synchronous serial I/O, UART 1           It mer R1: B bit x 1 channel (UMRT0): Clock synchronous serial I/O, UART 1         1 channel (UART0): Clock synchronous serial I/O, UART 1           It mer R1: B bit x 1 channel (UMRT0): Clock synchronous serial I/O, UART 1         1 channel           Interrupts         Internace           Interrupts         Internace           Vato converter         10-bit A/D converter: 1 circuit, 4 channels           Vatodog timer         15 bits x 1 channel (timer R2, UART0)           A/D converter         10-bit A/D con		ltem	Specification
instructions         50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) (other than K version) execution time           Minimum instruction execution time         50 ns (f(XIN) = 10 MHz, VCC = 3.0 to 5.5 V) (200 ns (f(XIN) = 10 MHz, VCC = 2.2 to 5.5 V) 200 ns (f(XIN) = 10 MHz, VCC = 2.2 to 5.5 V)           Operating mode         Single-chip           Address space         1 Mbyte           Memory capacity         Refer to Table 1.3 Product Information for R8C/28 Group           Peripheral         Ports         I/O ports: 3 pins, Input port: 3 pins           Functions         LED drive ports         I/O ports: 8 bits x 1 channel           Timer R:         B bits x 1 channel         Timer R8: 8 bits x 1 channel           Timer R:         B bits x 1 channel         Timer R8: 9 bits x 1 channel           Timer R:         1 channel (UART0): Clock synchronous serial I/O, UART           Clock synchronous serial         1 channel           Timer R:         1 channel           Interface         1 channel           Interface         1 channel           Interface         1 channel           VD covverter         1 obannel           ND covverter         1 obannel           VD covverter         1 obannel           VD covverter         1 obannel           VD covverter         1 obannel	CPU	Number of fundamental	89 instructions
Minimum instruction execution time         50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) (Kwersion)           00 ns (f(XIN) = 10 MHz, VCC = 3.0 to 5.5 V) (Kwersion)           100 ns (f(XIN) = 10 MHz, VCC = 3.0 to 5.5 V) (N. p version)           Operating mode           Address space           1 Mbyte           Peripheral           Ports           Functions           1 ED drive ports           1 More capacity           Refer to Table 1.3 Product Information for R8C/28 Group           Peripheral           Ports           1 More capacity           Timer R3: B bits x 1 channel           (Input capture and output compare circuits)           Timer R2: B bits x 1 channel           (Input capture and output compare match function (For J, K version, compare match function only.)           Serial interfaces         1 channel (UART1): UART           Clock synchronous serial         1 channel           Interface         1 channel           IND module         Hardware LIN: 1 channel (With prescaler)           Arb converter         10-bit X-0 converter.1 circuit, 4 channels           VAD converter         10-bit X-4 sources, Software: 4 sources, Friority levels: 7 levels           Clock synchronous serial         1 Couk interface(1)           Clock synchronous serial VO,		instructions	
execution time         62.5 ns (f(XIN) = 16 MHz, VCC = 2.2 to 5.5 V) 200 ns ((XIN) = 10 MHz, VCC = 2.2 to 5.5 V) 200 ns ((XIN) = 10 MHz, VCC = 2.2 to 5.5 V)           Operating mode         Single-chip           Address space         1 Mbyte           Memory capacity         Refer to Table 1.3 Product Information for R8C/28 Group           Peripheral         Ports         I/O ports: 3 pins, Input port: 3 pins           Functions         LED drive ports         I/O ports: 8 bits x 1 channel           Timer R0: 8 bits x 1 channel         Timer R0: 8 bits x 1 channel           Timer R0: 16 bits x 1 channel         (Input capture and output compare circuits)           Timer R0: 16 bits x 1 channel         Timer R0: 10 bits x 1 channel           (Input capture and output compare match function on (For J, K version, compare match function on (For J, K version, compare match function on (For J, K version, compare match function on (CART1): UART           Clock synchronous serial         1 channel           interface         1 channel           I/2 bus Interface(1)         Clock synchronous serial I/O with chip select           LIN module         Hardware LIN: 1 channel (timer RA, UART0)           A/D converter         10-bit A/D converter.1 circuit, 4 channels           Vatidog timer         15 bits x 1 channel (timer RA, UART0)           A/D converter         10-bit A/D converter.1 circuit, 4 channels		Minimum instruction	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) (other than K version)
100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) (n, D version)           Operating mode         Single-chip           Address space         1 Mbyte           Memory capacity         Refer to Table 1.3 Product Information for R8C/28 Group           Peripheral         Ports         1/O ports: 13 pins, Input port: 3 pins           Functions         LED drive ports         1/O ports: 13 pins, Input port: 3 pins           Timer R3: B bits x 1 channel         Timer R4: 8 bits x 1 channel           Timer R5: With real-time clock and compare match function (For J, K version, compare match function only.)         Timer RE: With real-time clock and compare match function (For J, K version, compare match function only.)           Serial interfaces         1 channel (UART): UART         Clock synchronous serial 1/O with chip select           Clock synchronous serial         1 channel (UART): UART         Clock synchronous serial 1/O with chip select           LIN module         Hardware LIN: 1 channel (Wint Prescaler)         Reset at selectable           Interrace         10-bit A/D converter: 1 circuit, 4 channels         Version)           Vatchdog timer         15 bits x 1 channel (Wint prescaler)         Reset at selectable           Interrace         1/2 bus x 1 channel (Wint prescaler)         Nachod g timer         10-bit A/D converter: 1 circuit, 4 channels           Vatchdog timer         15 bits x 1 channel (Wint prescaler)		execution time	62.5 ns (f(XIN) = 16 MHz, VCC = 3.0 to 5.5 V) (K version)
200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V) (N, D version)           Operating mode         Single-chip           Address space         1 Mbyte           Memory capacity         Refer to Table 1.3 Product Information for R8C/28 Group           Peripheral         Ports         1/O ports: 3 pins, Input port: 3 pins           Functions         LED drive ports         1/O ports: 13 pins, Input port: 3 pins           Timer RS:         Nins: 8 bits x 1 channel         Timer R8: 8 bits x 1 channel           Timer RC:         16 bits x 1 channel         (Input capture and output compare match function on (For 1, K version, compare match function on (For 1, K version, compare match function on (For 1, K version, compare match function on V):           Serial interfaces         1 channel (UARTO): Clock synchronous serial I/O, UART           Clock synchronous serial         1 channel         1 channel           Interface         1 channel         1/O ports: 15 sources (N, D version), Internal: 14 sources (J K version)           Katchdog timer         15 bits x 1 channel (With prescaler)         Reset start selectable           Watchdog timer         15 bits x 1 channel (With prescaler)         Nersion), Internal: 14 sources (J K version)           Vatterface         10 channel         1/O converter         10 channel           Vatchdog timer         15 bits x 1 chanel (With prescaler)         Nesset start selectable			100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
Operating mode         Single-chip           Address space         1 Möyre           Memory capacity         Refer to Table 1.3 Product Information for R8C/28 Group           Peripheral         Ports         1/O ports: 13 pins, Input port: 3 pins           Functions         IED drive ports         1/O ports: 18 bins (1 channel           Timer RS:         18 bits x 1 channel         (Each timer equipped with 8-bit prescaler)           Timer RS:         16 bits x 1 channel         (Each timer equipped with 8-bit prescaler)           Timer RS:         16 bits x 1 channel         (Input capture and output compare circuits)           Timer RS:         1 channel (UART0): Clock synchronous serial I/O, UART         1 channel (UART1): UART           Clock synchronous serial         1 channel (UART0): Clock synchronous serial I/O, UART         1 channel (UART1): UART           Clock synchronous serial         10 bit X 1 channel (With prescaler)         Reset start selectable           Internate         10 bit X 0 converter.         10 bit X 0 converter.         10 bit X 1 channel (With prescaler)           Vatchdog timer         10 bit X 1 channel (With prescaler)         Reset start selectable         1           Internate         1 sources (N, D version), Internal: 14 sources (J, K version)         2 sources (N, D version)         2 sources (N, D version)           Vottabde detection circuit<			200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V) (N, D version)
Address space         1 Mbyte           Memory capacity         Refer to Table 1.3 Product Information for R8C/28 Group           Peripheral Functions         Ports         UO ports: 13 pins, Input port: 3 pins           Timer RS:         Bits x1 channel         Timer RS: 8 bits x1 channel           Timer RC:         16 bits x1 channel         (Input capture and output compare circuits)           Timer RC:         16 bits x1 channel         (Input capture and output compare circuits)           Serial Interfaces         1 channel (UART0): Clock synchronous serial I/O, UART           Clock synchronous serial         1 channel         (Input capture and output compare match function only.)           Serial Interfaces         1 channel         (UART0): Clock synchronous serial I/O, UART           I channel         1 channel         (Input capture and output compare match function only.)           Add converter         1 channel         (Internat: 10, UART0)           Add converter         1 channel         (Internat: 14, Cource)           IN module         Hardware LIN: 1 channel (with prescaler)         Reset stat selectable           Internat: 15 sources (N, D version), Internat: 14 sources (J, K version)         External: 4 sources, (N, D version), Internat: 14 sources (J, K version)           Voltage detection circuit         0-n-chip oscillator high speed, low speed)         High speed on-chip oscilla		Operating mode	Single-chip
Memory capacity         Refer to Table 1.3 Product Information for R8C/28 Group           Peripheral         Ports         1/0 ports: 3 pins, Input port: 3 pins           Functions         LED drive ports         1/0 ports: 8 pins, IN, Dv resion)           Timer R         Bits x 1 channel (Each timer equipped with 8-bit prescaler) (Input capture and output compare match function (For J, K version, compare match function only.)           Serial interfaces         1 channel (UART0): Clock synchronous serial 1/0, UART           Clock synchronous serial interface         1 channel (UART0): Clock synchronous serial 1/0, UART           Clock synchronous serial interface         1 channel (UART0): Clock synchronous serial 1/0, UART           Clock synchronous serial interface         1 channel (UART0): Clock synchronous serial 1/0, UART           Vatchdog timer         10 bits x 1 channel (With rescaler)           Vatchdog timer         10 bits x 1 channel (with prescaler)           Reset start selectable         Internal: 15 sources (N, D version), Internal: 14 sources (J, K version)           Interrupts         Internal: 15 sources (N, D version), Internal: 14 sources (J, K version)           Voltage detection circuit         3 circuits           Vill ock generation circuit (with on -chip feedback resistor)           On-chip         On-chip           Power on reset zircuit         On-chip           Power on reset zircuit         <		Address space	1 Mbyte
Peripheral         Ports         I/O ports: 31 pins, Input port: 3 pins           Functions         LED drive ports         I/O ports: 81 pins, IND version)           Timers         Timer RA: 8 bits x 1 channel           Timer RA: 8 bits x 1 channel         (Each timer equipped with 8-bit prescaler)           Timer RC: 16 bits x 1 channel         (Input capture and output compare circuits)           Timer RC: 16 bits x 1 channel         (Input capture and output compare match function only.)           Serial interfaces         1 channel (UART1): UART           Clock synchronous serial         1 channel           ILIN module         Hardware LIN: 1 channel (timer RA, UART0)           A/D converter         10-bit A/D converter: 1 circuit, 4 channels           Watchdog timer         15 bits x 1 channel (with prescaler)           Reset start selectable         Internal: 15 sources (N, D version), Internal: 14 sources (J, K version)           Internal: 3 sources (N, D version), Internal: 14 sources (J, K version)         • XIN clock oscillator (with on-chip feedback resistor)           • On-chip oscillator (ligt speed, low speed)         • XIN clock socillator nas a frequency adjustment function           • Violage detection circuit         On-chip         • XIN clock socillator nas a frequency adjustment function           • Violage detection circuit         On-chip         • XIN clock socillator nas a frequency adjustment function </td <td></td> <td>Memory capacity</td> <td>Refer to Table 1.3 Product Information for R8C/28 Group</td>		Memory capacity	Refer to Table 1.3 Product Information for R8C/28 Group
Functions         LED drive ports         I/O ports: 8 pins (N, D version)           Timer R3         Timer R4: 8 bits x 1 channel           Timer R6: 16 bits x 1 channel         Timer R6: 76 bits x 1 channel           (Each timer equipped with 8-bit prescaler)         Timer R0: 16 bits x 1 channel           (Each timer equipped with 8-bit prescaler)         Timer R0: 16 bits x 1 channel           (Each timer equipped with 8-bit prescaler)         Timer R0: 16 bits x 1 channel           (Each timer equipped with 8-bit prescaler)         Timer R0: 16 bits x 1 channel           (Each timer equipped with 8-bit prescaler)         Timer R0: 16 bits x 1 channel           (Each x)         Clock synchronous serial         I/O, UART           1 channel (UART1): UART         Clock synchronous serial         I/O, UART           1 channel         Internal: UAR onter R0: KARTO)         AD           A/D converter         10-bit A/D converter: 1 circuit, 4 channels           Watchdog timer         15 bits x 1 channel (with prescaler)           Reset start selectable         Internal: 15 sources (N, D version), Internal: 14 sources (J, K version)           Internuts         Internal: 4 sources, Software: 4 sources, Priority levels: 7 levels           3 circuits         3 circuits         3 circuits           • XIN clock generation circuit (with on-chip feedback resistor)         • On-chip oscillator hi	Peripheral	Ports	I/O ports: 13 pins, Input port: 3 pins
Timers         Timer RA: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer RC: 16 bits x 1 channel (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function (For J, K version, compare match function only.)           Serial interfaces         1 channel (UART0): Clock synchronous serial I/O, UART           Clock synchronous serial interface         1 channel (UART1): UART           Clock synchronous serial interface         1 channel 1/C bus Interface(1) Clock synchronous serial I/O with chip select           LIN module         Hardware LIN: 1 channel (timer RA, UART0) A/D converter         10-bit A/D converter: 1 circuit, 4 channels           Watchdog timer         T5 bits x 1 channel (with prescaler) Reset start selectable         Internal: 14 sources (J, K version) External: 4 sources, Software: 4 sources, Priority levels: 7 levels           Clock generation circuits         3 circuits         3 circuits         * XIN clock generation circuit (with on-chip feedback resistor) • XIN clock generation circuit (32 kHz) (N, D version) External: 4 sources, Software: 4 sources, Priority levels: 7 levels           Oscillation stop detection circuit         On-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz) (N, D version) • Kal-time clock (timer RE) (N, D version)           Voltage detection circuit         On-chip           Power-on reset circuit         On-chip           Voltage detection circuit         VCC = 3.0 to 5.5 V (f(XIN) = 10 MHz) (VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) (N, D version)     <	Functions	LED drive ports	I/O ports: 8 pins (N, D version)
Finer RB: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler)           Timer RC: 16 bits x 1 channel (Iput capture and output compare circuits) Timer RC: 16 bits x 1 channel (Iput capture and output compare match function (For J, K version, compare match function (Each synchronous serial interface           Clock synchronous serial interface         1 channel (IAC bus Interface(1) Clock synchronous serial I/O with chip select LIN module           LIN module         Hardware LIN: 1 channel (timer RA, UARTO)           A/D converter         10-bit A/D converter: 1 circuit, 4 channels           Watchdog timer         15 bits x 1 channel (with prescaler) Reset start selectable           Interrupts         Internal: 15 sources, No Version), Internal: 14 sources (J, K version) External: 4 sources, Software: 4 sources, Priority levels: 7 levels           Clock generation circuits         3 circuits           VN clock generation circuit (with on-chip feedback resistor)           • XIN clock generation circuit (32 kHz) (N, D version)           value detection function           Voltage detection circuit         On-chip           Power-on reset circuit         On-chip           Obscillation stop detection function         VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version) VCC = 3.0 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 10 MHz)           Current consumption (N, D version)         Typ. 10 mA (VC		Timers	Timer RA: 8 bits × 1 channel
Elect timer equipped with 8-bit prescaler)           Timer RC: 16 bits x 1 channel (Input capture and output compare match function (For J, K version, compare match function only.)           Serial interfaces         1 channel (UART0): Clock synchronous serial I/O, UART 1 channel (UART1): UART           Clock synchronous serial interface         1/2 chus Interface(1) (Clock synchronous serial I/O with chip select           LIN module         Hardware LIN: 1 channel (With Prescaler) (Clock synchronous serial I/O with chip select           LIN module         Hardware LIN: 1 channel (with prescaler) Reset start selectable           Interrupts         Internai: 15 sources (N, D version), Internal: 14 sources (J, K version) Natchdog timer           Interrupts         Internai: 5 sources (N, D version), Internal: 14 sources (J, K version) Externai: 4 sources, Software: 4 sources, Priority levels: 7 levels           Clock generation circuits         3 circuits           3 circuits         3 circuits           Volt dopt generation circuit (with on-chip feedback resistor) • On-chip oscillator higs speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz) (N, D version) • Real-time clock (timer RE) (N, D version)           Oscillation stop detection function         VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version) VCC = 3.0 to 5.5 V (f(XIN) = 10 MHz) (K version)           Voltage detection circuit         On-chip           Power-on reset circuit         On-chip to MA (VCC = 3.0 V, f(XIN) = 10			Timer RB: 8 bits × 1 channel
Finer RC: 16 bits × 1 channel (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function (Cor J, K version, compare match function only.)           Serial interfaces         1 channel (UART1): UART           Clock synchronous serial interface         1 channel (IPATU): UART           Clock synchronous serial interface         1 channel (IPATU): UART           LIN module         Hardware LIN: 1 channel (Imer RA, UART0)           A/D converter         10-bit A/D converter: 1 circuit, 4 channels           Watchdog timer         15 bits x 1 channel (With prescaler) Reset stat selectable           Interrupts         Internal: 15 sources (N, D version), Internal: 14 sources (J, K version) External: 4 sources, Software: 4 sources, Priority levels: 7 levels           Clock generation circuits         3 circuits           VAN clock generation circuit (with on-chip feedback resistor)           • XIN clock generation circuit (22 kHz) (N, D version)           • Reset -tirce clock generation circuit (22 kHz) (N, D version)           • Clock generation circuit         On-chip           • XIN clock coscillation stop detection function         On-chip           Voltage detection circuit         On-chip           Power-on reset circuit         On-chip           Power-on reset circuit         On-chip           Characteristics         Supply voltage         VCC = 3.0 to 5.5 V (f(XIN) = 10 MHz) VCC =			(Each timer equipped with 8-bit prescaler)
Imput capture and output compare circuits)           Timer RE: With real-time clock and compare match function (For J, K version, compare match function only.)           Serial interfaces         1 channel (UART0): Clock synchronous serial interface           Clock synchronous serial interface         1 channel (UART1): UART           Clock synchronous serial interface         1 channel (UCC synchronous serial I/O with chip select           LIN module         Hardware LIN: 1 channel (timer RA, UART0)           A/D converter         10-bit A/D converter: 1 circuit, 4 channels           Matchdog timer         15 bits x 1 channel (with prescaler) Reset start selectable           Interrupts         Internal: 15 sources (N, D version), Internal: 14 sources (J, K version)           Interrupts         Scircuits           ViN clock generation circuit (32 kHz) (N, D version)           Voltage detection circuit         ViN clock oscillation stop detection function           Voltage detection circuit         On-chip           Power-on reset circuit         On-chip           Power-on reset circuit         On-chip           Voltage detection circuit         On-chip           Power-on reset circuit         On-chip           Voltage detection         To-chip           Voltage detection         To-chip           Voltage detection circuit         On-chip			Timer RC: 16 bits × 1 channel
Imer RE: With real-time clock and compare match function           (For J, K version, compare match function only.)           Serial interfaces         1 channel (UART0): Clock synchronous serial I/O, UART           Clock synchronous serial interface         1 channel (UART1): UART           Clock synchronous serial interface         1 channel (UART1): UART           LIN module         Hardware LN: 1 channel (timer RA, UART0)           A/D converter         10-bit A/D converter: 1 circuit, 4 channels           Watchdog timer         15 bits × 1 channel (timer RA, UART0)           Reset start selectable         Internue: 15 sources (N, D version), Internal: 14 sources (J, K version)           External: 4 sources, Software: 4 sources, Priority levels: 7 levels         Clock generation circuit 3 circuits           Clock generation circuits         3 circuits         • XIN clock generation circuit (with on-chip feedback resistor)           • On-chip oscillator (high speed, oscillator has a frequency adjustment function function         • XIN clock generation circuit (3 kH2) (N, D version)           Oscillation stop detection         XIN clock socillation stop detection function           Voltage detection circuit         On-chip           Power-on reset circuit         On-chip           Power-on reset circuit         On-chip           Clock supply voltage         VCC = 3.0 to 5.5 V (f(XIN) = 10 MH2) (K version)			(Input capture and output compare circuits)
Serial interfaces         1 channel (UART0): Clock synchronous serial I/O, UART           1 channel (UART0): Clock synchronous serial I/O, UART         1 channel (UART0): Clock synchronous serial I/O, UART           Clock synchronous serial         1 channel           Interface         1 2C bus Interface(1)           Clock synchronous serial I/O with chip select         LIN module           Hardware LIN: 1 channel (timer RA, UART0)         AD converter           AD converter         10-bit AD converter: 1 circuit, 4 channels           Watchdog timer         15 bits x 1 channel (with prescaler)           Reset start selectable         Reset start selectable           Interrupts         Internal: 4 sources, Software: 4 sources, Priority levels: 7 levels           Clock generation circuits         3 circuits           Scillation stop detection function         XIN clock generation circuit (with on-chip feedback resistor)           • On-chip oscillator in as a frequency adjustment function function         XIN clock generation circuit (32 kHz) (N, D version)           Votage detection circuit         On-chip         No chy oscillator in as a frequency adjustment function           Votage detection circuit         On-chip         No chy oscillation stop detection function           Votage detection circuit         On-chip         No chy oscillator in the version)           VCC = 2.7 to 5.5 V (f(XIN) = 20 MHz) (other t			Timer RE: With real-time clock and compare match function
Serial interfaces         1 channel (UAR10): Clock synchronous serial I/O, UAR1           1 channel (UAR11): UART         1 channel (UAR11): UART           Clock synchronous serial interface         1 channel (UAR11): UART           LIN module         Hardware LIN: 1 channel (timer RA, UART0)           A/D converter         10-bit A/D converter: 1 circuit, 4 channels           Watchdog timer         15 bits x1 channel (with prescaler) Reset start selectable           Interrupts         Internal: 15 sources (N, D version), Internal: 14 sources (J, K version) External: 4 sources, Software: 4 sources, Priority levels: 7 levels           Clock generation circuits         3 circuits           3 circuits         3 circuits           • XIN clock generation circuit (with on-chip feedback resistor)           • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function           • XIN clock generation circuit (2 kHz) (N, D version)           • Real-time clock (timer RE) (N, D version)           • Voltage detection circuit         On-chip           Power-on reset circuit         On-chip           Power-on reset circuit         On-chip           Current consumption (N, D version)         Typ. 10 mA (VCC = 3.0 V, f(XIN) = 20 MHz) (other than K version)           VCC = 2.2 to 5.5 V (f(XIN) = 10 MHz)         Typ. 2.0 µ, A (VCC = 3.0 V, f(XIN) = 10 MHz)           Typ. 0.7		<b>a</b>	(For J, K version, compare match function only.)
Clock synchronous serial interface       1 channel (DART1): UART         LIN module       Hardware LIN: 1 channel (timer RA, UART0)         A/D converter       10-bit A/D converter: 1 circuit, 4 channels         Watchdog timer       15 bits x 1 channel (with prescaler) Reset start selectable         Interrupts       Internal: 15 sources (N, D version), Internal: 14 sources (J, K version) External: 4 sources, Software: 4 sources, Priority levels: 7 levels         Clock generation circuits       3 circuits         XIN clock generation circuit (with on-chip feedback resistor)         • On-chip oscillator has a frequency adjustment function         Valtage detection circuit       XIN clock generation circuit (32 kHz) (N, D version)         • Xell volck generation circuit (32 kHz) (N, D version)         • Notage detection circuit       On-chip         • On-chip       Power-on reset circuit         • Voltage detection circuit       On-chip         • Vocc = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version)         • VCC = 3.0 to 5.5 V (f(XIN) = 10 MHz)         • Vocc = 2.7 to 5.5 V (f(XIN) = 10 MHz)         • Vocc = 2.2 to 5.5 V (f(XIN) = 10 MHz)         • Vocc = 3.0 v, dittion = 10 MHz)         • Vocc = 2.7 to 5.5 V         • Current consumption       Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz)         • Vocc = 2.7 to 5.5 V         • Oparaming and erasu		Serial interfaces	1 channel (UART0): Clock synchronous serial I/O, UART
Clock synchronous serial interface         1 channel IPC bus Interface <sup>(1)</sup> Clock synchronous serial I/O with chip select           LIN module         Hardware LIN: 1 channel (timer RA, UART0)           A/D converter         10-bit A/D converter: 1 circuit, 4 channels           Watchdog timer         15 bits × 1 channel (with prescaler) Reset start selectable           Interrupts         Internal: 15 sources, 00 version), Internal: 14 sources, J, K version) External: 4 sources, Software: 4 sources, Priority levels: 7 levels           Clock generation circuits         3 circuits           VXIN clock generation circuit (with on-chip feedback resistor)           On-chip oscillator (high speed, low speed) High-speed on-chip oscillator nas a frequency adjustment function * XCIN clock generation circuit (32 kHz) (N, D version)           Oscillation stop detection function         XIN clock oscillation stop detection function function           VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version)         VCC = 3.0 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)           Characteristics         Typ. 70 mA (VCC = 3.0 V, stop mode)         Typ. 6 mA (VCC = 3.0 V, stop mode)           Flash Memory         Programming and erasure voltage         VCC = 2.7 to 5.5 V           Programming and erasure endurance         VCC = 2.7 to 5.5 V           Operating Ambient Temperature         -20 to 85°C (N version)           -20 to 85°C (N version)         -20 to 125°C (K version)(2)			1 channel (UART1): UART
Interface         I/2 bus Interface <sup>(1)</sup> Clock synchronous serial I/O with chip select           LIN module         Hardware LIN: 1 channel (timer RA, UARTO)           A/D converter         10-bit A/D converter: 1 circuit, 4 channels           Watchdog timer         15 bits × 1 channel (with prescaler)           Reset start selectable         Internal: 4 sources, Software: 4 sources, Priority levels: 7 levels           Clock generation circuits         3 circuits           VIN clock generation circuit (with on-chip feedback resistor)         • On-chip oscillator (high speed, low speed)           High-speed on-chip oscillator has a frequency adjustment function         • XCIN clock generation circuit (32 kHz) (N, D version)           Oscillation stop detection         XIN clock oscillation stop detection function           Voltage detection circuit         On-chip           Power-on reset circuit         On-chip           Power-on reset circuit         On-chip           Current consumption         Typ. 10 mA (VCC = 3.0 V, f(XIN) = 20 MHz) (K version)           VCC = 2.7 to 5.5 V (f(XIN) = 20 MHz)         Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz)           Typ. 0.7 µA (VCC = 3.0 V, f(XIN) = 10 MHz)         Typ. 0.7 µA (VCC = 3.0 V, stop mode)           Flash Memory         Programming and erasure voltage         VCC = 2.7 to 5.5 V           Programming and erasure endurance         100 tim		Clock synchronous serial	1 channel
Electrical         Supply voltage         VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version)           Vacce and the set of the set o		Interface	I <sup>2</sup> C bus Interface <sup>(1)</sup>
LIN module         Hardware Lin: 1 channel (timer RA, UAR10)           AD converter         10-bit A/D converter: 1 circuit, 4 channels           Watchdog timer         15 bits × 1 channel (with prescaler) Reset start selectable           Interrupts         Internal: 15 sources (N, D version), Internal: 14 sources (J, K version)           External: 4 sources, Software: 4 sources, Priority levels: 7 levels           Clock generation circuits         3 circuits           VIN clock generation circuit (with on-chip feedback resistor)           • On-chip oscillator has a frequency adjustment function function           Voltage detection circuit         On-chip oscillator has a frequency adjustment function           Voltage detection circuit         On-chip           Power-on reset circuit         On-chip           Power-on reset circuit         On-chip           VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version)           VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version)           VCC = 2.2 to 5.5 V (f(XIN) = 10 MHz)           (N, D version)         Typ. 10 mA (VCC = 3.0 V, f(XIN) = 20 MHz)           (N, D version)         Typ. 2.0 u, A(VCC = 3.0 V, f(XIN) = 10 MHz)           (N, D version)         Typ. 10 mA (VCC = 3.0 V, stop mode)           VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)         Typ. 0.7 µA (VCC = 3.0 V, stop mode)           Flash Memory         Programming and erasur			Clock synchronous serial I/O with chip select
A/D converter       10-bit A/D converter: 1 circuit, 4 channels         Watchdog timer       15 bits x 1 channel (with prescaler) Reset start selectable         Interrupts       Internal: 15 sources (N, D version), Internal: 14 sources (J, K version) External: 4 sources, Software: 4 sources, Priority levels: 7 levels         Clock generation circuits       3 circuits         • XIN clock generation circuit (with on-chip feedback resistor)         • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function         • XCIN clock generation circuit (32 kHz) (N, D version)         • Real-time clock (timer RE) (N, D version)         • Not clock generation circuit (32 kHz) (N, D version)         • Voltage detection circuit       On-chip         • Voltage detection circuit       On-chip         • Over-on reset circuit       On-chip         Power-on reset circuit       On-chip         Power-on reset circuit       On-chip         VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version)         VCC = 2.7 to 5.5 V (f(XIN) = 16 MHz)         V, D version)       Typ. 6 mA (VCC = 5.0 V, f(XIN) = 10 MHz)         VCC = 2.2 to 5.5 V (f(XIN) = 10 MHz)         Typ. 0.7 µA (VCC = 3.0 V, f(XIN) = 10 MHz)         Typ. 0.7 µA (VCC = 3.0 V, stop mode)         Flash Memory       Programming and erasure endurance       100 times </td <td></td> <td>LIN module</td> <td>Hardware LIN: 1 channel (timer RA, UARTO)</td>		LIN module	Hardware LIN: 1 channel (timer RA, UARTO)
Watchdog timer         15 bits × 1 channel (with prescaler) Reset start selectable           Interrupts         Interrupts         Internal: 15 sources (N, D version), Internal: 14 sources (J, K version) External: 4 sources, Software: 4 sources, Priority levels: 7 levels           Clock generation circuits         3 circuits         3 circuits           ViN clock generation circuit (with on-chip feedback resistor)         • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function           VXCIN clock generation circuit (32 kHz) (N, D version)         • Real-time clock (timer RE) (N, D version)           Oscillation stop detection function         On-chip           Voltage detection circuit         On-chip           Power-on reset circuit         On-chip           VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version) VCC = 3.0 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 10 MHz) Typ. 0 mA (VCC = 5.0 V, f(XIN) = 20 MHz) (N, D version)           Current consumption (N, D version)         Typ. 10 mA (VCC = 5.0 V, f(XIN) = 10 MHz) Typ. 2.0 μA (VCC = 3.0 V, f(XIN) = 10 MHz)           Typ. 0.7 μA (VCC = 3.0 V, stop mode)         VCC = 2.7 to 5.5 V           Flash Memory voltage         Programming and erasure endurance         100 times           Operating Ambient Temperature endurance         -20 to 85°C (N version) -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup>		A/D converter	10-bit A/D converter: 1 circuit, 4 channels
Interrupts         Internal: 15 sources (N, D version), Internal: 14 sources (J, K version), External: 4 sources, Software: 4 sources, Priority levels: 7 levels           Clock generation circuits         3 circuits         • XIN clock generation circuit (with on-chip feedback resistor)           • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function         • XIN clock generation circuit (32 kHz) (N, D version)           • Oscillation stop detection function         • XIN clock generation circuit (32 kHz) (N, D version)           • Voltage detection circuit         On-chip           Power-on reset circuit         On-chip           Power-on reset circuit         On-chip           Power-on reset circuit         On-chip           VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version) VCC = 2.2 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 50 MHz) (N, D version)           Current consumption (N, D version)         Typ. 6 mA (VCC = 3.0 V, f(XIN) = 20 MHz) Typ. 0.7 $\mu$ A (VCC = 3.0 V, stop mode)           Flash Memory         Programming and erasure endurance         100 times           Programming and erasure endurance         100 times           Operating Ambient Temperature         -20 to 85°C (N version) -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup>		Watchdog timer	15 bits × 1 channel (with prescaler)
Interrupts         Internat: 1s sources (N, D version), Internat: 14 sources (J, K version) External: 4 sources, Software: 4 sources, Priority levels: 7 levels           Clock generation circuits         3 circuits         3 circuits           VIN clock generation circuit (with on-chip feedback resistor)         • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz) (N, D version)           Oscillation stop detection function         XIN clock oscillation stop detection function           Voltage detection circuit         On-chip           Power-on reset circuit         On-chip           Power-on reset circuit         On-chip           Power-on reset circuit         On-chip           VCC = 3.0 to 5.5 V (f(XIN) = 10 MHz) (K version)           VCC = 2.2 to 5.5 V (f(XIN) = 10 MHz)           Current consumption (N, D version)         Typ. 10 mA (VCC = 5.0 V, f(XIN) = 10 MHz)           Typ. 0.7 μA (VCC = 3.0 V, stop mode)         Typ. 0.7 μA (VCC = 3.0 V, stop mode)           Flash Memory         Programming and erasure endurance         VCC = 2.7 to 5.5 V           Operating Ambient Temperature         -20 to 85°C (N version)           -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup>			Reset start selectable
External: 4 sources, Software: 4 sources, Priority levels: 7 levels         Clock generation circuits       3 circuits         VIN clock generation circuit (with on-chip feedback resistor)         • On-chip oscillator (high speed, low speed)         High-speed on-chip oscillator has a frequency adjustment function         • XCIN clock generation circuit (32 kHz) (N, D version)         • Real-time clock (timer RE) (N, D version)         • Real-time clock (timer RE) (N, D version)         Voltage detection circuit       On-chip         Power-on reset circuit       On-chip         Electrical       Supply voltage       VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version)         VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version)       VCC = 2.2 to 5.5 V (f(XIN) = 10 MHz)         VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (N, D version)       VCC = 2.2 to 5.5 V (f(XIN) = 20 MHz)         Current consumption       Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz)         (N, D version)       Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz)         Typ. 0 run (VCC = 3.0 V, f(XIN) = 20 MHz)       Typ. 0.7 µA (VCC = 3.0 V, f(XIN) = 20 MHz)         Flash Memory       Programming and erasure voltage       VCC = 2.7 to 5.5 V         Programming and erasure endurance       100 times       -20 to 85°C (N version)         -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> -40 to 85°C (D, J version) <sup>(2)</sup> ,		Interrupts	Internal: 15 sources (N, D version), Internal: 14 sources (J, K version)
Clock generation circuits       3 circuits         • XIN clock generation circuit (with on-chip feedback resistor)       • On-chip oscillator (high speed, low speed)         High-speed on-chip oscillator has a frequency adjustment function       • XCIN clock generation circuit (32 kHz) (N, D version)         • XCIN clock generation circuit (32 kHz) (N, D version)       • Real-time clock (timer RE) (N, D version)         • Voltage detection function       Voltage detection circuit       On-chip         Power-on reset circuit       On-chip       On-chip         Power-on reset circuit       On-chip       VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version)         VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version)       VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)         VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (N, D version)       VCC = 2.2 to 5.5 V (f(XIN) = 10 MHz)         VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (N, D version)       Typ. 6 mA (VCC = 3.0 V, f(XIN) = 20 MHz)         V, D version)       Typ. 10 mA (VCC = 3.0 V, f(XIN) = 10 MHz)         Typ. 0.7 µA (VCC = 3.0 V, f(XIN) = 10 MHz)       Typ. 2.0 µA (VCC = 3.0 V, stop mode)         Flash Memory       Programming and erasure voltage       VCC = 2.7 to 5.5 V         Programming and erasure endurance       -20 to 85°C (N version)       -20 to 85°C (N version)         -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> -20 to molded-plastic LSSOP       -20 to molded-plastic LS			External: 4 sources, Software: 4 sources, Priority levels: 7 levels
Proceeding and provided to the section of the sec (the section of the section of the section of		Clock generation circuits	3 CIFCUITS
Fight Speed, Now Speed,			<ul> <li>Any clock generation circuit (with on-chip reedback resistor)</li> <li>On obin oscillator (high anodal low anod)</li> </ul>
IndestructionNotice in the second problem of the second problem			<ul> <li>On-chip oscillator (high speed, low speed)</li> <li>High speed on chip oscillator has a frequency adjustment function</li> </ul>
Production concurrence       • Real-time clock (timer RE) (N, D version)         Oscillation stop detection function       XIN clock oscillation stop detection function         Voltage detection circuit       On-chip         Power-on reset circuit       On-chip         Electrical       Supply voltage       VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version)         VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version)       VCC = 3.0 to 5.5 V (f(XIN) = 10 MHz)         Characteristics       Current consumption       Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz)         (N, D version)       Typ. 10 mA (VCC = 3.0 V, f(XIN) = 10 MHz)         (N, D version)       Typ. 0.7 µA (VCC = 3.0 V, f(XIN) = 10 MHz)         Typ. 2.0 µA (VCC = 3.0 V, stop mode)       Typ. 0.7 µA (VCC = 3.0 V, stop mode)         Flash Memory       Programming and erasure voltage       VCC = 2.7 to 5.5 V         Programming and erasure endurance       100 times       100 times         Operating Ambient Temperature       -20 to 85°C (N version)       -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> Package       20-pin molded-plastic LSSOP       -40 to 125°C (K version) <sup>(2)</sup>			XCIN clock generation circuit (32 kHz) (N. D. version)
Oscillation stop detection function       XIN clock oscillation stop detection function         Voltage detection circuit Power-on reset circuit       On-chip         Electrical Characteristics       Supply voltage       VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version) VCC = 2.2 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (N, D version)         Current consumption (N, D version)       Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) VCC = 3.0 V, f(XIN) = 20 MHz) Typ. 0 mA (VCC = 3.0 V, f(XIN) = 20 MHz)         Flash Memory       Programming and erasure voltage       VCC = 2.2 to 5.5 V         Flash Memory       Programming and erasure endurance       VCC = 2.7 to 5.5 V         Operating Ambient Temperature       -20 to 85°C (N version) -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> Package       20-pin molded-plastic LSSOP			Real-time clock (timer RF) (N. D. version)
Initial of a bit of a		Oscillation stop detection	XIN clock oscillation stop detection function
Voltage detection circuit       On-chip         Power-on reset circuit       On-chip         Electrical Characteristics       Supply voltage       VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version) VCC = 2.2 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (N, D version)         Current consumption (N, D version)       Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 20 MHz) Typ. 2.0 $\mu$ A (VCC = 3.0 V, stop mode)         Flash Memory       Programming and erasure voltage       VCC = 2.7 to 5.5 V Typ. 0.7 $\mu$ A (VCC = 3.0 V, stop mode)         Flash Memory       Programming and erasure endurance       100 times         Operating Ambient Temperature       -20 to 85°C (N version) -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> Package       20-pin molded-plastic LSSOP		function	
Power-on reset circuitOn-chipElectrical CharacteristicsSupply voltageVCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (N, D version)Current consumption (N, D version)Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 $\mu$ A (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 0.7 $\mu$ A (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz) Typ. 0.7 $\mu$ A (VCC = 3.0 V, stop mode)Flash Memory Programming and erasure voltageVCC = 2.7 to 5.5 V Typ. 0.7 $\mu$ A (VCC = 3.0 V, stop mode)Flash Memory Programming and erasure endurance100 timesOperating Ambient Temperature-20 to 85°C (N version) -40 to 85°C (D, J version)(2), -40 to 125°C (K version)(2)Package20-pin molded-plastic LSSOP		Voltage detection circuit	On-chin
Electrical CharacteristicsSupply voltageVCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (N, D version)Current consumption (N, D version)Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 20 MHz) Typ. 2.0 µA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 µA (VCC = 3.0 V, stop mode)Flash MemoryProgramming and erasure voltageVCC = 2.7 to 5.5 V Typ. 0.7 µA (VCC = 3.0 V, stop mode)Flash MemoryProgramming and erasure voltageVCC = 2.7 to 5.5 VOperating Ambient Temperature-20 to 85°C (N version) -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> Package20-pin molded-plastic LSSOP		Power-on reset circuit	On-chip
CharacteristicsVCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (N, D version)Current consumption (N, D version)Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 10 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 $\mu$ A (VCC = 3.0 V, stop mode)Flash MemoryProgramming and erasure voltageVCC = 2.7 to 5.5 V Typ. 0.7 $\mu$ A (VCC = 3.0 V, stop mode)Flash MemoryProgramming and erasure enduranceVCC = 2.7 to 5.5 VOperating Ambient Temperature-20 to 85°C (N version) -40 to 85°C (D, J version)^{(2)}, -40 to 125°C (K version)^{(2)}Package20-pin molded-plastic LSSOP	Electrical	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version)
VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (N, D version)Current consumption (N, D version)Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 $\mu$ A (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz) Typ. 0.7 $\mu$ A (VCC = 3.0 V, stop mode)Flash MemoryProgramming and erasure voltageVCC = 2.7 to 5.5 VProgramming and erasure endurance100 timesOperating Ambient Temperature-20 to 85°C (N version) -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> Package20-pin molded-plastic LSSOP	Characteristics		VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version)
VCC = 2.2 to 5.5 V ( $f(XIN) = 5 MHz$ ) (N, D version)Current consumption (N, D version)Typ. 10 mA (VCC = 5.0 V, $f(XIN) = 20 MHz$ ) Typ. 6 mA (VCC = 3.0 V, $f(XIN) = 10 MHz$ ) Typ. 2.0 $\mu$ A (VCC = 3.0 V, wait mode ( $f(XCIN) = 32 \text{ kHz}$ ) Typ. 0.7 $\mu$ A (VCC = 3.0 V, stop mode)Flash MemoryProgramming and erasure voltageVCC = 2.7 to 5.5 VProgramming and erasure endurance100 timesOperating Ambient Temperature-20 to 85°C (N version) -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> Package20-pin molded-plastic LSSOP			VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
Current consumption (N, D version)Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 $\mu$ A (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz) Typ. 0.7 $\mu$ A (VCC = 3.0 V, stop mode)Flash MemoryProgramming and erasure voltageVCC = 2.7 to 5.5 VProgramming and erasure endurance100 timesOperating Ambient Temperature-20 to 85°C (N version) -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> Package20-pin molded-plastic LSSOP			VCC = 2.2 to 5.5 V $(f(XIN) = 5 \text{ MHz})$ (N, D version)
$ \begin{array}{c} (N, D \text{ version}) & Typ. 6 \text{ mA} (VCC = 3.0 \text{ V}, f(XIN) = 10 \text{ MHz}) \\ Typ. 2.0 \ \muA (VCC = 3.0 \text{ V}, \text{ wait mode} (f(XCIN) = 32 \text{ kHz}) \\ Typ. 0.7 \ \muA (VCC = 3.0 \text{ V}, \text{ stop mode}) \\ \hline Flash \ Memory & \underbrace{Programming \text{ and erasure} \\ voltage & VCC = 2.7 \text{ to } 5.5 \text{ V} \\ \hline Votage & VCC = 2.7 \text{ to } 5.5 \text{ V} \\ \hline Programming \text{ and erasure} \\ endurance & 100 \text{ times} \\ \hline Operating \ Ambient \ Temperature & \underbrace{-20 \text{ to } 85^\circ \mathbb{C} (N \text{ version}) \\ -40 \text{ to } 85^\circ \mathbb{C} (D, \text{ J} \text{ version})^{(2)}, -40 \text{ to } 125^\circ \mathbb{C} (K \text{ version})^{(2)} \\ \hline Package & 20-pin molded-plastic \ LSSOP \\ \hline \end{array} $		Current consumption	Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz)
Typ. 2.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz) Typ. 0.7 μA (VCC = 3.0 V, stop mode)         Flash Memory       Programming and erasure voltage       VCC = 2.7 to 5.5 V         Programming and erasure endurance       100 times         Operating Ambient Temperature       -20 to 85°C (N version)         -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> Package       20-pin molded-plastic LSSOP		(N, D version)	Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz)
Typ. 0.7 μA (VCC = 3.0 V, stop mode)       Flash Memory     Programming and erasure voltage     VCC = 2.7 to 5.5 V       Programming and erasure endurance     100 times       Operating Ambient Temperature     -20 to 85°C (N version)       -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> Package     20-pin molded-plastic LSSOP			Typ. 2.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)
Flash Memory       Programming and erasure voltage       VCC = 2.7 to 5.5 V         Programming and erasure endurance       100 times         Operating Ambient Temperature       -20 to 85°C (N version)         -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> Package       20-pin molded-plastic LSSOP			Typ. 0.7 μA (VCC = 3.0 V, stop mode)
voltage       Programming and erasure endurance     100 times       Operating Ambient Temperature     -20 to 85°C (N version)       -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> Package     20-pin molded-plastic LSSOP	Flash Memory	Programming and erasure	VCC = 2.7 to 5.5 V
Programming and erasure endurance       100 times         Operating Ambient Temperature       -20 to 85°C (N version)         -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> Package       20-pin molded-plastic LSSOP		voltage	
endurance       Operating Ambient Temperature     -20 to 85°C (N version)       -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> Package     20-pin molded-plastic LSSOP		Programming and erasure	100 times
Operating Ambient Temperature       -20 to 85°C (N version)         -40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> Package       20-pin molded-plastic LSSOP		endurance	
-40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup> Package     20-pin molded-plastic LSSOP	Operating Ambie	nt Temperature	-20 to 85°C (N version)
Package 20-pin molded-plastic LSSOP			-40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup>
	Package		20-pin molded-plastic LSSOP

Table 1.1	Functions and Sr	pecifications for	R8C/28 Group
	i unctions and op		100/20 010up

NOTES:

1. I<sup>2</sup>C bus is a trademark of Koninklijke Philips Electronics N. V.

2. Specify the D, K version if D, K version functions are to be used.



#### 1.6 Pin Functions

Table 1.5 lists Pin Functions.

#### Table 1.5Pin Functions

Туре	Symbol	I/O Type	Description
Power supply input	VCC, VSS	I	Apply 2.2 to 5.5 V (J, K version are 2.7 to 5.5 V) to the VCC
Analog power	AVCC AVSS	1	Power supply for the A/D converter
supply input			Connect a capacitor between AVCC and AVSS.
Reset input	RESET	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between
XIN clock output	XOUT	0	the XIN and XOUT pins. To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XCIN clock input (N, D version)	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT
XCIN clock output (N, D version)	XCOUT	0	pins. To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
INT interrupt input	INTO, INT1, INT3	I	INT interrupt input pins
Key input interrupt	KI0 to KI3	I	Key input interrupt input pins
Timer RA	TRAO	0	Timer RA output pin
	TRAIO	I/O	Timer RA I/O pin
Timer RB	TRBO	0	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Sharing output-compare output / input-capture input / PWM / PWM2 output pins
Serial interface	CLK0	I/O	Clock I/O pin
	RXD0, RXD1	I	Receive data input pin
	TXD0, TXD1	0	Transmit data output pin
I <sup>2</sup> C bus interface	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
Clock synchronous	SSI	I/O	Data I/O pin
serial I/O with chip	SCS	I/O	Chip-select signal I/O pin
Select	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN8 to AN11	I	Analog input pins to A/D converter
I/O port	P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not
			by a program. P1_0 to P1_7 also function as LED drive ports (N, D version).
Input port	P4_2, P4_6, P4_7	I	Input-only ports

I: Input O: Output I/O:

I/O: Input and output



				I/O Pin Functions for of Peripheral Modules				
Pin Number	Control Pin	Port	Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I <sup>2</sup> C bus Interface	A/D Converter
1		P3_5		TRCIOD		SSCK	SCL	
2		P3_7		TRAO	RXD1/(TXD1) <sup>(1)</sup>	SSO		
3	RESET							
4	XOUT/ XCOUT <sup>(2)</sup>	P4_7						
5	VSS/AVSS							
6	XIN/XCIN <sup>(2)</sup>	P4_6						
7	VCC/AVCC							
8	MODE							
9		P4_5	INT0		(RXD1) <sup>(1)</sup>			
10		P1_7	INT1	TRAIO				
11		P1_6			CLK0	(SSI) <sup>(1)</sup>		
12		P1_5	(INT1) <sup>(1)</sup>	(TRAIO) <sup>(1)</sup>	RXD0			
13		P1_4			TXD0			
14		P1_3	KI3	TRBO				AN11
15		P1_2	KI2	TRCIOB				AN10
16	VRFF	P4_2						
17		P1_1	KI1	TRCIOA/ TRCTRG				AN9
18		P1_0	KI0					AN8
19		P3_3	INT3	TRCCLK		SSI		
20		P3_4		TRCIOC		SCS	SDA	

 Table 1.6
 Pin Name Information by Pin Number

NOTES:

1. This can be assigned to the pin in parentheses by a program.

2. XCIN, XCOUT can be used only for N or D version.



### 3.2 R8C/29 Group

Figure 3.2 is a Memory Map of R8C/29 Group. The R8C/29 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.





Address	Register	Symbol	After reset
0080h			
0081h			
0082h			
0083h			
00846			
000411			
00850			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
000Eh			
000Eh			
008FN			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h		İ	
0096h		1	
0097h			
00986		ł	
0000h			
009911			
009An			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UARTO Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	UOTB	XXh
00A3h		00.5	XXh
00/(0h	UAPTO Transmit/Passiva Control Pagistar 0	11000	00001000b
00A411	UARTO Transmit/Receive Control Register 0	0000	000010000
UUA5h	UARTO Transmit/Receive Control Register 1	0001	d01000010b
00A6h	UARI0 Receive Buffer Register	UORB	XXh
00A7h			XXh
00A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
00A9h	UART1 Bit Rate Register	U1BRG	XXh
00AAh	UART1 Transmit Buffer Register	U1TB	XXh
00ABh			XXh
00ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
004 Dh	UART1 Transmit/Receive Control Register 1	U1C1	0000010b
	UIADT1 Deceive Buffer Degister		XXP
	UNNEE RECEIVE DUILEE REGISTER	UIRD	
UUAFn			77U
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h		İ	
00B6h		1	
00B7h			1
00Bah	SS Control Paginter H / IIC hup Control Paginter (2)		00b
UUB9h	SS Control Register L / IIC bus Control Register 2 <sup>(2)</sup>	SSCRL / ICCR2	011111010
00BAh	SS Mode Register / IIC bus Mode Register <sup>(2)</sup>	SSMR / ICMR	00011000b
00BBh	SS Enable Register / IIC bus Interrupt Enable Register <sup>(2)</sup>	SSER / ICIER	00h
00BCh	SS Status Register / IIC bus Status Register <sup>(2)</sup>	SSSR / ICSR	00h / 0000X000b
00BDh	SS Mode Register 2 / Slave Address Register <sup>(2)</sup>	SSMR2/SAR	00h
OOPEN	CO WOULD Register 2 / Slave Audiess Register		CCh
UUBEN	55 Transmit Data Register / IIC bus Transmit Data Register <sup>(2)</sup>	SSIDK/ICDKI	
00BFh	SS Receive Data Register / IIC bus Receive Data Register <sup>(2)</sup>	SSRDR / ICDRR	FFh
X. Undefined			

#### SFR Information (3)<sup>(1)</sup> Table 4.3

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

RENESAS

Symbol	Boromotor	Conditions		Linit			
Symbol	Falameter	Conditions	Min.	Тур.	Max.		
-	Program/erase endurance <sup>(2)</sup>	R8C/28 Group	100 <sup>(3)</sup>	-	-	times	
		R8C/29 Group	1,000 <sup>(3)</sup>	-	-	times	
-	Byte program time		-	50	400	μs	
-	Block erase time		-	0.4	9	S	
td(SR-SUS)	Time delay from suspend request until		-	-	97 + CPU clock	μs	
	suspend				× 6 cycles		
-	Interval from erase start/restart until		650	-	-	μs	
	following suspend request						
-	Interval from program start/restart until		0	-	-	ns	
	following suspend request						
-	Time from suspend until program/erase		-	-	3 + CPU clock	μs	
	restart				× 4 cycles		
-	Program, erase voltage		2.7	-	5.5	V	
-	Read voltage		2.2	-	5.5	V	
-	Program, erase temperature		0	-	60	°C	
-	Data hold time <sup>(7)</sup>	Ambient temperature = 55°C	20	-	-	year	

Table 5.4	Flash Memory (Program ROM) Electrical Characteristics
-----------	---

NOTES:

1. Vcc = 2.7 to 5.5 V at Topr = 0 to  $60^{\circ}$ C, unless otherwise specified.

2. Definition of programming/erasure endurance

The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).

4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.

5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.

- 6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 7. The data hold time includes time that the power supply is off or the clock is not supplied.

Symbol	Parameter	Condition		Llnit		
Symbol	Tarameter	Condition	Min.	Тур.	Max.	Onit
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	$\label{eq:VCC} \begin{array}{l} VCC = 4.75 \text{ to } 5.25 \text{ V} \\ 0^\circ C \leq Topr \leq 60^\circ C^{(2)} \end{array}$	39.2	40	40.8	MHz
		$\label{eq:Vcc} \begin{array}{l} \mbox{Vcc} = 3.0 \mbox{ to } 5.5 \mbox{ V} \\ \mbox{-}20^{\circ}\mbox{C} \leq \mbox{T}_{opr} \leq 85^{\circ}\mbox{C}^{(2)} \end{array}$	38.8	40	41.2	MHz
		$\label{eq:VCC} \begin{array}{l} \mbox{Vcc} = 3.0 \mbox{ to } 5.5 \mbox{ V} \\ \mbox{-40}^{\circ}\mbox{C} \leq \mbox{Topr} \leq 85^{\circ}\mbox{C}^{(2)} \end{array}$	38.4	40	41.6	MHz
		$\label{eq:Vcc} \begin{array}{l} \mbox{Vcc} = 2.7 \mbox{ to } 5.5 \mbox{ V} \\ \mbox{-}20^{\circ}\mbox{C} \leq \mbox{Topr} \leq 85^{\circ}\mbox{C}^{(2)} \end{array}$	38	40	42	MHz
		$\label{eq:Vcc} \begin{array}{l} \text{Vcc} = 2.7 \text{ to } 5.5 \text{ V} \\ \text{-40}^\circ\text{C} \leq \text{T}_{opr} \leq 85^\circ\text{C}^{(2)} \end{array}$	37.6	40	42.4	MHz
		$\label{eq:Vcc} \begin{array}{l} \mbox{Vcc} = 2.2 \mbox{ to } 5.5 \mbox{ V} \\ \mbox{-}20^\circ \mbox{C} \leq \mbox{Topr} \leq 85^\circ \mbox{C}^{(3)} \end{array}$	35.2	40	44.8	MHz
		$\label{eq:Vcc} \begin{array}{l} \mbox{Vcc} = 2.2 \mbox{ to } 5.5 \mbox{ V} \\ \mbox{-40}^\circ \mbox{C} \leq \mbox{Topr} \leq 85^\circ \mbox{C}^{(3)} \end{array}$	34	40	46	MHz
		$\label{eq:VCC} \begin{array}{l} Vcc = 5.0 \ V \pm 10\% \\ -20^{\circ}C \leq T_{opr} \leq 85^{\circ}C^{(2)} \end{array}$	38.8	40	40.8	MHz
		$\label{eq:VC} \begin{array}{l} \mbox{Vcc} = 5.0 \mbox{ V} \pm 10\% \\ \mbox{-40}^\circ \mbox{C} \leq \mbox{Topr} \leq 85^\circ \mbox{C}^{(2)} \end{array}$	38.4	40	40.8	MHz
	High-speed on-chip oscillator frequency when	$VCC = 5.0 V$ , $Topr = 25^{\circ}C$	-	36.864	-	MHz
	correction value in FRA7 register is written to FRA1 register <sup>(4)</sup>	Vcc = 3.0 to 5.5 V -20°C ≤ Topr ≤ 85°C	-3%	_	3%	%
-	Value in FRA1 register after reset		08h <sup>(3)</sup>	-	F7h <sup>(3)</sup>	-
-	Oscillation frequency adjustment unit of high- speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	-	+0.3	—	MHz
-	Oscillation stability time		-	10	100	μs
_	Self power consumption at oscillation	$VCC = 5.0 V$ , $Topr = 25^{\circ}C$	_	400	-	μA

Table 5.10	High-speed On-Chip Oscillator Circuit Electrical Characteristics
------------	--

NOTES:

1. Vcc = 2.2 to 5.5 V, Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

2. These standard values show when the FRA1 register value after reset is assumed.

3. These standard values show when the corrected value of the FRA6 register is written to the FRA1 register.

4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

#### Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition		Standard		Llpit
Symbol	Falanetei	Condition	Min.	Тур.	Max.	Unit
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
-	Oscillation stability time		-	10	100	μS
-	Self power consumption at oscillation	VCC = $5.0 \text{ V}$ , Topr = $25^{\circ}\text{C}$	-	15	-	μA

NOTE:

1. Vcc = 2.2 to 5.5 V, Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

#### Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	:	Linit		
Symbol	Falanetei	Condition	Min.	Тур.	Max.	Offic
td(P-R)	Time for internal power supply stabilization during		1	-	2000	μS
	power-on <sup>(2)</sup>					
td(R-S)	STOP exit time <sup>(3)</sup>		-	-	150	μS

NOTES:

1. The measurement condition is Vcc = 2.2 to 5.5 V and  $T_{opr} = 25^{\circ}C$ .

2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.





Table 5.20 Serial Interfac
----------------------------

Symbol	Parameter	Stan	Lloit	
Symbol		Min.	Max.	Unit
tc(CK)	CLK0 input cycle time	200	-	ns
tw(ckh)	CLK0 input "H" width	100	-	ns
tW(CKL)	CLK0 input "L" width	100	-	ns
td(C-Q)	TXDi output delay time	-	50	ns
th(C-Q)	TXDi hold time	0	-	ns
tsu(D-C)	RXDi input setup time	50	-	ns
th(C-D)	RXDi input hold time	90	_	ns

i = 0 or 1



Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V

#### Table 5.21 External Interrupt INTi (i = 0, 1, 3) Input

Symbol	Symbol Parameter	Stan	Lloit	
Symbol		Min.	Max.	Offic
tw(INH)	INTi input "H" width	250 <sup>(1)</sup>	-	ns
tw(INL)	INTi input "L" width	250(2)	-	ns

NOTES:

1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.



Figure 5.11 External Interrupt INTi Input Timing Diagram when Vcc = 5 V

Symbol	Parameter		Condition		Standard			Unit
Symbol	i aia	Ineter	Condit		Min.	Тур.	Max.	Onit
Vон	Output "H" voltage	Except P1_0 to P1_7, XOUT	Iон = -1 mA		Vcc - 0.5	-	Vcc	V
		P1_0 to P1_7	Drive capacity HIGH	Іон = -5 mA	Vcc - 0.5	-	Vcc	V
			Drive capacity LOW	Iон = -1 mA	Vcc - 0.5	-	Vcc	V
		XOUT	Drive capacity HIGH	Iон = -0.1 mA	Vcc - 0.5	-	Vcc	V
			Drive capacity LOW	Іон = -50 μА	Vcc - 0.5	-	Vcc	V
Vol	Output "L" voltage	Except P1_0 to P1_7, XOUT	IOL = 1 mA		_	_	0.5	V
		P1_0 to P1_7	Drive capacity HIGH	lo∟ = 5 mA	-	-	0.5	V
			Drive capacity LOW	lo∟ = 1 mA	-	-	0.5	V
		XOUT	Drive capacity HIGH	lo∟ = 0.1 mA	-	-	0.5	V
			Drive capacity LOW	IoL = 50 μA	_	_	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO			0.1	0.3	_	V
		RESET			0.1	0.4	-	V
Ін	Input "H" current		VI = 3 V, Vcc = 3V	/	-	-	4.0	μA
lı∟	Input "L" current		VI = 0 V, Vcc = 3V	/	-	-	-4.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 3V	/	66	160	500	kΩ
RfXIN	Feedback resistance	XIN			-	3.0	-	MΩ
Rfxcin	Feedback resistance	XCIN			_	18	-	MΩ
Vram	RAM hold voltage		During stop mode		1.8	—	—	V

NOTE:

1. Vcc = 2.7 to 3.3 V at Topr = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

#### Timing requirements (Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = 25°C) [Vcc = 3 V]

#### Table 5.24 XIN Input, XCIN Input

Symbol	Paramatar	Stan	Lloit	
Symbol			Max.	Unit
tc(XIN)	XIN input cycle time	100	-	ns
twh(xin)	XIN input "H" width	40	-	ns
twl(XIN)	XIN input "L" width	40	-	ns
tc(XCIN)	XCIN input cycle time	14	-	μS
twh(xcin)	XCIN input "H" width	7	-	μS
twl(xcin)	XCIN input "L" width	7	-	μS



### Figure 5.12 XIN Input and XCIN Input Timing Diagram when Vcc = 3 V

#### Table 5.25 TRAIO Input

Symbol	Symbol Parameter	Stan	Lloit	
Symbol		Min.	Max.	Onit
tc(TRAIO)	TRAIO input cycle time	300	-	ns
twh(traio)	TRAIO input "H" width	120	-	ns
twl(traio)	TRAIO input "L" width	120	-	ns



#### Figure 5.13 TRAIO Input Timing Diagram when Vcc = 3 V

# Table 5.29Electrical Characteristics (6) [Vcc = 2.2 V]<br/>(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit	
Symbol	i alametei		Condition	Min.	Тур.	Max.	Onit
Icc	Power supply current (Vcc = 2.2 to 2.7 V) Single-chip mode,	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	3.5	-	mA
	other pins are Vss	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	1.5	-	mA
		High-speed on-chip oscillator	XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	_	3.5	-	mA
		XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	1.5	-	mA	
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	-	100	230	μΑ
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	_	100	230	μΑ
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	-	25	_	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	22	60	μΑ
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	20	55	μΑ
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	3.0		μΑ
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	1.8	_	μΑ
		Stop mode	XIN clock off, $T_{opr} = 25^{\circ}C$ High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	0.7	3.0	μA
			XIN clock off, $T_{opr} = 85^{\circ}C$ High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	1.1	-	μA



#### Timing requirements (Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C) [Vcc = 2.2 V]

#### Table 5.30 XIN Input, XCIN Input

Symbol	Baramatar	Stan	Linit	
Symbol			Max.	Unit
tc(XIN)	XIN input cycle time	200	-	ns
twh(xin)	XIN input "H" width	90	-	ns
twl(XIN)	XIN input "L" width	90	-	ns
tc(XCIN)	XCIN input cycle time	14	-	μS
twh(xcin)	XCIN input "H" width	7	-	μS
twl(xcin)	XCIN input "L" width	7	-	μS



### Figure 5.16 XIN Input and XCIN Input Timing Diagram when Vcc = 2.2 V

#### Table 5.31 TRAIO Input

Symbol	Parameter	Stan	Linit	
Symbol	Falameter	Min.	Max.	Unit
tc(TRAIO)	TRAIO input cycle time	500	-	ns
twh(traio)	TRAIO input "H" width	200	-	ns
twl(traio)	TRAIO input "L" width	200	-	ns



#### Figure 5.17 TRAIO Input Timing Diagram when Vcc = 2.2 V

Table 5.32 Serial Interface
-----------------------------

Symbol	Parameter	Stan	Lloit	
Symbol			Max.	Ofine
tc(CK)	CLK0 input cycle time	800	-	ns
tw(ckh)	CLK0 input "H" width	400	-	ns
tW(CKL)	CLK0 input "L" width	400	-	ns
td(C-Q)	TXDi output delay time	-	200	ns
th(C-Q)	TXDi hold time	0	-	ns
tsu(D-C)	RXDi input setup time	150	-	ns
th(C-D)	RXDi input hold time	90	-	ns

i = 0 or 1





#### Table 5.33 External Interrupt INTi (i = 0, 1, 3) Input

Symbol	Parameter		Standard	
	Falameter	Min.	Max.	Unit
tw(INH)	INTi input "H" width	1000(1)	-	ns
tw(INL)	INTi input "L" width	1000 <sup>(2)</sup>	-	ns

NOTES:

1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.



Figure 5.19 External Interrupt INTi Input Timing Diagram when VCC = 2.2 V



Figure 5.24 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

RENESAS



Figure 5.25 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Symbol	Paramotor		Condition		Standard			Llpit
Symbol	Fai	ameter	Condition		Min.	Тур.	Max.	Unit
Vон	Output "H" voltage	Except XOUT	Iон = -5 mA		Vcc - 2.0	-	Vcc	V
			Іон = -200 μА		Vcc - 0.3	-	Vcc	V
		XOUT	Drive capacity HIGH	Iон = -1 mA	Vcc - 2.0	-	Vcc	V
			Drive capacity LOW	Іон = -500 μА	Vcc - 2.0	-	Vcc	V
Vol	Output "L" voltage	Except XOUT	IoL = 5 mA		-	-	2.0	V
			Ιοι = 200 μΑ		-	-	0.45	V
		XOUT	Drive capacity HIGH	IoL = 1 mA	-	-	2.0	V
			Drive capacity LOW	IoL = 500 μA	-	-	2.0	V
Vt+-Vt-	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO			0.1	0.5	_	V
		RESET			0.1	1.0	-	V
Ін	Input "H" current		VI = 5 V, Vcc = 5V		-	I	5.0	μA
lı∟	Input "L" current		VI = 0 V, Vcc = 5V		-	-	-5.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5V		30	50	167	kΩ
Rfxin	Feedback resistance	XIN			-	1.0	-	MΩ
VRAM	RAM hold voltage		During stop mode		2.0	_	-	V

### Table 5.47 Electrical Characteristics (1) [Vcc = 5 V]

NOTE:

1. Vcc = 4.2 to 5.5 V at  $T_{opr} = -40$  to  $85^{\circ}C$  (J version) / -40 to  $125^{\circ}C$  (K version), f(XIN) = 20 MHz, unless otherwise specified.

#### Timing Requirements (Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

#### Table 5.49 XIN Input

Symbol	Baramatar		Standard	
	Falameter	Min.	Min. Max.	Unit
tc(XIN)	XIN input cycle time	50	-	ns
twh(xin)	XIN input "H" width	25	-	ns
twl(XIN)	XIN input "L" width	25	-	ns



Figure 5.27 XIN Input Timing Diagram when Vcc = 5 V

#### Table 5.50 TRAIO Input

Symbol	Parameter	Standard		Linit
	Falantelei	Min. Max.		Onit
tc(TRAIO)	TRAIO input cycle time	100	-	ns
twh(traio)	TRAIO input "H" width	40	-	ns
twl(traio)	TRAIO input "L" width	40	-	ns



Figure 5.28 TRAIO Input Timing Diagram when Vcc = 5 V

## **REVISION HISTORY**

# R8C/28 Group, R8C/29 Group Datasheet

Rev.	Date		Description
		Page	Summary
0.10	Nov 14, 2005	-	First Edition issued
0.30	Feb 28, 2006	all pages	"J, K version" added
		1	1.1 Applications revised
		2	Table 1.1 Functions and Specifications for R8C/28 Group revised
		3	Table 1.2 Functions and Specifications for R8C/29 Group revised
		4	Figure 1.1 Block Diagram; NOTE3 added
		5	Table 1.3 Product Information for R8C/28 Group and Figure 1.2 Type Number, Memory Size, and Package of R8C/28 Group revised
		6	Table 1.4 Product Information for R8C/29 Group and Figure 1.3 Type Number, Memory Size, and Package of R8C/29 Group revised
		7	Figure 1.4 Pin Assignments (Top View); NOTE3 added
		8	Table 1.5 Pin Functions revised
		9	Table 1.6 Pin Name Information by Pin Number; "XOUT" → "XOUT/XCOUT", "XIN" → "XIN/XCIN" revised and NOTE2 added
		13	Figure 3.1 Memory Map of R8C/28 Group; "R5F21284JSP, R5F21284KSP" added
		14	Figure 3.2 Memory Map of R8C/29 Group; "R5F21294JSP, R5F21294KSP" added
		15	Table 4.1 SFR Information (1); NOTE6 added
		18	Table 4.4 SFR Information (4); 00FEh: "DRR" → "P1DRR" symbol name revised
		22 to 66	5. Electrical Characteristics added
0.40	Mar 29, 2006	2	Table 1.1 Functions and Specifications for R8C/28 Group revised
		3	Table 1.2 Functions and Specifications for R8C/29 Group revised
		15	Table 4.1 SFR Information (1); - 0032h, 0036h, 0038h revised
			- NOTES 2 to 6 revised and NOTES 7 to 8 added
0.50		19	Table 4.5 SFR Information (5); NOTE2 added
0.50	Apr 27, 2006	18	Table 4.4; 00FDh: revised
1.00	NI 00 0000	46	Table 5.35; System clock Conditions: revised
1.00	Nov 08, 2006	All pages	"PRELIMINARY" deleted
		1	1 "J and κ versions are under developmentnotice." added
		2	Table 1.1 revised
		3	
		4	Table 1.2 revised
		5	
		6	Table 1.4 revised