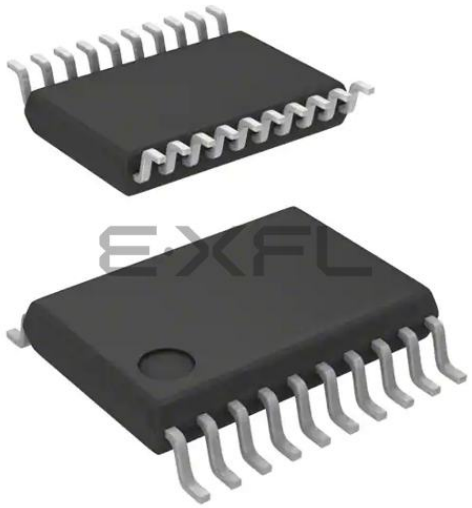
# Renesas Electronics America Inc - R5F21286KSP#W4 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 16MHz |
| Connectivity | I²C, LINbus, SIO, SSU, UART/USART |
| Peripherals | LED, POR, Voltage Detect, WDT |
| Number of I/O | 13 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1.5K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-LSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 20-LSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21286ksp-w4 |

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**Table 1.4 Product Information for R8C/29 Group Current of Sep. 2008**

| Type No. | ROM Capacity | | RAM Capacity | Package Type | Remarks | |
|---|---|---|---|---|---|---|
| | Program ROM | Data flash | | | | |
| R5F21292SNSP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | PLSP0020JB-A | N version | |
| R5F21294SNSP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLSP0020JB-A | | |
| R5F21292SDSP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | PLSP0020JB-A | D version | |
| R5F21294SDSP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLSP0020JB-A | | |
| R5F21294JSP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLSP0020JB-A | J version | |
| R5F21296JSP | 32 Kbytes | 1 Kbyte × 2 | 1.5 Kbyte | PLSP0020JB-A | | |
| R5F21294KSP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLSP0020JB-A | K version | |
| R5F21296KSP | 32 Kbytes | 1 Kbyte × 2 | 1.5 Kbyte | PLSP0020JB-A | | |
| R5F21292SNXXXSP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | PLSP0020JB-A | N version | Factory programming product(1) |
| R5F21294SNXXXSP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLSP0020JB-A | | |
| R5F21292SDXXXSP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | PLSP0020JB-A | D version | |
| R5F21294SDXXXSP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLSP0020JB-A | | |
| R5F21294JXXXSP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLSP0020JB-A | J version | |
| R5F21296JXXXSP | 32 Kbytes | 1 Kbyte × 2 | 1.5 Kbyte | PLSP0020JB-A | | |
| R5F21294KXXXSP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLSP0020JB-A | K version | |
| R5F21296KXXXSP | 32 Kbytes | 1 Kbyte × 2 | 1.5 Kbyte | PLSP0020JB-A | | |

NOTE:
1. The user ROM is programmed before shipment.

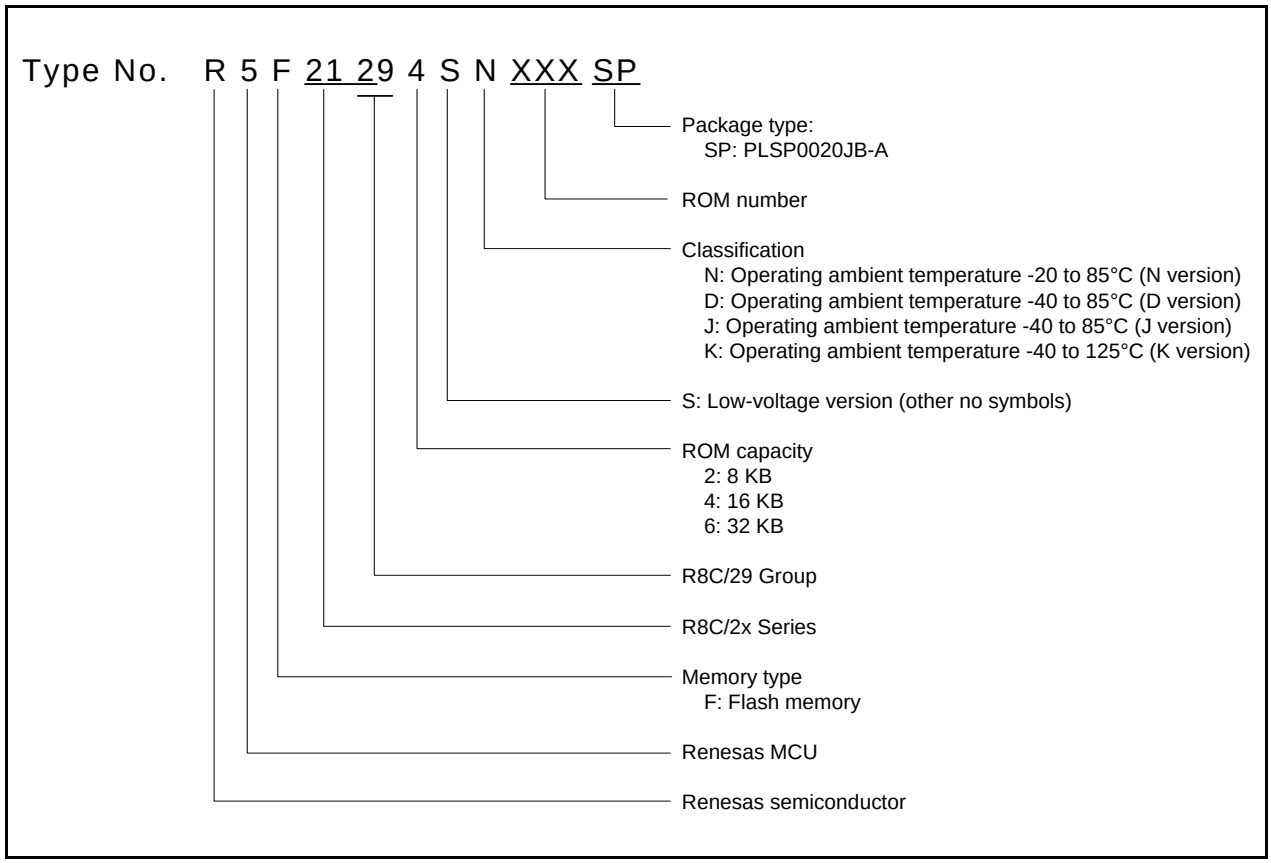
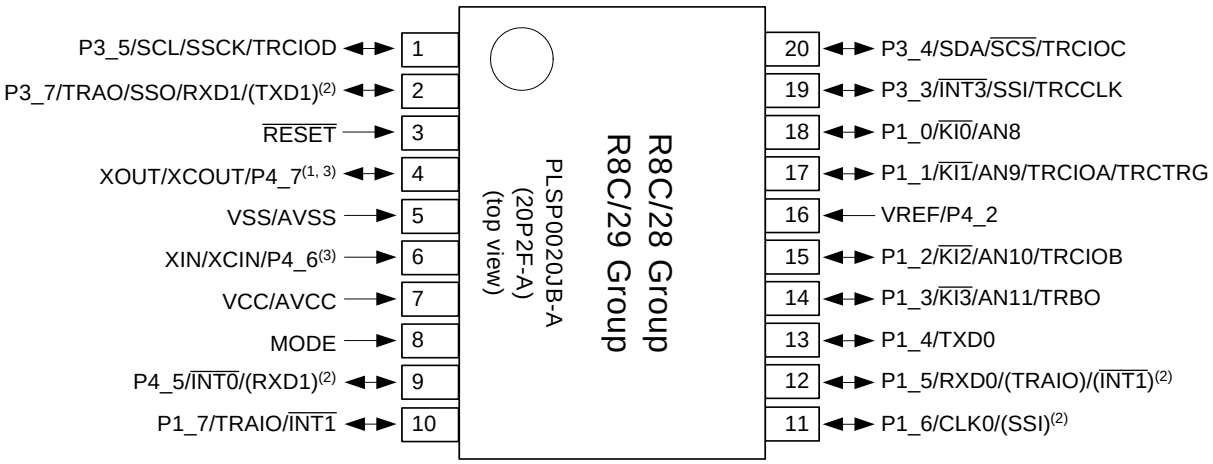



**Figure 1.3 Type Number, Memory Size, and Package of R8C/29 Group**

## 1.5 Pin Assignments

Figure 1.4 shows Pin Assignments (Top View).

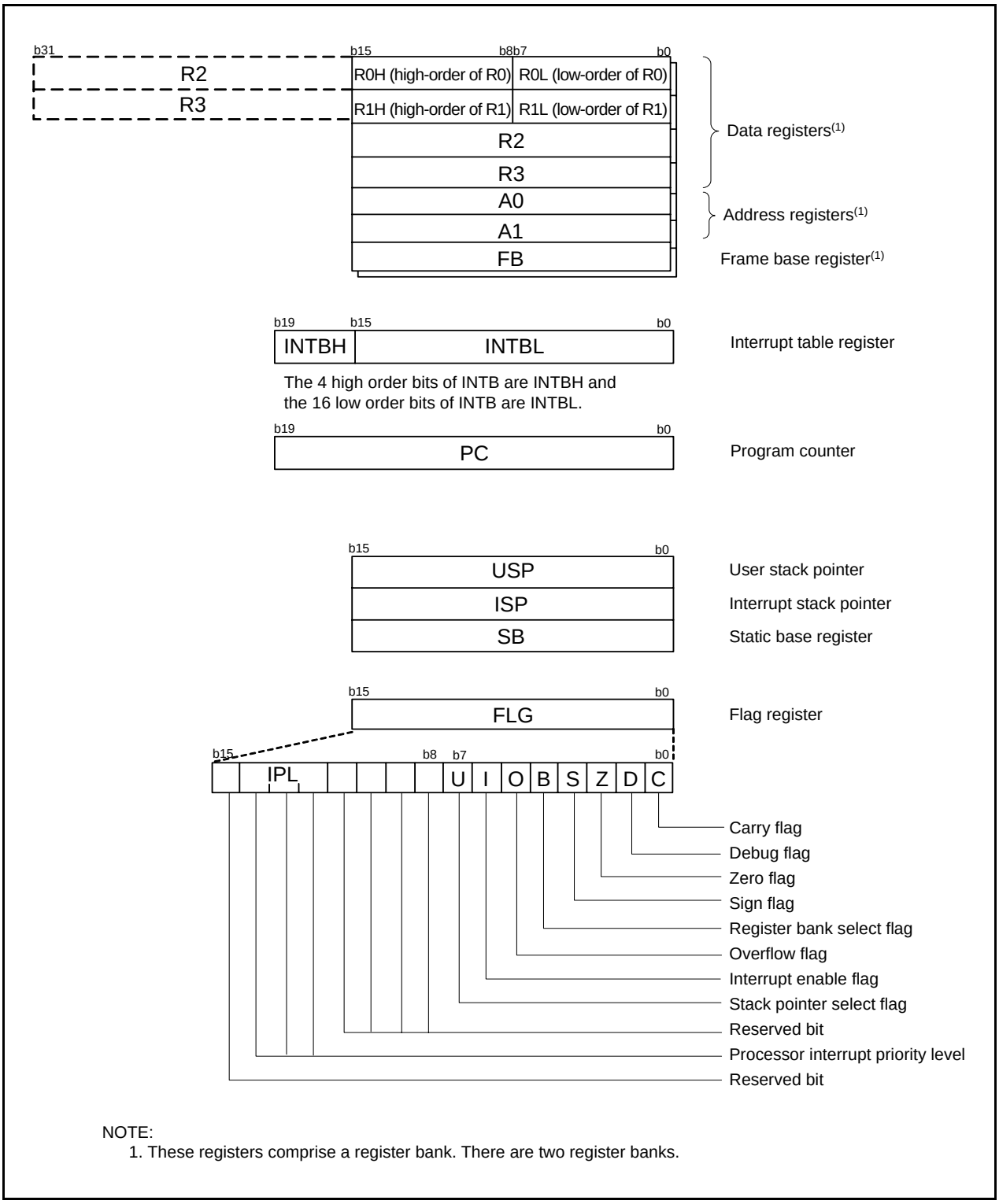



NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. XCIN, XCOUT can be used only for N or D version.
4. Confirm the pin 1 position on the package by referring to the package dimensions.

**Figure 1.4 Pin Assignments (Top View)**

# 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.




NOTE:
1. These registers comprise a register bank. There are two register banks.

**Figure 2.1 CPU Registers**

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

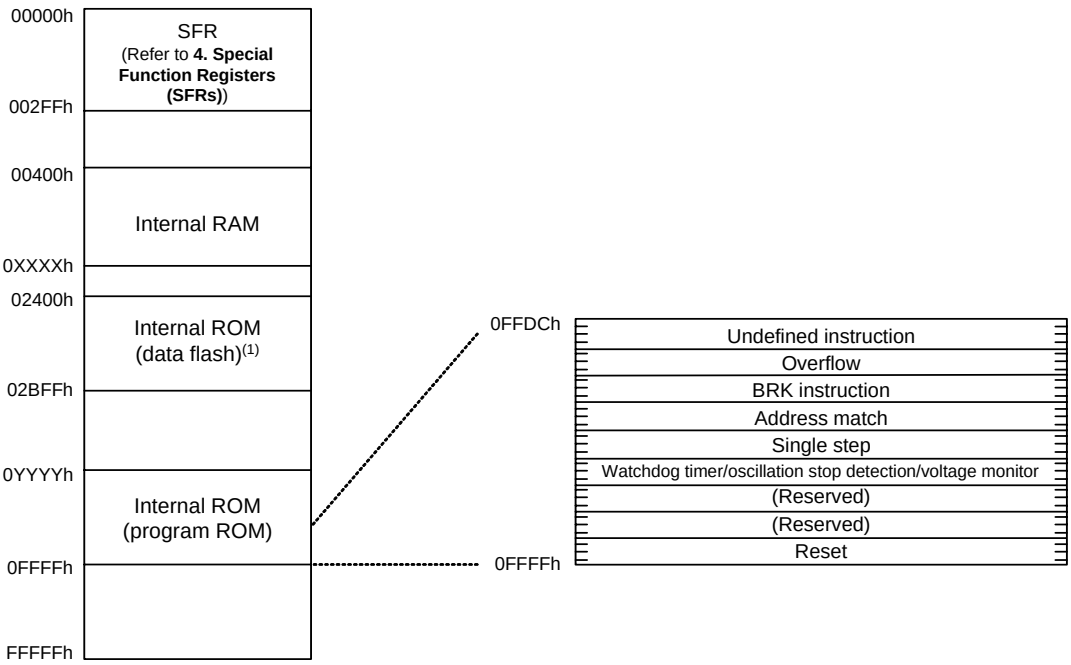
Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

## 3.2 R8C/29 Group

Figure 3.2 is a Memory Map of R8C/29 Group. The R8C/29 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.




NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.

| Part Number | Internal ROM | | Internal RAM | |
|---|---|---|---|---|
| | Size | Address 0YYYYh | Size | Address 0XXXXh |
| R5F21292SNSP, R5F21292SDSP, R5F21292SNXXXSP, R5F21292SDXXXSP | 8 Kbytes | 0E000h | 512 bytes | 005FFh |
| R5F21294SNSP, R5F21294SDSP, R5F21294JSP, R5F21294KSP, R5F21294SNXXXSP, R5F21294SDXXXSP, R5F21294JXXXSP, R5F21294KXXXSP | 16 Kbytes | 0C000h | 1 Kbyte | 007FFh |
| R5F21296JSP, R5F21296KSP, R5F21296JXXXSP, R5F21296KXXXSP | 32 Kbytes | 08000h | 1.5 Kbytes | 009FFh |

**Figure 3.2 Memory Map of R8C/29 Group**

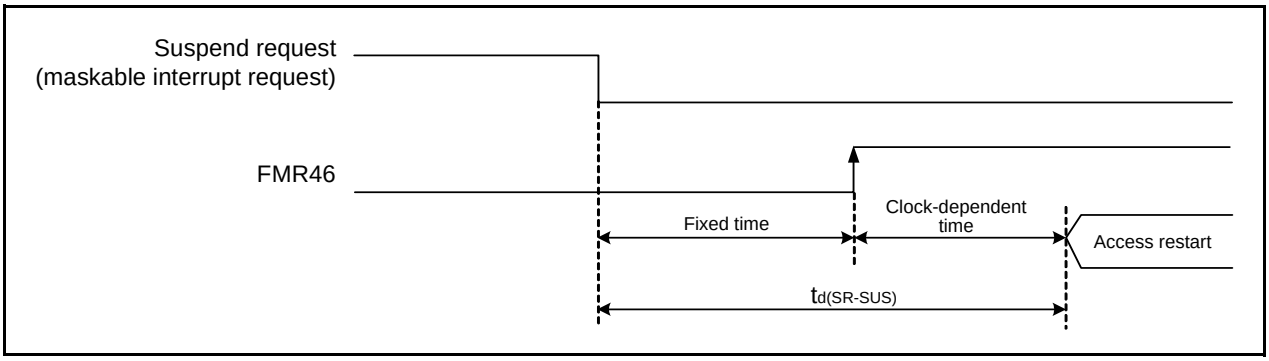



**Figure 5.2 Time delay until Suspend**

### Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det0}$ | Voltage detection level | | 2.2 | 2.3 | 2.4 | V |
| – | Voltage detection circuit self power consumption | VCA25 = 1, $V_{CC}$ = 5.0 V | – | 0.9 | – | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts(2) | | – | – | 300 | µs |
| Vccmin | MCU operating voltage minimum value | | 2.2 | – | – | V |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

### Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det1}$ | Voltage detection level(4) | | 2.70 | 2.85 | 3.00 | V |
| – | Voltage monitor 1 interrupt request generation time(2) | | – | 40 | – | µs |
| – | Voltage detection circuit self power consumption | VCA26 = 1, $V_{CC}$ = 5.0 V | – | 0.6 | – | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts(3) | | – | – | 100 | µs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes $V_{det1}$.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
   The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

### Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det2}$ | Voltage detection level | | 3.3 | 3.6 | 3.9 | V |
| – | Voltage monitor 2 interrupt request generation time(2) | | – | 40 | – | µs |
| – | Voltage detection circuit self power consumption | VCA27 = 1, $V_{CC}$ = 5.0 V | – | 0.6 | – | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts(3) | | – | – | 100 | µs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes $V_{det2}$.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

### Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO40M | High-speed on-chip oscillator frequency temperature • supply voltage dependence | $V_{CC}$ = 4.75 to 5.25 V<br>0°C ≤ $T_{opr}$ ≤ 60°C(2) | 39.2 | 40 | 40.8 | MHz |
| | | $V_{CC}$ = 3.0 to 5.5 V<br>-20°C ≤ $T_{opr}$ ≤ 85°C(2) | 38.8 | 40 | 41.2 | MHz |
| | | $V_{CC}$ = 3.0 to 5.5 V<br>-40°C ≤ $T_{opr}$ ≤ 85°C(2) | 38.4 | 40 | 41.6 | MHz |
| | | $V_{CC}$ = 2.7 to 5.5 V<br>-20°C ≤ $T_{opr}$ ≤ 85°C(2) | 38 | 40 | 42 | MHz |
| | | $V_{CC}$ = 2.7 to 5.5 V<br>-40°C ≤ $T_{opr}$ ≤ 85°C(2) | 37.6 | 40 | 42.4 | MHz |
| | | $V_{CC}$ = 2.2 to 5.5 V<br>-20°C ≤ $T_{opr}$ ≤ 85°C(3) | 35.2 | 40 | 44.8 | MHz |
| | | $V_{CC}$ = 2.2 to 5.5 V<br>-40°C ≤ $T_{opr}$ ≤ 85°C(3) | 34 | 40 | 46 | MHz |
| | | $V_{CC}$ = 5.0 V ± 10%<br>-20°C ≤ $T_{opr}$ ≤ 85°C(2) | 38.8 | 40 | 40.8 | MHz |
| | | $V_{CC}$ = 5.0 V ± 10%<br>-40°C ≤ $T_{opr}$ ≤ 85°C(2) | 38.4 | 40 | 40.8 | MHz |
| | High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register(4) | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 36.864 | – | MHz |
| | | $V_{CC}$ = 3.0 to 5.5 V<br>-20°C ≤ $T_{opr}$ ≤ 85°C | -3% | – | 3% | % |
| – | Value in FRA1 register after reset | | 08h(3) | – | F7h(3) | – |
| – | Oscillation frequency adjustment unit of high-speed on-chip oscillator | Adjust FRA1 register (value after reset) to -1 | – | +0.3 | – | MHz |
| – | Oscillation stability time | | – | 10 | 100 | µs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 400 | – | µA |

NOTES:
1. $V_{CC}$ = 2.2 to 5.5 V, $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.
3. These standard values show when the corrected value of the FRA6 register is written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

### Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| fOCO-S | Low-speed on-chip oscillator frequency | | 30 | 125 | 250 | kHz |
| – | Oscillation stability time | | – | 10 | 100 | µs |
| – | Self power consumption at oscillation | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25°C | – | 15 | – | µA |

NOTE:
1. $V_{CC}$ = 2.2 to 5.5 V, $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

### Table 5.12 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for internal power supply stabilization during power-on(2) | | 1 | – | 2000 | µs |
| $t_{d(R-S)}$ | STOP exit time(3) | | – | – | 150 | µs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.2 to 5.5 V and $T_{opr}$ = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

**Table 5.15 Electrical Characteristics (1) [Vcc = 5 V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | Except P1_0 to P1_7, XOUT | $I_{OH}$ = -5 mA | | Vcc - 2.0 | – | Vcc | V |
| | | | $I_{OH}$ = -200 µA | | Vcc - 0.5 | – | Vcc | V |
| | | P1_0 to P1_7 | Drive capacity HIGH | $I_{OH}$ = -20 mA | Vcc - 2.0 | – | Vcc | V |
| | | | Drive capacity LOW | $I_{OH}$ = -5 mA | Vcc - 2.0 | – | Vcc | V |
| | | XOUT | Drive capacity HIGH | $I_{OH}$ = -1 mA | Vcc - 2.0 | – | Vcc | V |
| | | | Drive capacity LOW | $I_{OH}$ = -500 µA | Vcc - 2.0 | – | Vcc | V |
| $V_{OL}$ | Output “L” voltage | Except P1_0 to P1_7, XOUT | $I_{OL}$ = 5 mA | | – | – | 2.0 | V |
| | | | $I_{OL}$ = 200 µA | | – | – | 0.45 | V |
| | | P1_0 to P1_7 | Drive capacity HIGH | $I_{OL}$ = 20 mA | – | – | 2.0 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 5 mA | – | – | 2.0 | V |
| | | XOUT | Drive capacity HIGH | $I_{OL}$ = 1 mA | – | – | 2.0 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 500 µA | – | – | 2.0 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO | | | 0.1 | 0.5 | – | V |
| | | $\overline{RESET}$ | | | 0.1 | 1.0 | – | V |
| $I_{IH}$ | Input “H” current | | VI = 5 V, Vcc = 5V | | – | – | 5.0 | µA |
| $I_{IL}$ | Input “L” current | | VI = 0 V, Vcc = 5V | | – | – | -5.0 | µA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V, Vcc = 5V | | 30 | 50 | 167 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 1.0 | – | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | – | 18 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

NOTE:
1. Vcc = 4.2 to 5.5 V at $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

**Table 5.17 Electrical Characteristics (3) [Vcc = 5 V]**
**($T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $I_{CC}$ | Power supply current ($V_{CC}$ = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are $V_{SS}$ | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 25 | 75 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 23 | 60 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (high drive)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 4.0 | – | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (low drive)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 2.2 | – | µA |
| | | Stop mode | XIN clock off, $T_{opr}$ = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 0.8 | 3.0 | µA |
| | | | XIN clock off, $T_{opr}$ = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 1.2 | – | µA |

**Timing Requirements**
**(Unless Otherwise Specified: $V_{CC}$ = 5 V, $V_{SS}$ = 0 V at $T_{opr}$ = 25°C) [$V_{CC}$ = 5 V]**

**Table 5.18 XIN Input, XCIN Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 50 | – | ns |
| $t_{WH(XIN)}$ | XIN input “H” width | 25 | – | ns |
| $t_{WL(XIN)}$ | XIN input “L” width | 25 | – | ns |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | – | µs |
| $t_{WH(XCIN)}$ | XCIN input “H” width | 7 | – | µs |
| $t_{WL(XCIN)}$ | XCIN input “L” width | 7 | – | µs |

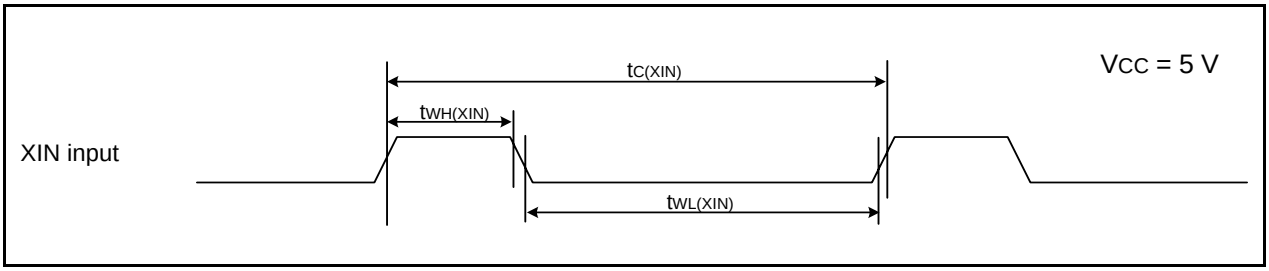



**Figure 5.8 XIN Input and XCIN Input Timing Diagram when $V_{CC}$ = 5 V**

**Table 5.19 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 100 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width | 40 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width | 40 | – | ns |

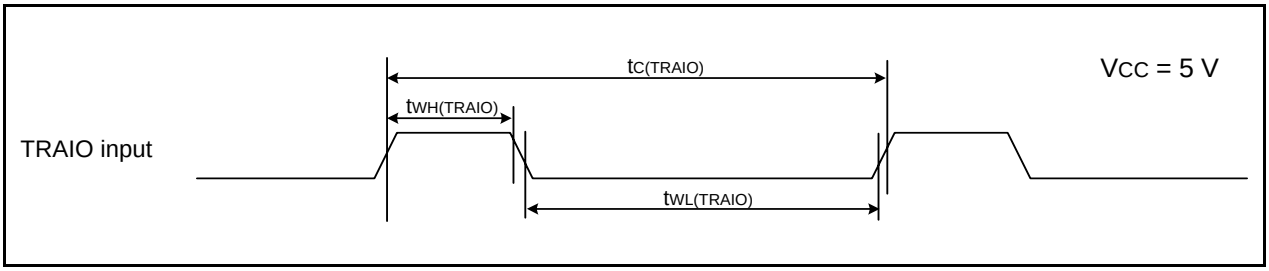



**Figure 5.9 TRAIO Input Timing Diagram when $V_{CC}$ = 5 V**

**Table 5.28 Electrical Characteristics (5) [Vcc = 2.2 V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | Except P1_0 to P1_7, XOUT | $I_{OH}$ = -1 mA | | Vcc - 0.5 | – | Vcc | V |
| | | P1_0 to P1_7 | Drive capacity HIGH | $I_{OH}$ = -2 mA | Vcc - 0.5 | – | Vcc | V |
| | | | Drive capacity LOW | $I_{OH}$ = -1 mA | Vcc - 0.5 | – | Vcc | V |
| | | XOUT | Drive capacity HIGH | $I_{OH}$ = -0.1 mA | Vcc - 0.5 | – | Vcc | V |
| | | | Drive capacity LOW | $I_{OH}$ = -50 µA | Vcc - 0.5 | – | Vcc | V |
| $V_{OL}$ | Output “L” voltage | Except P1_0 to P1_7, XOUT | $I_{OL}$ = 1 mA | | – | – | 0.5 | V |
| | | P1_0 to P1_7 | Drive capacity HIGH | $I_{OL}$ = 2 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 1 mA | – | – | 0.5 | V |
| | | XOUT | Drive capacity HIGH | $I_{OL}$ = 0.1 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 50 µA | – | – | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO | | | 0.05 | 0.3 | – | V |
| | | $\overline{RESET}$ | | | 0.05 | 0.15 | – | V |
| $I_{IH}$ | Input “H” current | | VI = 2.2 V | | – | – | 4.0 | µA |
| $I_{IL}$ | Input “L” current | | VI = 0 V | | – | – | -4.0 | µA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V | | 100 | 200 | 600 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 5 | – | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | – | 35 | – | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

NOTE:
1. Vcc = 2.2 V at $T_{opr}$ = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

**Timing requirements**
**(Unless Otherwise Specified: $V_{CC}$ = 2.2 V, $V_{SS}$ = 0 V at $T_{opr}$ = 25°C) [$V_{CC}$ = 2.2 V]**

**Table 5.30 XIN Input, XCIN Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 200 | – | ns |
| $t_{WH(XIN)}$ | XIN input “H” width | 90 | – | ns |
| $t_{WL(XIN)}$ | XIN input “L” width | 90 | – | ns |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | – | µs |
| $t_{WH(XCIN)}$ | XCIN input “H” width | 7 | – | µs |
| $t_{WL(XCIN)}$ | XCIN input “L” width | 7 | – | µs |

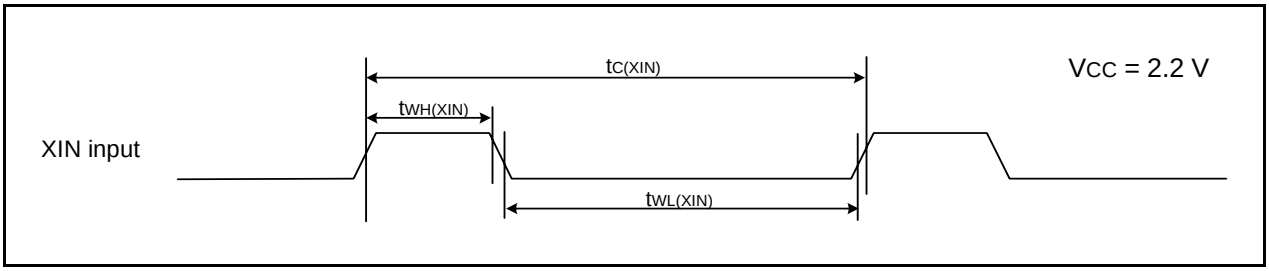



**Figure 5.16 XIN Input and XCIN Input Timing Diagram when $V_{CC}$ = 2.2 V**

**Table 5.31 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 500 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width | 200 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width | 200 | – | ns |

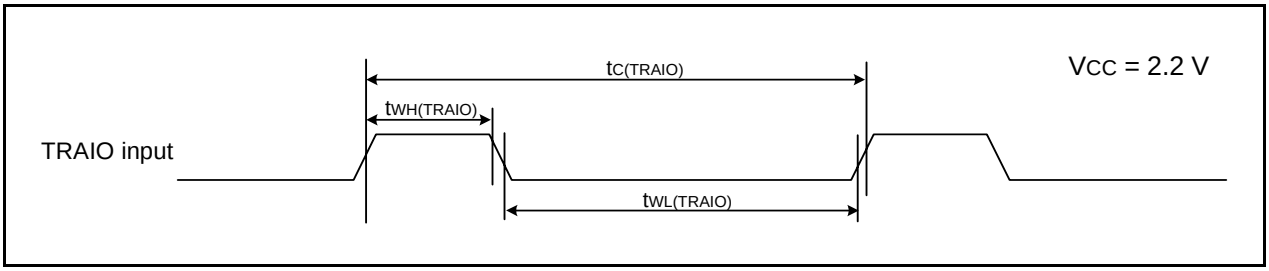



**Figure 5.17 TRAIO Input Timing Diagram when $V_{CC}$ = 2.2 V**

## 5.2 J, K Version

### Table 5.34 Absolute Maximum Ratings

| Symbol | Parameter | Condition | Rated Value | Unit |
|---|---|---|---|---|
| $V_{CC}$/$AV_{CC}$ | Supply voltage | | -0.3 to 6.5 | V |
| $V_I$ | Input voltage | | -0.3 to $V_{CC}$ + 0.3 | V |
| $V_O$ | Output voltage | | -0.3 to $V_{CC}$ + 0.3 | V |
| $P_d$ | Power dissipation | -40 °C ≤ $T_{opr}$ ≤ 85 °C | 300 | mW |
| | | 85 °C ≤ $T_{opr}$ ≤ 125 °C | 125 | mW |
| $T_{opr}$ | Operating ambient temperature | | -40 to 85 (J version) / -40 to 125 (K version) | °C |
| $T_{stg}$ | Storage temperature | | -65 to 150 | °C |

### Table 5.35 Recommended Operating Conditions

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{CC}$/$AV_{CC}$ | Supply voltage | | | 2.7 | – | 5.5 | V |
| $V_{SS}$/$AV_{SS}$ | Supply voltage | | | – | 0 | – | V |
| $V_{IH}$ | Input “H” voltage | | | 0.8 $V_{CC}$ | – | $V_{CC}$ | V |
| $V_{IL}$ | Input “L” voltage | | | 0 | – | 0.2 $V_{CC}$ | V |
| $I_{OH(sum)}$ | Peak sum output “H” current | Sum of all pins $I_{OH(peak)}$ | | – | – | -60 | mA |
| $I_{OH(peak)}$ | Peak output “H” current | | | – | – | -10 | mA |
| $I_{OH(avg)}$ | Average output “H” current | | | – | – | -5 | mA |
| $I_{OL(sum)}$ | Peak sum output “L” currents | Sum of all pins $I_{OL(peak)}$ | | – | – | 60 | mA |
| $I_{OL(peak)}$ | Peak output “L” currents | | | – | – | 10 | mA |
| $I_{OL(avg)}$ | Average output “L” current | | | – | – | 5 | mA |
| $f_{(XIN)}$ | XIN clock input oscillation frequency | | 3.0 V ≤ $V_{CC}$ ≤ 5.5 V (other than K version) | 0 | – | 20 | MHz |
| | | | 3.0 V ≤ $V_{CC}$ ≤ 5.5 V (K version) | 0 | – | 16 | MHz |
| | | | 2.7 V ≤ $V_{CC}$ < 3.0 V | 0 | – | 10 | MHz |
| – | System clock | OCD2 = 0 XIN clock selected | 3.0 V ≤ $V_{CC}$ ≤ 5.5 V (other than K version) | 0 | – | 20 | MHz |
| | | | 3.0 V ≤ $V_{CC}$ ≤ 5.5 V (K version) | 0 | – | 16 | MHz |
| | | | 2.7 V ≤ $V_{CC}$ < 3.0 V | 0 | – | 10 | MHz |
| | | OCD2 = 1 On-chip oscillator clock selected | FRA01 = 0 Low-speed on-chip oscillator clock selected | – | 125 | – | kHz |
| | | | FRA01 = 1 High-speed on-chip oscillator clock selected (other than K version) | – | – | 20 | MHz |
| | | | FRA01 = 1 High-speed on-chip oscillator clock selected | – | – | 10 | MHz |

NOTES:
1. $V_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

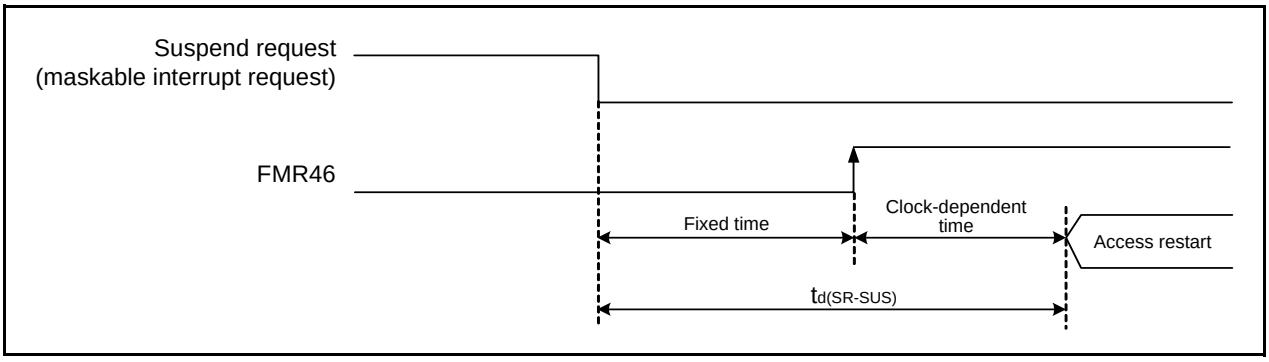



**Figure 5.21 Time delay until Suspend**

### Table 5.39 Voltage Detection 1 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det1}$ | Voltage detection level(2, 4) | | 2.70 | 2.85 | 3.0 | V |
| $t_{d(Vdet1-A)}$ | Voltage monitor 1 reset generation time(5) | | – | 40 | 200 | µs |
| – | Voltage detection circuit self power consumption | VCA26 = 1, $V_{CC}$ = 5.0 V | – | 0.6 | – | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts(3) | | – | – | 100 | µs |
| Vccmin | MCU operating voltage minimum value | | 2.70 | – | – | V |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.7 to 5.5 V and $T_{opr}$ = -40 to 85°C (J version) / -40 to 125°C (K version).
2. Hold $V_{det2} > V_{det1}$.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
   The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.
5. Time until the voltage monitor 1 reset is generated after the voltage passes $V_{det1}$ when $V_{CC}$ falls. When using the digital filter, its sampling time is added to $t_{d(Vdet1-A)}$. When using the voltage monitor 1 reset, maintain this time until $V_{CC}$ = 2.0 V after the voltage passes $V_{det1}$ when the power supply falls.

### Table 5.40 Voltage Detection 2 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det2}$ | Voltage detection level(2) | | 3.3 | 3.6 | 3.9 | V |
| $t_{d(Vdet2-A)}$ | Voltage monitor 2 reset/interrupt request generation time(3., 5) | | – | 40 | 200 | µs |
| – | Voltage detection circuit self power consumption | VCA27 = 1, $V_{CC}$ = 5.0 V | – | 0.6 | – | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts(4) | | – | – | 100 | µs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.7 to 5.5 V and $T_{opr}$ = -40 to 85°C (J version) / -40 to 125°C (K version).
2. Hold $V_{det2} > V_{det1}$.
3. Time until the voltage monitor 2 reset/interrupt request is generated after the voltage passes $V_{det2}$.
4. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
5. When using the digital filter, its sampling time is added to $t_{d(Vdet2-A)}$. When using the voltage monitor 2 reset, maintain this time until $V_{CC}$ = 2.0 V after the voltage passes $V_{det2}$ when the power supply falls.

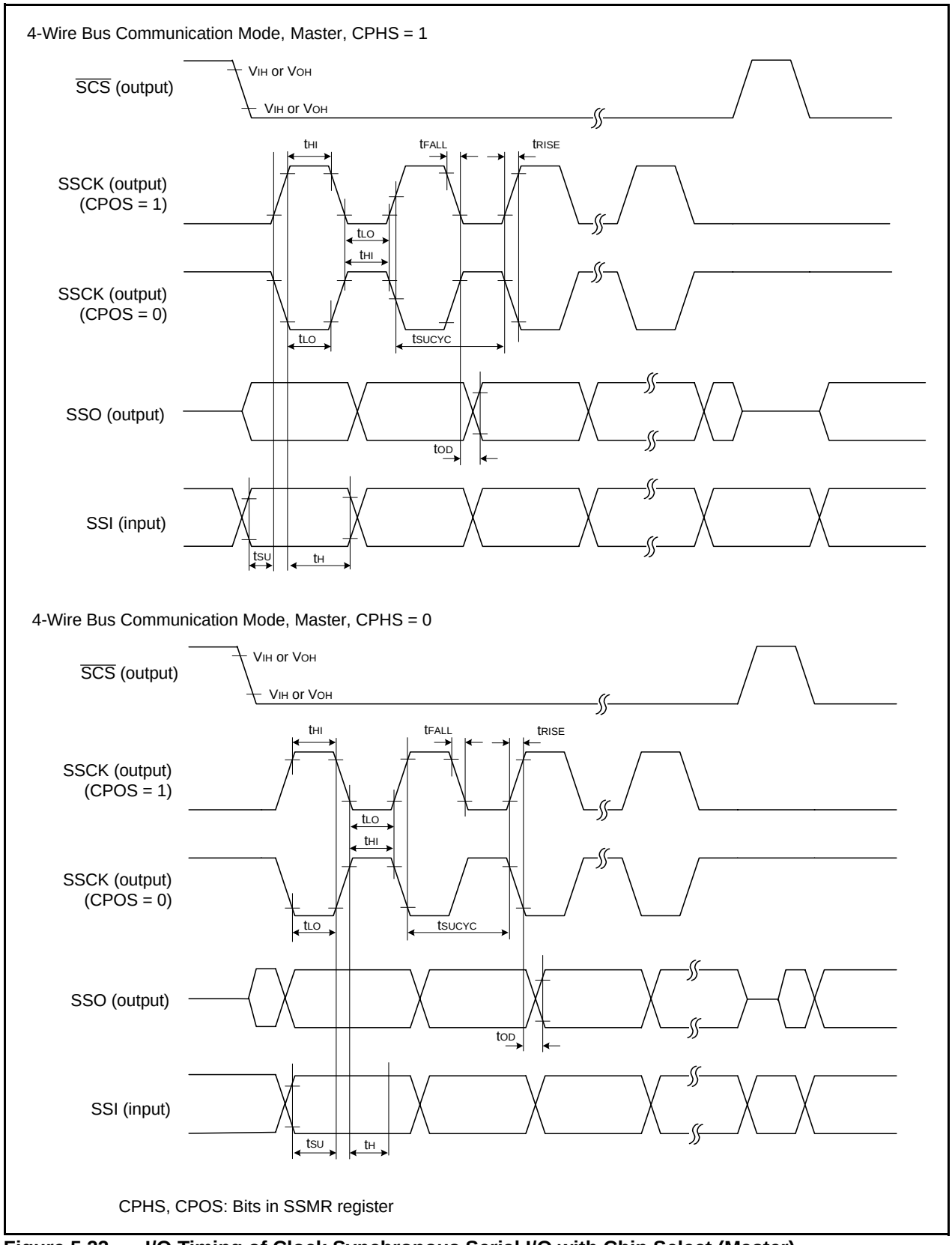



**Figure 5.23 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)**

**Table 5.51 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLK0 input cycle time | 200 | – | ns |
| $t_{W(CKH)}$ | CLK0 input “H” width | 100 | – | ns |
| $t_{W(CKL)}$ | CLK0 input “L” width | 100 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 50 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 50 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0 or 1

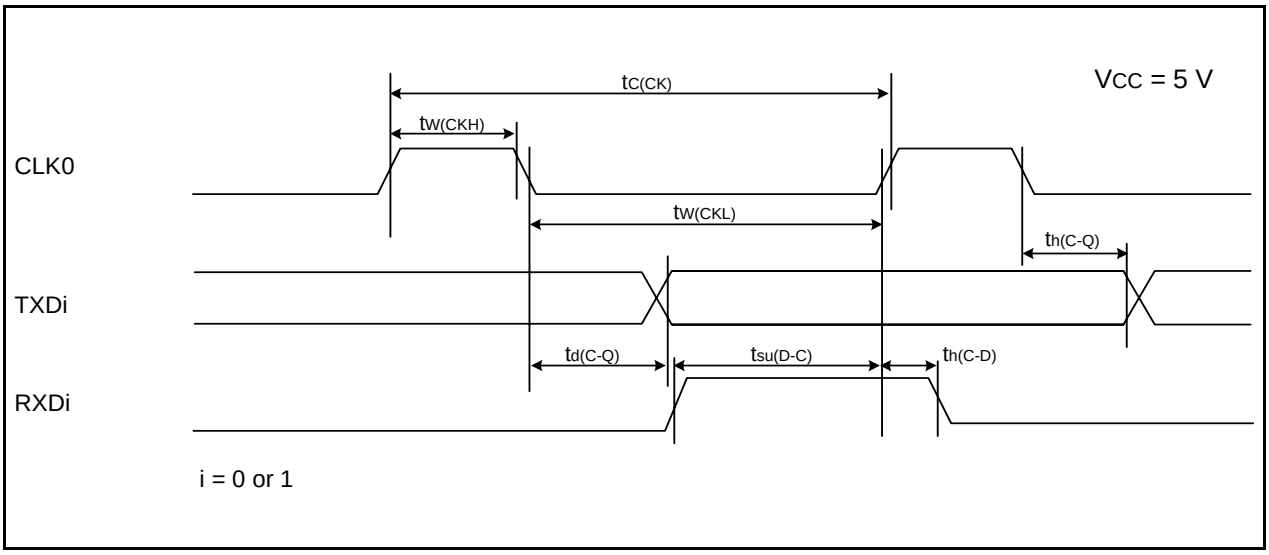



**Figure 5.29 Serial Interface Timing Diagram when VCC = 5 V**

**Table 5.52 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{INTi}$ input “H” width | 250(1) | – | ns |
| $t_{W(INL)}$ | $\overline{INTi}$ input “L” width | 250(2) | – | ns |

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

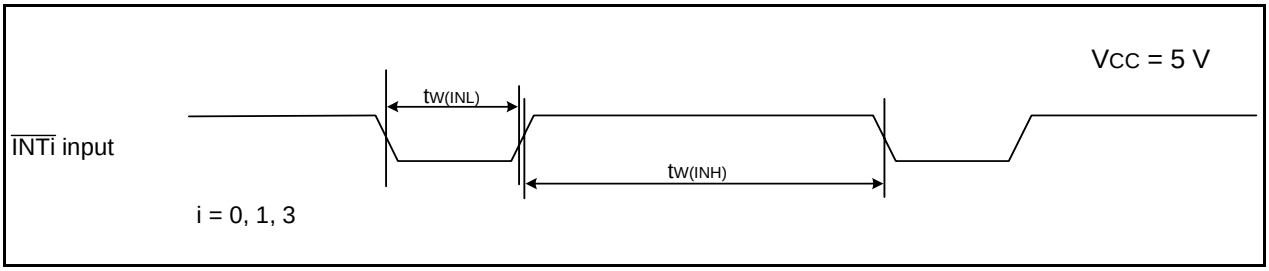



**Figure 5.30 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 5 V**

**Table 5.54 Electrical Characteristics (4) [Vcc = 3 V]**
**(Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| ICC | Power supply current (VCC = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are VSS | High-speed clock mode | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 6 | – | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 5 | 9 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR47 = 1 | – | 130 | 300 | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 25 | 70 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0<br>VCA20 = 1 | – | 23 | 55 | µA |
| | | Stop mode | XIN clock off, Topr = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 0.7 | 3.0 | µA |
| | | | XIN clock off, Topr = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 1.1 | – | µA |
| | | | XIN clock off, Topr = 125°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | – | 3.8 | – | µA |

**Table 5.57 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLK0 input cycle time | 300 | – | ns |
| $t_{W(CKH)}$ | CLK0 input “H” width | 150 | – | ns |
| $t_{W(CKL)}$ | CLK0 Input “L” width | 150 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 80 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 70 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0 or 1

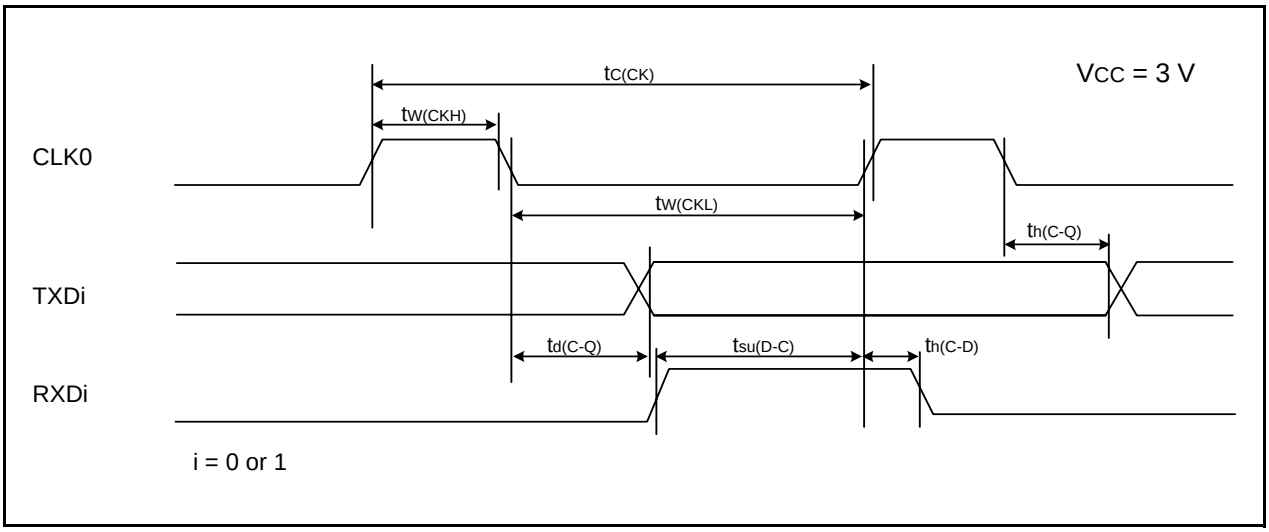



**Figure 5.33 Serial Interface Timing Diagram when VCC = 3 V**

**Table 5.58 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{INTi}$ input “H” width | 380(1) | – | ns |
| $t_{W(INL)}$ | $\overline{INTi}$ input “L” width | 380(2) | – | ns |

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

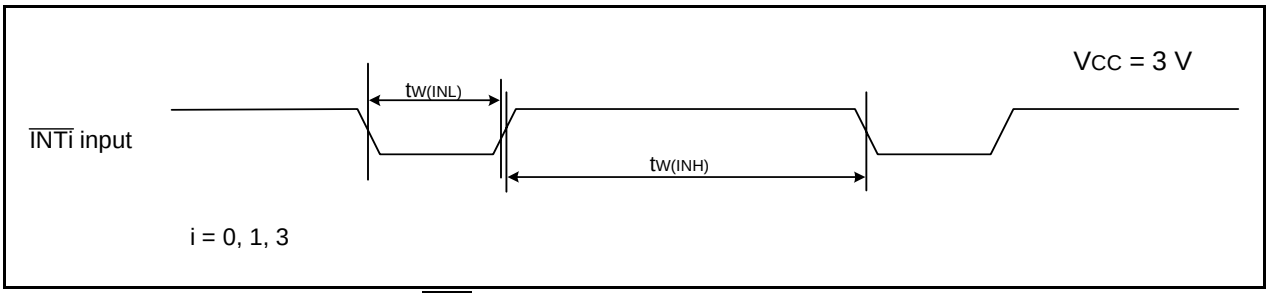



**Figure 5.34 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 3 V**

| REVISION HISTORY | R8C/28 Group, R8C/29 Group Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Nov 08, 2006 | 15 | Table 4.1;<br>• "0000h to 003Fh" → "0000h to 002Fh" revised<br>• 000Fh: "000XXXXXb" → "00X11111b" revised<br>• 001Ch: "00h" → "00h, 10000000b" revised<br>• 0029h: "High-Speed On-Chip Oscillator Control Register 4, FRA4, When shipping" added<br>• 002Bh: "High-Speed On-Chip Oscillator Control Register 6, FRA6, When shipping" added<br>• NOTE2 revised, NOTE3 added |
| | | 16 | Table 4.2; "0040h to 007Fh" → "0030h to 007Fh" revised |
| | | 18 | Table 4.4; 00E1h, 00E5h, 00E8h "XXh" → "00h" revised |
| | | 22 | Table 5.2 revised |
| | | 23 | Figure 5.1 figure title revised |
| | | 24 | Table 5.4 revised |
| | | 25 | Table 5.5 revised |
| | | 26 | Figure 5.2 figure title revised and Table 5.7 NOTE4 added |
| | | 27 | Table 5.9 revised, Figure 5.3 revised |
| | | 28 | Table 5.10, Table 5.11revised |
| | | 34 | Table 5.15 revised |
| | | 35 | Table 5.16 revised |
| | | 36 | Table 5.17 revised |
| | | 39 | Table 5.22 revised |
| | | 40 | Table 5.23 revised |
| | | 44 | Table 5.29 revised |
| | | 47 | 5.2 "J and K versions are under development...notice." added<br>Table 5.34, Table 5.35 revised |
| | | 48 | Table 5.36 revised, Figure 5.20 figure title revised |
| | | 51 | Figure 5.21 figure title revised |
| | | 52 | Table 5.41, Figure 5.22 revised |
| | | 53 | Table 5.42, Table 5.43 revised |
| | | 59 | Table 5.47 revised |
| | | 60 | Table 5.48 revised |
| | | 63 | Table 5.53 revised |
| | | 64 | Table 5.54 revised |
| | | 67 | Package Dimensions; "Diagrams showing the latest...website." added |
| 1.10 | May 17, 2007 | 2 | Table 1.1 revised |
| | | 3 | Table 1.2 revised |
| | | 5 | Table 1.3 and Figure 1.2 revised |
| | | 6 | Table 1.4 and Figure 1.3 revised |
| | | 7 | Figure 1.4 NOTE4 added |