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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21292sdsp-u0

1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C CPU core, and are packaged in a 20-pin molded-plastic LSSOP. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.

Furthermore, the R8C/29 Group has on-chip data flash (1 KB \times 2 blocks).

The difference between the R8C/28 Group and R8C/29 Group is only the presence or absence of data flash. Their peripheral functions are the same.

1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer products, automotive, etc.

1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/28 Group and Table 1.2 outlines the Functions and Specifications for R8C/29 Group.

Table 1.1 Functions and Specifications for R8C/28 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns ($f(XIN) = 20$ MHz, $VCC = 3.0$ to 5.5 V) (other than K version) 62.5 ns ($f(XIN) = 16$ MHz, $VCC = 3.0$ to 5.5 V) (K version) 100 ns ($f(XIN) = 10$ MHz, $VCC = 2.7$ to 5.5 V) 200 ns ($f(XIN) = 5$ MHz, $VCC = 2.2$ to 5.5 V) (N, D version)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to Table 1.3 Product Information for R8C/28 Group
Peripheral Functions	Ports	I/O ports: 13 pins, Input port: 3 pins
	LED drive ports	I/O ports: 8 pins (N, D version)
	Timers	Timer RA: 8 bits \times 1 channel Timer RB: 8 bits \times 1 channel (Each timer equipped with 8-bit prescaler) Timer RC: 16 bits \times 1 channel (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function (For J, K version, compare match function only.)
	Serial interfaces	1 channel (UART0): Clock synchronous serial I/O, UART 1 channel (UART1): UART
	Clock synchronous serial interface	1 channel I ² C bus Interface ⁽¹⁾ Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog timer	15 bits \times 1 channel (with prescaler) Reset start selectable
	Interrupts	Internal: 15 sources (N, D version), Internal: 14 sources (J, K version) External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	3 circuits • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz) (N, D version) • Real-time clock (timer RE) (N, D version)
	Oscillation stop detection function	XIN clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip
Electrical Characteristics	Supply voltage	$VCC = 3.0$ to 5.5 V ($f(XIN) = 20$ MHz) (other than K version) $VCC = 3.0$ to 5.5 V ($f(XIN) = 16$ MHz) (K version) $VCC = 2.7$ to 5.5 V ($f(XIN) = 10$ MHz) $VCC = 2.2$ to 5.5 V ($f(XIN) = 5$ MHz) (N, D version)
	Current consumption (N, D version)	Typ. 10 mA ($VCC = 5.0$ V, $f(XIN) = 20$ MHz) Typ. 6 mA ($VCC = 3.0$ V, $f(XIN) = 10$ MHz) Typ. 2.0 μ A ($VCC = 3.0$ V, wait mode ($f(XCIN) = 32$ kHz)) Typ. 0.7 μ A ($VCC = 3.0$ V, stop mode)
Flash Memory	Programming and erasure voltage	$VCC = 2.7$ to 5.5 V
	Programming and erasure endurance	100 times
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D, J version) ⁽²⁾ , -40 to 125°C (K version) ⁽²⁾
Package		20-pin molded-plastic LSSOP

NOTES:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D, K version if D, K version functions are to be used.

Table 1.2 Functions and Specifications for R8C/29 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns ($f(XIN) = 20$ MHz, $VCC = 3.0$ to 5.5 V) (other than K version) 62.5 ns ($f(XIN) = 16$ MHz, $VCC = 3.0$ to 5.5 V) (K version) 100 ns ($f(XIN) = 10$ MHz, $VCC = 2.7$ to 5.5 V) 200 ns ($f(XIN) = 5$ MHz, $VCC = 2.2$ to 5.5 V) (N, D version)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to Table 1.4 Product Information for R8C/29 Group
Peripheral Functions	Ports	I/O ports: 13 pins, Input port: 3 pins
	LED drive ports	I/O ports: 8 pins (N, D version)
	Timers	Timer RA: 8 bits \times 1 channel Timer RB: 8 bits \times 1 channel (Each timer equipped with 8-bit prescaler) Timer RC: 16 bits \times 1 channel (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function (For J, K version, compare match function only.)
	Serial interfaces	1 channel (UART0): Clock synchronous serial I/O, UART 1 channel (UART1): UART
	Clock synchronous serial interface	1 channel I ² C bus Interface ⁽¹⁾ Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog timer	15 bits \times 1 channel (with prescaler) Reset start selectable
	Interrupts	Internal: 15 sources (N, D version), Internal: 14 sources (J, K version) External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	3 circuits • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz) (N, D version) • Real-time clock (timer RE) (N, D version)
	Oscillation stop detection function	XIN clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip
Electrical Characteristics	Supply voltage	$VCC = 3.0$ to 5.5 V ($f(XIN) = 20$ MHz) (other than K version) $VCC = 3.0$ to 5.5 V ($f(XIN) = 16$ MHz) (K version) $VCC = 2.7$ to 5.5 V ($f(XIN) = 10$ MHz) $VCC = 2.2$ to 5.5 V ($f(XIN) = 5$ MHz) (N, D version)
	Current consumption (N, D version)	Typ. 10 mA ($VCC = 5.0$ V, $f(XIN) = 20$ MHz) Typ. 6 mA ($VCC = 3.0$ V, $f(XIN) = 10$ MHz) Typ. 2.0 μ A ($VCC = 3.0$ V, wait mode ($f(XCIN) = 32$ kHz)) Typ. 0.7 μ A ($VCC = 3.0$ V, stop mode)
Flash Memory	Programming and erasure voltage	$VCC = 2.7$ to 5.5 V
	Programming and erasure endurance	10,000 times (data flash) 1,000 times (program ROM)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D, J version) ⁽²⁾ , -40 to 125°C (K version) ⁽²⁾
Package		20-pin molded-plastic LSSOP

NOTES:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D, K version if D, K version functions are to be used.

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I ² C bus Interface	A/D Converter
1		P3_5		TRCIOD		SSCK	SCL	
2		P3_7		TRAO	RXD1/(TXD1) ⁽¹⁾	SSO		
3	RESET							
4	XOUT/XCOUT ⁽²⁾	P4_7						
5	VSS/AVSS							
6	XIN/XCIN ⁽²⁾	P4_6						
7	VCC/AVCC							
8	MODE							
9		P4_5	INT0		(RXD1) ⁽¹⁾			
10		P1_7	INT1	TRAIO				
11		P1_6			CLK0	(SSI) ⁽¹⁾		
12		P1_5	(INT1) ⁽¹⁾	(TRAIO) ⁽¹⁾	RXD0			
13		P1_4			TXD0			
14		P1_3	KI3	TRBO				AN11
15		P1_2	KI2	TRCIOB				AN10
16	VRFF	P4_2						
17		P1_1	KI1	TRCIOA/TRCTRG				AN9
18		P1_0	KI0					AN8
19		P3_3	INT3	TRCCLK		SSI		
20		P3_4		TRCIOC		SCS	SDA	

NOTES:

1. This can be assigned to the pin in parentheses by a program.
2. XCIN, XCOUT can be used only for N or D version.

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

Table 4.2 SFR Information (2)⁽¹⁾

Address	Register	Symbol	After reset
0030h			
0031h	Voltage Detection Register 1 ⁽²⁾	VCA1	00001000b
0032h	Voltage Detection Register 2 ⁽²⁾	VCA2	<ul style="list-style-type: none"> • N, D version 00h⁽³⁾ • J, K version 00100000b⁽⁴⁾ 00h⁽⁷⁾ 01000000b⁽⁸⁾
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register ⁽⁵⁾	VW1C	<ul style="list-style-type: none"> • N, D version 00001000b • J, K version 0000X000b⁽⁷⁾ 0100X001b⁽⁸⁾
0037h	Voltage Monitor 2 Circuit Control Register ⁽⁵⁾	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register ⁽⁶⁾	VW0C	0000X000b ⁽³⁾ 0100X001b ⁽⁴⁾
0039h			
003Fh			
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU/IIC bus Interrupt Control Register ⁽⁹⁾	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
006Fh			
0070h			
007Fh			

X: Undefined

NOTES:

- The blank regions are reserved. Do not access locations in these regions.
- (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
(J, K version) Software reset, watchdog timer reset, or voltage monitor 2 reset do not affect this register.
- The LVD00N bit in the OFS register is set to 1 and hardware reset.
- Power-on reset, voltage monitor 0 reset, or the LVD00N bit in the OFS register is set to 0 and hardware reset.
- (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
(J, K version) Software reset, watchdog timer reset, or voltage monitor 2 reset do not affect b2 and b3.
- (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
(J, K version) These regions are reserved. Do not access locations in these regions.
- The LVD10N bit in the OFS register is set to 1 and hardware reset.
- Power-on reset, voltage monitor 1 reset, or the LVD10N bit in the OFS register is set to 0 and hardware reset.
- Selected by the IICSEL bit in the PMR register.

Table 4.4 SFR Information (4)⁽¹⁾

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h			
00E1h	Port P1 Register	P1	00h
00E2h			
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	00h
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	00h
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h	Pin Select Register 1	PINSR1	00h
00F6h	Pin Select Register 2	PINSR2	00h
00F7h	Pin Select Register 3	PINSR3	00h
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	00h
00FEh	Port P1 Drive Capacity Control Register ⁽²⁾	P1DRR	00h
00FFh			

X: Undefined

NOTES:

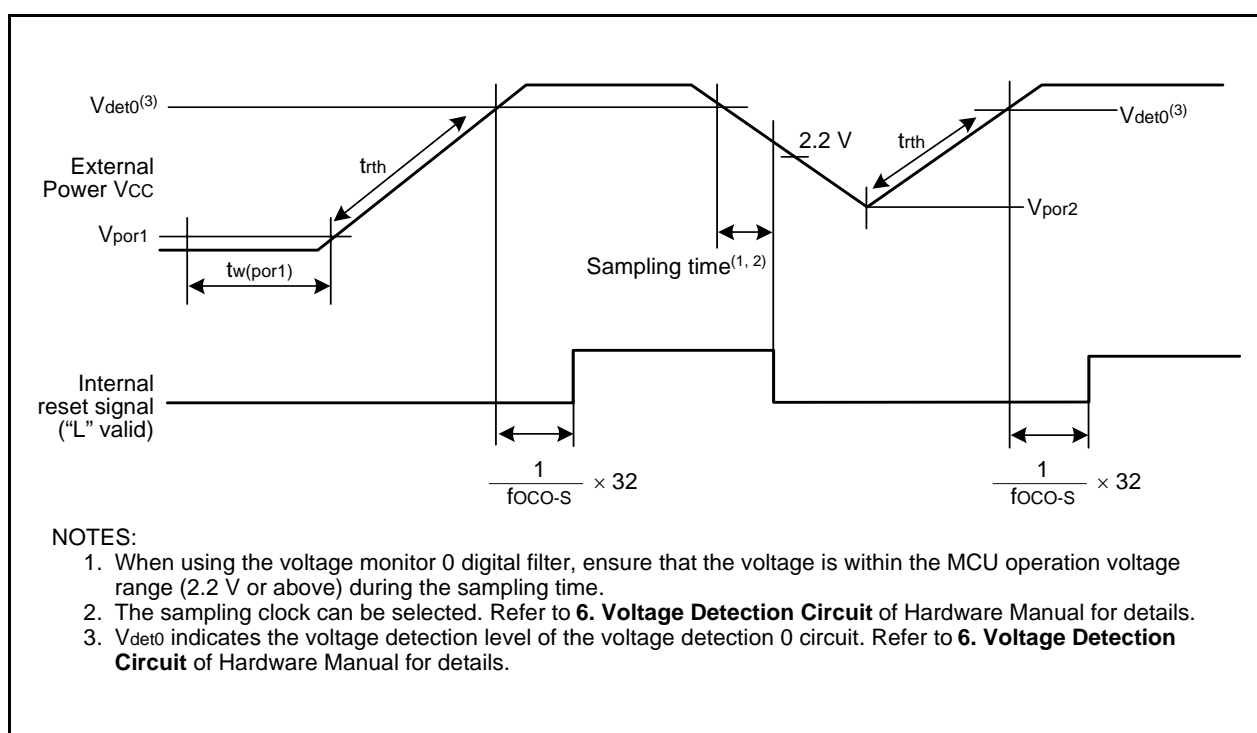
1. The blank regions are reserved. Do not access locations in these regions.
2. In J, K version these regions are reserved. Do not access locations in these regions.

Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics⁽³⁾

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{por1}	Power-on reset valid voltage ⁽⁴⁾		–	–	0.1	V
V _{por2}	Power-on reset or voltage monitor 0 reset valid voltage		0	–	V _{det0}	V
tr _{th}	External power V _{CC} rise gradient ⁽²⁾		20	–	–	mV/msec

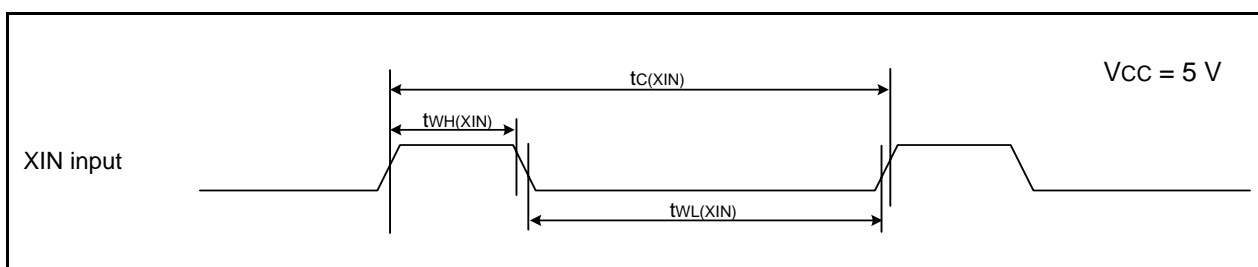
NOTES:

1. The measurement condition is T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if V_{CC} ≥ 1.0 V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. tw_(por1) indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain tw_(por1) for 30 s or more if -20°C ≤ T_{opr} ≤ 85°C, maintain tw_(por1) for 3,000 s or more if -40°C ≤ T_{opr} < -20°C.

**Figure 5.3 Reset Circuit Electrical Characteristics**

Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 5\text{ V}$]****Table 5.18 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input "H" width	25	–	ns
$t_{WL(XIN)}$	XIN input "L" width	25	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input "H" width	7	–	μs
$t_{WL(XCIN)}$	XCIN input "L" width	7	–	μs

**Figure 5.8 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.19 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	40	–	ns

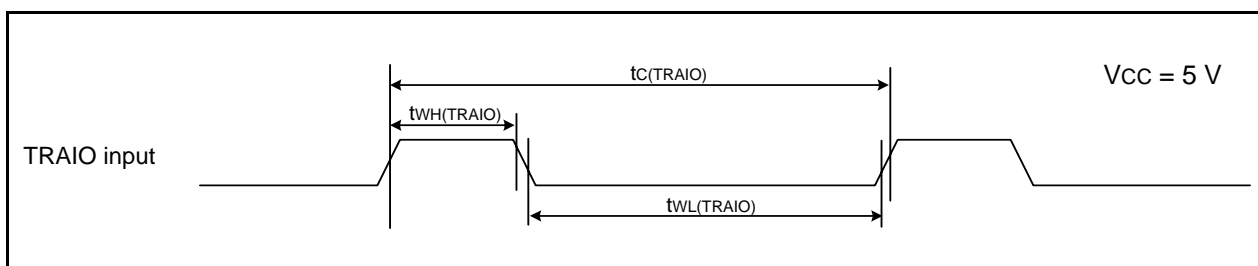
**Figure 5.9 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

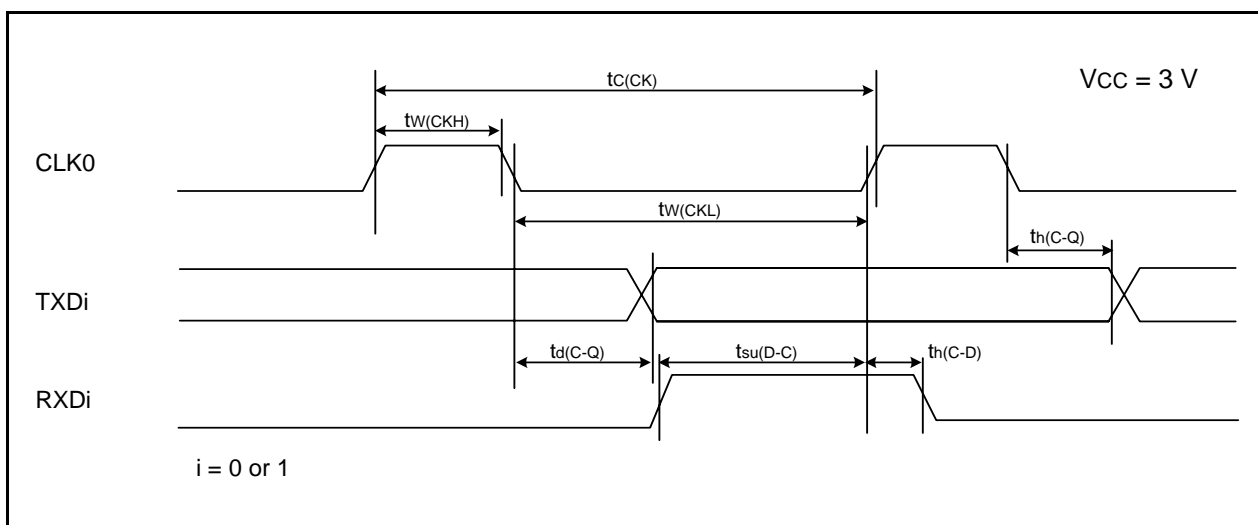
Table 5.23 Electrical Characteristics (4) [V_{CC} = 3 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division			mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8			mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on f _{OCO} = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division			mA
			XIN clock off High-speed on-chip oscillator on f _{OCO} = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8			mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1			μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1			μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1			μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1			μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1			μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1			μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1			μA
			XIN clock off, T _{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0			μA
		Stop mode	XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0			μA
			XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0			μA

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	—	ns
$t_{w(CKH)}$	CLK0 input “H” width	150	—	ns
$t_{w(CKL)}$	CLK0 Input “L” width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 or 1

**Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.27 External Interrupt \overline{INTi} (i = 0, 1, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INTi} input “H” width	380 ⁽¹⁾	—	ns
$t_{w(INL)}$	\overline{INTi} input “L” width	380 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

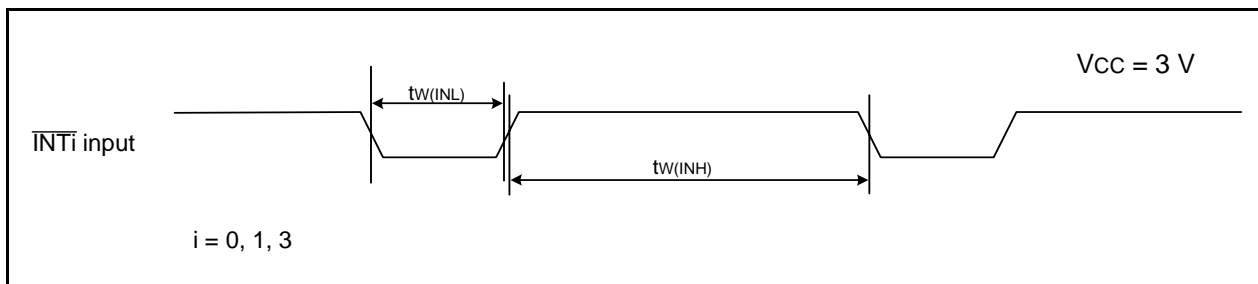
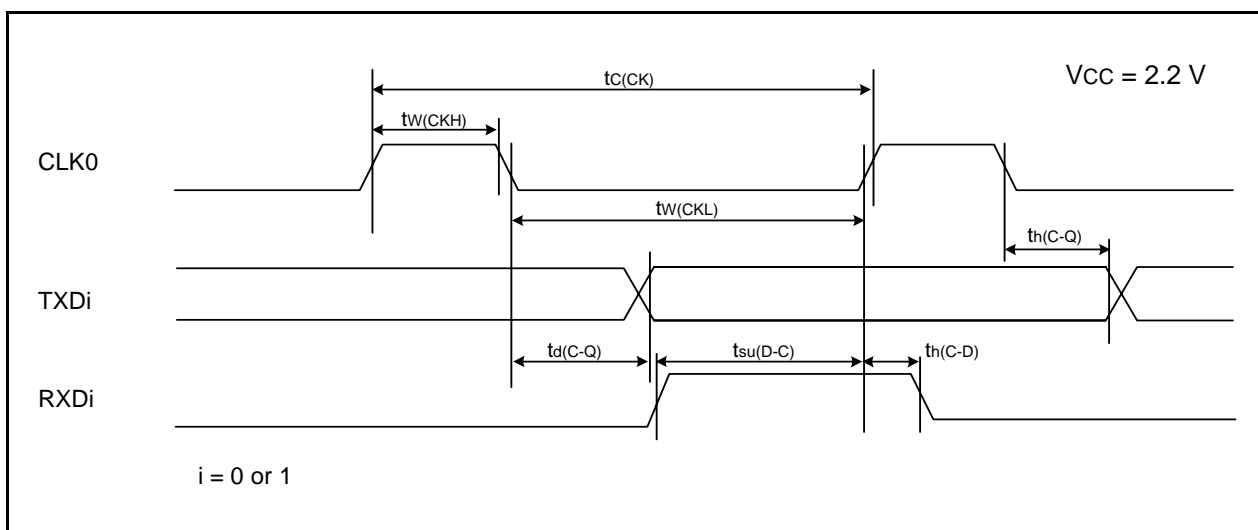
**Figure 5.15 External Interrupt \overline{INTi} Input Timing Diagram when Vcc = 3 V**

Table 5.32 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	800	—	ns
$t_{w(CKH)}$	CLK0 input "H" width	400	—	ns
$t_{w(CKL)}$	CLK0 input "L" width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

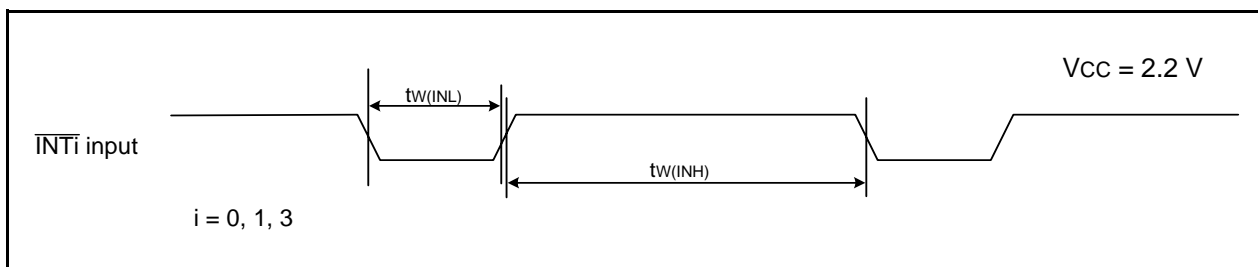
i = 0 or 1

**Figure 5.18 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.33 External Interrupt \overline{INTi} (i = 0, 1, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INTi} input "H" width	1000 ⁽¹⁾	—	ns
$t_{w(INL)}$	\overline{INTi} input "L" width	1000 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.19 External Interrupt \overline{INTi} Input Timing Diagram when Vcc = 2.2 V**

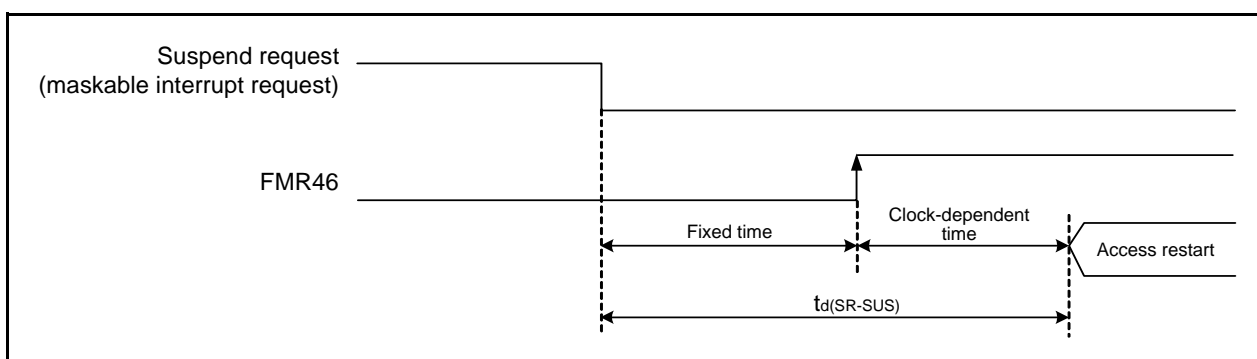


Figure 5.21 Time delay until Suspend

Table 5.39 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det1}	Voltage detection level ^(2, 4)		2.70	2.85	3.0	V
t _d (V _{det1} -A)	Voltage monitor 1 reset generation time ⁽⁵⁾		—	40	200	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, V _{CC} = 5.0 V	—	0.6	—	μA
t _d (E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs
V _{ccmin}	MCU operating voltage minimum value		2.70	—	—	V

NOTES:

1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version).
2. Hold V_{det2} > V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.
5. Time until the voltage monitor 1 reset is generated after the voltage passes V_{det1} when V_{CC} falls. When using the digital filter, its sampling time is added to t_d(V_{det1}-A). When using the voltage monitor 1 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det1} when the power supply falls.

Table 5.40 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det2}	Voltage detection level ⁽²⁾		3.3	3.6	3.9	V
t _d (V _{det2} -A)	Voltage monitor 2 reset/interrupt request generation time ^(3, 5)		—	40	200	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, V _{CC} = 5.0 V	—	0.6	—	μA
t _d (E-A)	Waiting time until voltage detection circuit operation starts ⁽⁴⁾		—	—	100	μs

NOTES:

1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version).
2. Hold V_{det2} > V_{det1}.
3. Time until the voltage monitor 2 reset/interrupt request is generated after the voltage passes V_{det2}.
4. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
5. When using the digital filter, its sampling time is added to t_d(V_{det2}-A). When using the voltage monitor 2 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det2} when the power supply falls.

Table 5.41 Power-on Reset Circuit, Voltage Monitor 1 Reset Electrical Characteristics⁽³⁾

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{por1}	Power-on reset valid voltage ⁽⁴⁾		–	–	0.1	V
V _{por2}	Power-on reset or voltage monitor 1 reset valid voltage		0	–	V _{det1}	V
tr _{th}	External power V _{CC} rise gradient	V _{CC} ≤ 3.6 V	20 ⁽²⁾	–	–	mV/msec
		V _{CC} > 3.6 V	20 ⁽²⁾	–	2,000	mV/msec

NOTES:

1. The measurement condition is T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. This condition (the minimum value of external power V_{CC} rise gradient) does not apply if V_{por2} ≥ 1.0 V.
3. To use the power-on reset function, enable voltage monitor 1 reset by setting the LVD1ON bit in the OFS register to 0, the VW1C0 and VW1C6 bits in the VW1C register to 1 respectively, and the VCA26 bit in the VCA2 register to 1.
4. tw_(por1) indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain tw_(por1) for 30 s or more if -20°C ≤ T_{opr} ≤ 125°C, maintain tw_(por1) for 3,000 s or more if -40°C ≤ T_{opr} < -20°C.

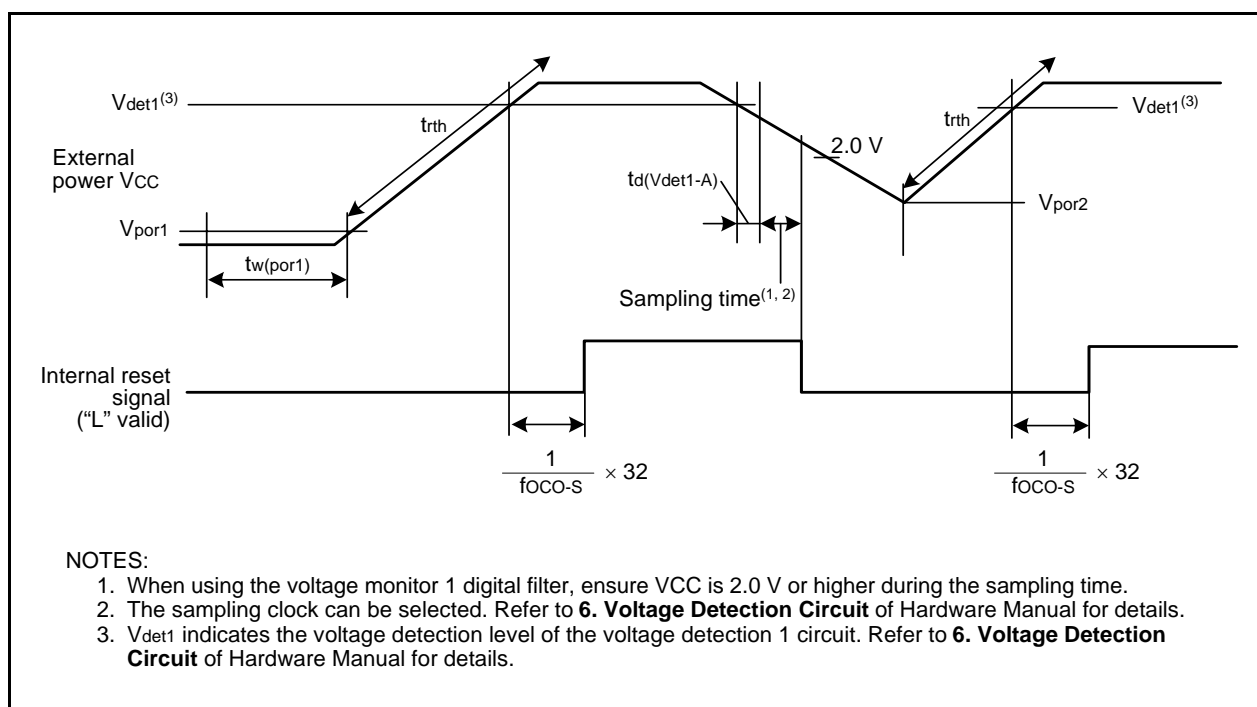
**Figure 5.22 Reset Circuit Electrical Characteristics**

Table 5.46 Timing Requirements of I²C bus Interface⁽¹⁾

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12t _{CYC} + 600 ⁽²⁾	–	–	ns
t _{SCLH}	SCL input “H” width		3t _{CYC} + 300 ⁽²⁾	–	–	ns
t _{SCLL}	SCL input “L” width		5t _{CYC} + 500 ⁽²⁾	–	–	ns
t _{sf}	SCL, SDA input fall time		–	–	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		–	–	1t _{CYC} ⁽²⁾	ns
t _{BUF}	SDA input bus-free time		5t _{CYC} ⁽²⁾	–	–	ns
t _{STAH}	Start condition input hold time		3t _{CYC} ⁽²⁾	–	–	ns
t _{STAS}	Retransmit start condition input setup time		3t _{CYC} ⁽²⁾	–	–	ns
t _{STOP}	Stop condition input setup time		3t _{CYC} ⁽²⁾	–	–	ns
t _{SDAS}	Data input setup time		1t _{CYC} + 20 ⁽²⁾	–	–	ns
t _{SDAH}	Data input hold time		0	–	–	ns

NOTES:

1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. 1t_{CYC} = 1/f₁(s)

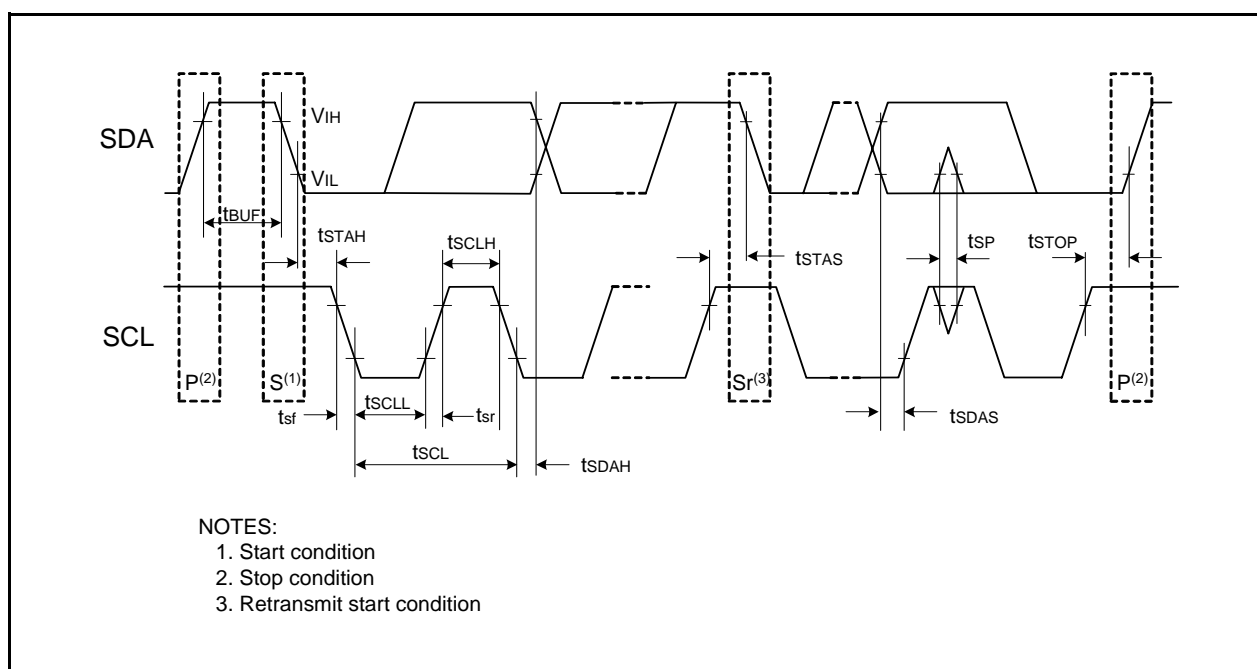
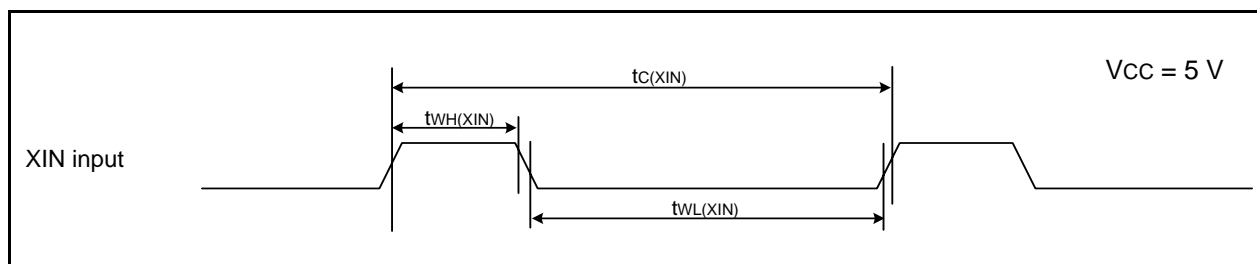
**Figure 5.26 I/O Timing of I²C bus Interface**

Table 5.48 Electrical Characteristics (2) [V_{CC} = 5 V]
(T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.)

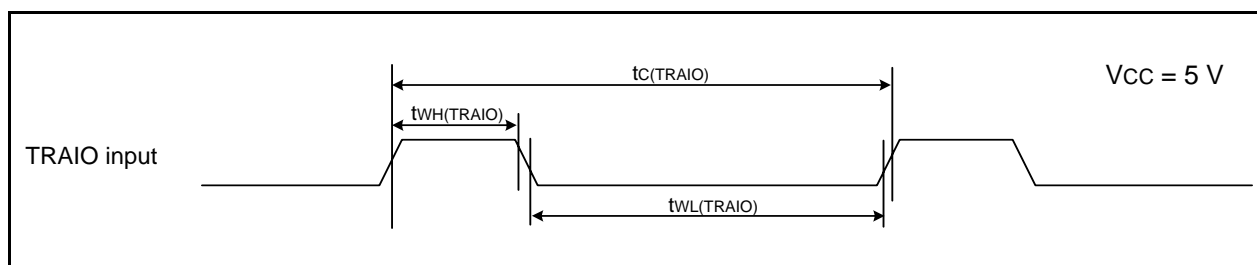
Symbol	Parameter	Condition	Standard			Unit	
			Min.	Typ.	Max.		
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	10	17	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	9	15	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	6	—	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	5	—	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	4	—	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.5	—	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz (J version) Low-speed on-chip oscillator on = 125 kHz No division	—	10	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz (J version) Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	4	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	5.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.5	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	—	130	300	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	25	75	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	23	60	μA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	0.8	3.0	μA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	1.2	—	μA
			XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	4.0	—	μA

Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 5\text{ V}$]****Table 5.49 XIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input "H" width	25	–	ns
$t_{WL(XIN)}$	XIN input "L" width	25	–	ns

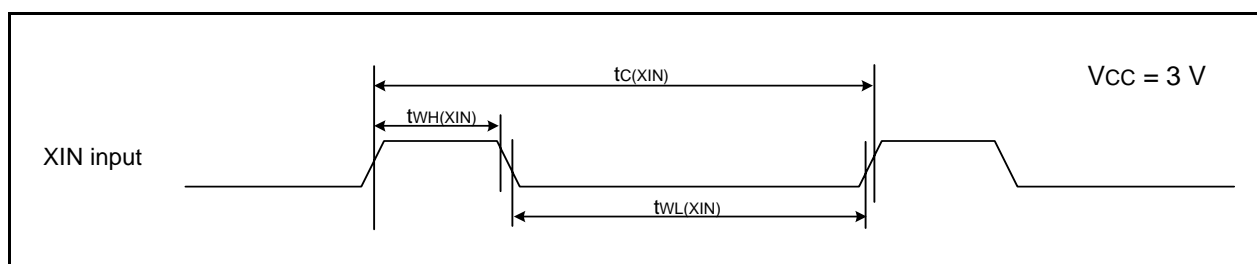
**Figure 5.27 XIN Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.50 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	40	–	ns

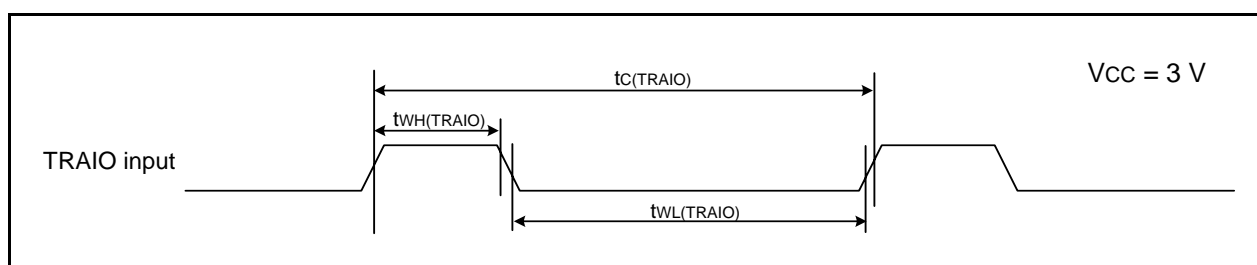
**Figure 5.28 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 3\text{ V}$]****Table 5.55 XIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input "H" width	40	–	ns
$t_{WL(XIN)}$	XIN input "L" width	40	–	ns

**Figure 5.31 XIN Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.56 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	120	–	ns

**Figure 5.32 TRAIO Input Timing Diagram when $V_{CC} = 3\text{ V}$**

REVISION HISTORY	R8C/28 Group, R8C/29 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.10	Nov 14, 2005	–	First Edition issued
0.30	Feb 28, 2006	all pages	“J, K version” added
		1	1.1 Applications revised
		2	Table 1.1 Functions and Specifications for R8C/28 Group revised
		3	Table 1.2 Functions and Specifications for R8C/29 Group revised
		4	Figure 1.1 Block Diagram; NOTE3 added
		5	Table 1.3 Product Information for R8C/28 Group and Figure 1.2 Type Number, Memory Size, and Package of R8C/28 Group revised
		6	Table 1.4 Product Information for R8C/29 Group and Figure 1.3 Type Number, Memory Size, and Package of R8C/29 Group revised
		7	Figure 1.4 Pin Assignments (Top View); NOTE3 added
		8	Table 1.5 Pin Functions revised
		9	Table 1.6 Pin Name Information by Pin Number; “XOUT” → “XOUT/XCOUT”, “XIN” → “XIN/XCIN” revised and NOTE2 added
		13	Figure 3.1 Memory Map of R8C/28 Group; “R5F21284JSP, R5F21284KSP” added
		14	Figure 3.2 Memory Map of R8C/29 Group; “R5F21294JSP, R5F21294KSP” added
		15	Table 4.1 SFR Information (1); NOTE6 added
		18	Table 4.4 SFR Information (4); 00FEh: “DRR” → “P1DRR” symbol name revised
		22 to 66	5. Electrical Characteristics added
0.40	Mar 29, 2006	2	Table 1.1 Functions and Specifications for R8C/28 Group revised
		3	Table 1.2 Functions and Specifications for R8C/29 Group revised
		15	Table 4.1 SFR Information (1); - 0032h, 0036h, 0038h revised - NOTES 2 to 6 revised and NOTES 7 to 8 added
		19	Table 4.5 SFR Information (5); NOTE2 added
0.50	Apr 27, 2006	18	Table 4.4; 00FDh: revised
		46	Table 5.35; System clock Conditions: revised
1.00	Nov 08, 2006	All pages	“PRELIMINARY” deleted
		1	1 “J and K versions are under development...notice.” added
		2	Table 1.1 revised
		3	Table 1.2 revised
		4	Figure 1.1 revised
		5	Table 1.3 revised
		6	Table 1.4 revised

Notes:

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