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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, LINbus, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21292sdsp-w4">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21292sdsp-w4</a>

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## 1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C CPU core, and are packaged in a 20-pin molded-plastic LSSOP. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.

Furthermore, the R8C/29 Group has on-chip data flash (1 KB  $\times$  2 blocks).

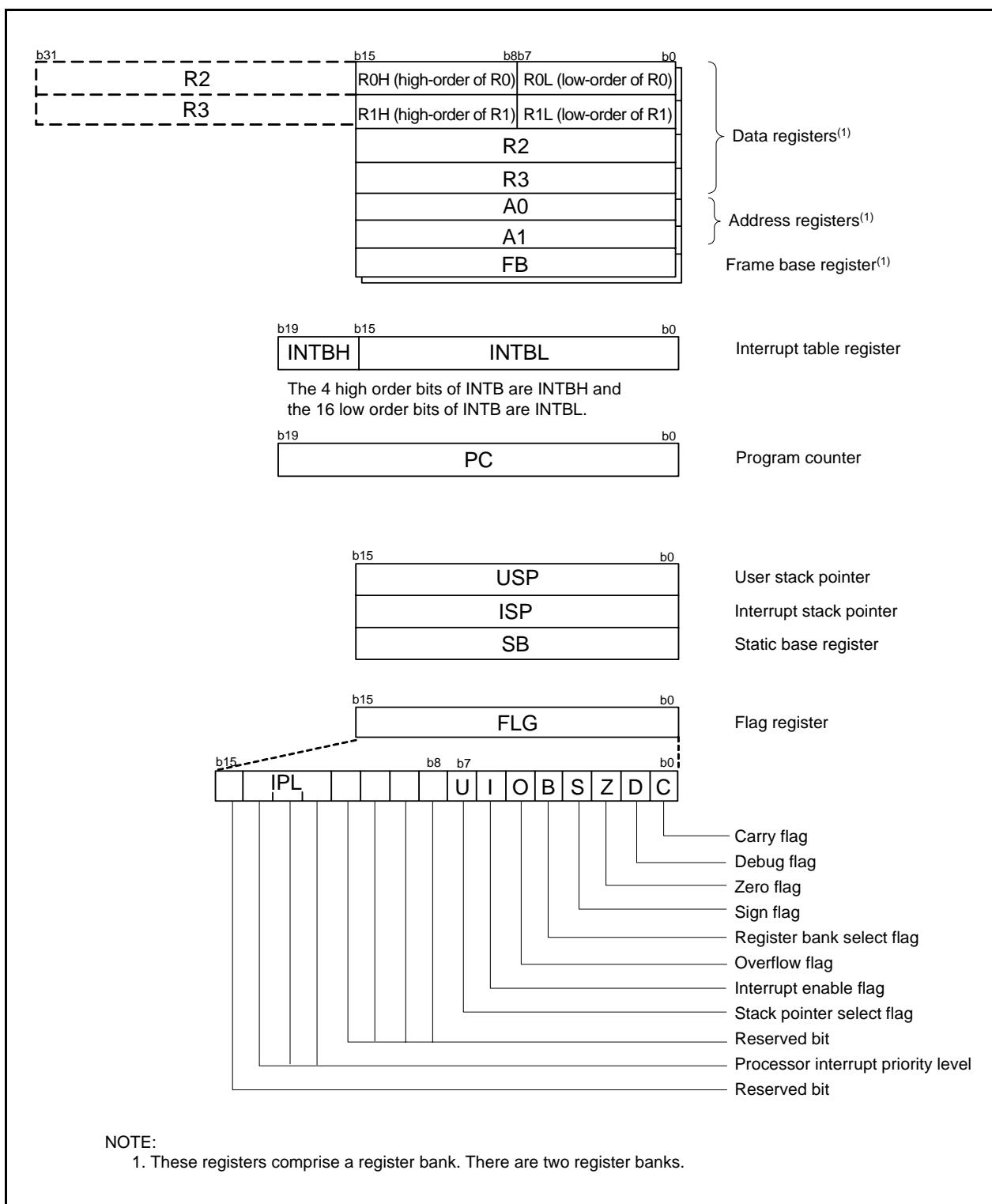
The difference between the R8C/28 Group and R8C/29 Group is only the presence or absence of data flash. Their peripheral functions are the same.

### 1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer products, automotive, etc.

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



**Figure 2.1 CPU Registers**

**Table 4.4 SFR Information (4)<sup>(1)</sup>**

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h			
00E1h	Port P1 Register	P1	00h
00E2h			
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	00h
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	00h
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h	Pin Select Register 1	PINSR1	00h
00F6h	Pin Select Register 2	PINSR2	00h
00F7h	Pin Select Register 3	PINSR3	00h
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	00h
00FEh	Port P1 Drive Capacity Control Register <sup>(2)</sup>	P1DRR	00h
00FFh			

X: Undefined

## NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. In J, K version these regions are reserved. Do not access locations in these regions.

**Table 4.6 SFR Information (6)<sup>(1)</sup>**

Address	Register	Symbol	After reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

**Table 5.4 Flash Memory (Program ROM) Electrical Characteristics**

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance <sup>(2)</sup>	R8C/28 Group	100 <sup>(3)</sup>	–	–	times
		R8C/29 Group	1,000 <sup>(3)</sup>	–	–	times
–	Byte program time		–	50	400	μs
–	Block erase time		–	0.4	9	s
t <sub>d</sub> (SR-SUS)	Time delay from suspend request until suspend		–	–	97 + CPU clock × 6 cycles	μs
–	Interval from erase start/restart until following suspend request		650	–	–	μs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycles	μs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time <sup>(7)</sup>	Ambient temperature = 55°C	20	–	–	year

**NOTES:**

1. V<sub>CC</sub> = 2.7 to 5.5 V at T<sub>opr</sub> = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance  
The programming and erasure endurance is defined on a per-block basis.  
If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.  
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

**Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics<sup>(4)</sup>**

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance <sup>(2)</sup>		10,000 <sup>(3)</sup>	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	50	400	μs
—	Byte program time (program/erase endurance > 1,000 times)		—	65	—	μs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	9	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	—	s
t <sub>d</sub> (SR-SUS)	Time delay from suspend request until suspend		—	—	97 + CPU clock × 6 cycles	μs
—	Interval from erase start/restart until following suspend request		650	—	—	μs
—	Interval from program start/restart until following suspend request		0	—	—	ns
—	Time from suspend until program/erase restart		—	—	3 + CPU clock × 4 cycles	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		2.2	—	5.5	V
—	Program, erase temperature		-20 <sup>(8)</sup>	—	85	°C
—	Data hold time <sup>(9)</sup>	Ambient temperature = 55°C	20	—	—	year

**NOTES:**

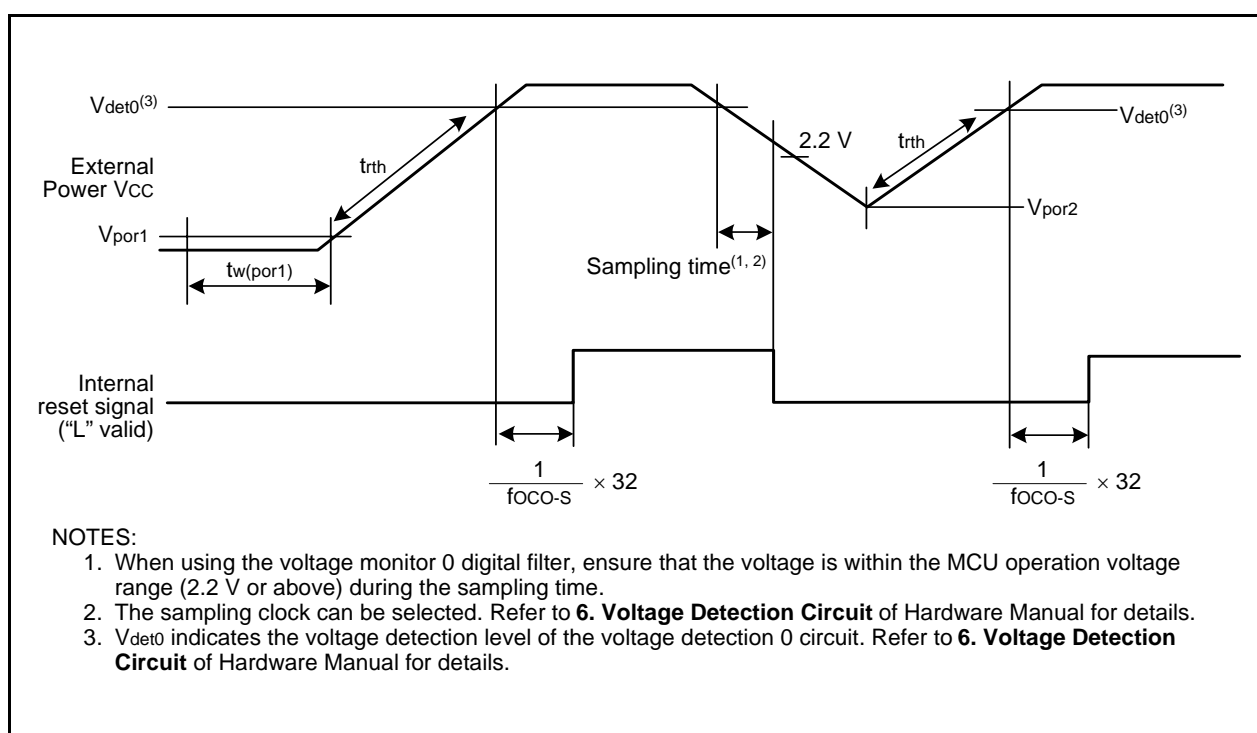
1. V<sub>CC</sub> = 2.7 to 5.5 V at T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance  
The programming and erasure endurance is defined on a per-block basis.  
If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.  
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. -40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

**Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics<sup>(3)</sup>**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>por1</sub>	Power-on reset valid voltage <sup>(4)</sup>		–	–	0.1	V
V <sub>por2</sub>	Power-on reset or voltage monitor 0 reset valid voltage		0	–	V <sub>det0</sub>	V
tr <sub>th</sub>	External power V <sub>cc</sub> rise gradient <sup>(2)</sup>		20	–	–	mV/msec

**NOTES:**

1. The measurement condition is T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V<sub>cc</sub> rise gradient) does not apply if V<sub>cc</sub> ≥ 1.0 V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. tw<sub>(por1)</sub> indicates the duration the external power V<sub>cc</sub> must be held below the effective voltage (V<sub>por1</sub>) to enable a power on reset. When turning on the power for the first time, maintain tw<sub>(por1)</sub> for 30 s or more if -20°C ≤ T<sub>opr</sub> ≤ 85°C, maintain tw<sub>(por1)</sub> for 3,000 s or more if -40°C ≤ T<sub>opr</sub> < -20°C.

**Figure 5.3 Reset Circuit Electrical Characteristics**

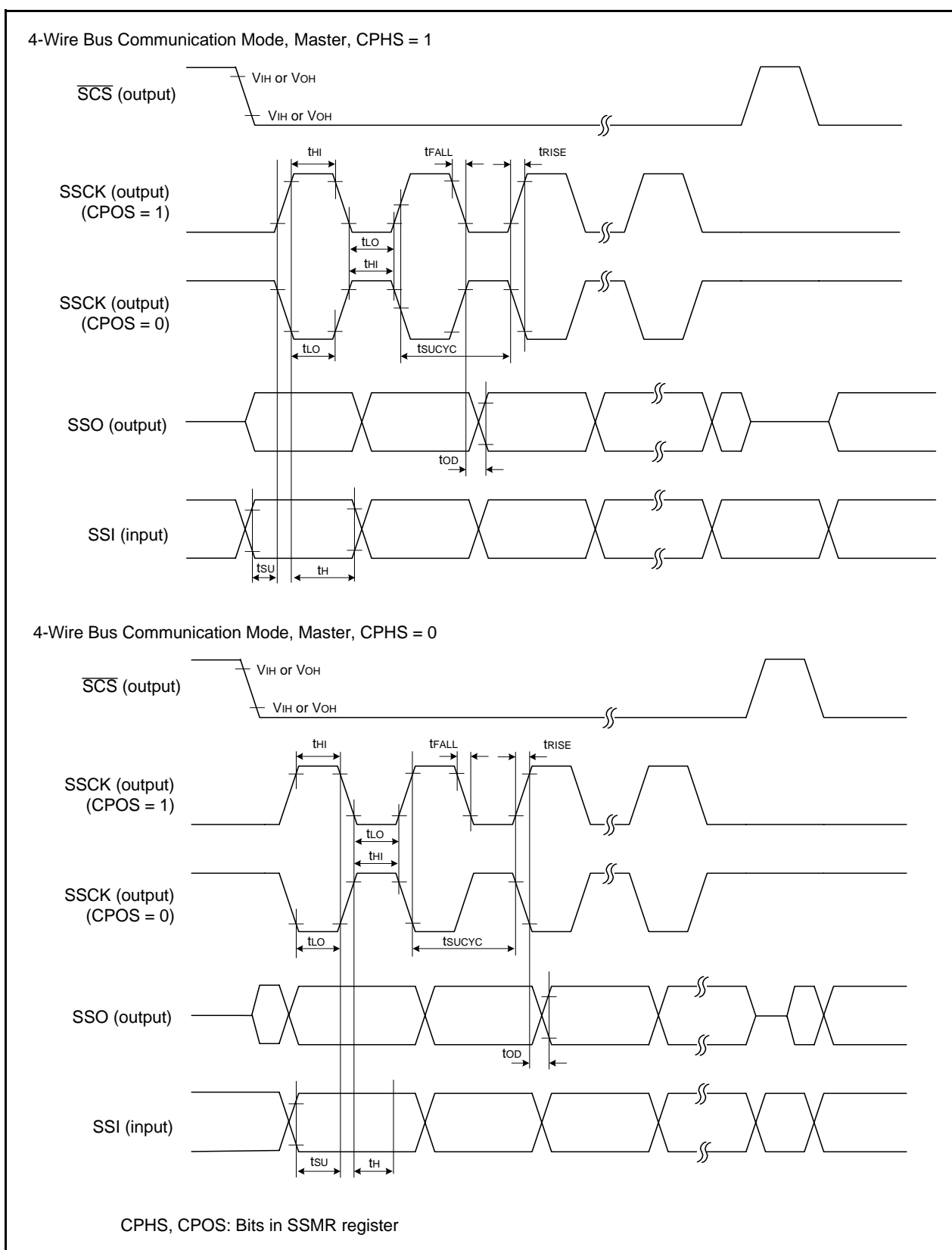


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

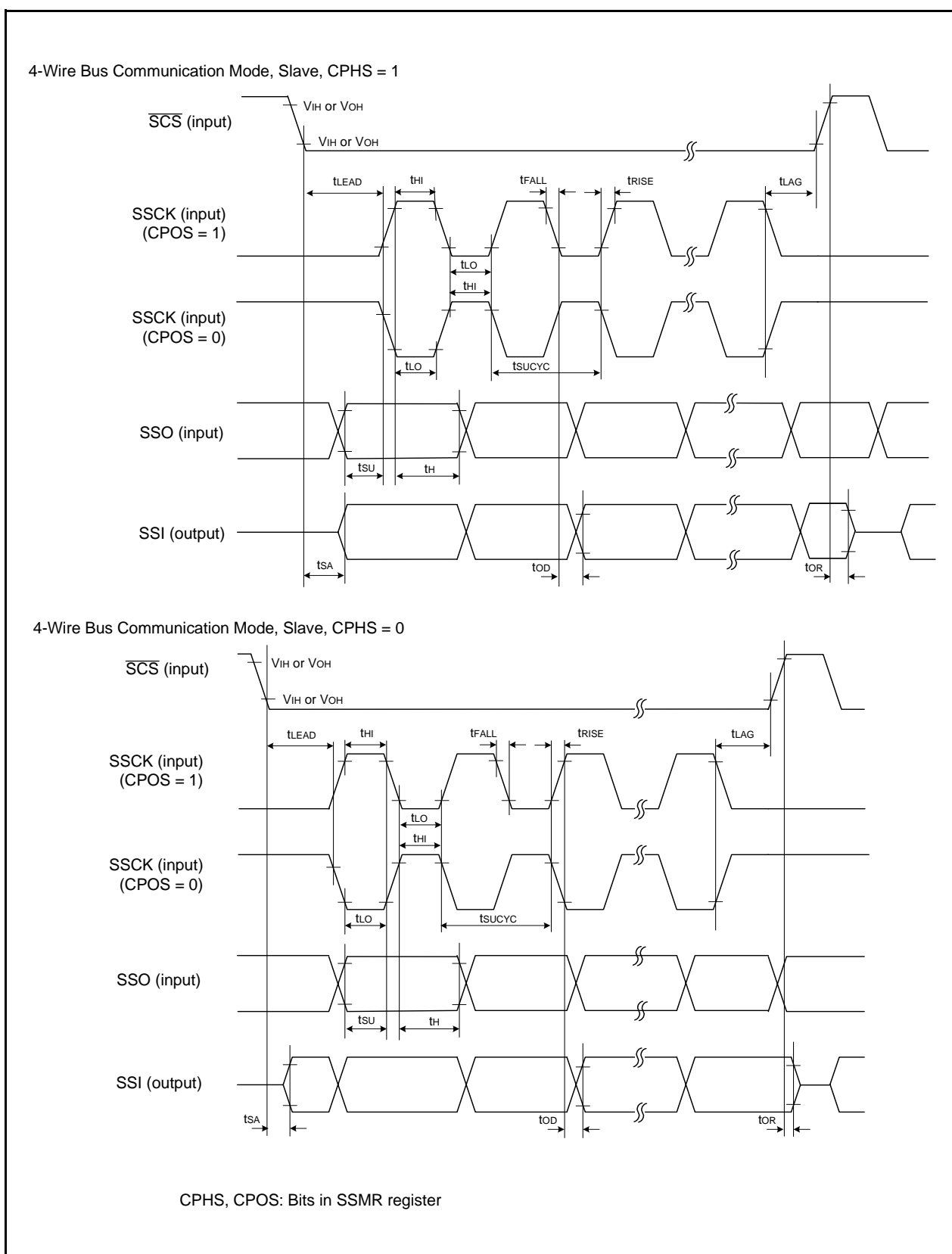


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

**Table 5.22 Electrical Characteristics (3) [V<sub>CC</sub> = 3 V]**

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V <sub>OH</sub>	Output "H" voltage	Except P1_0 to P1_7, XOUT	I <sub>OH</sub> = -1 mA		V <sub>CC</sub> - 0.5	—	V <sub>CC</sub>	V
		P1_0 to P1_7	Drive capacity HIGH	I <sub>OH</sub> = -5 mA	V <sub>CC</sub> - 0.5	—	V <sub>CC</sub>	V
			Drive capacity LOW	I <sub>OH</sub> = -1 mA	V <sub>CC</sub> - 0.5	—	V <sub>CC</sub>	V
		XOUT	Drive capacity HIGH	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> - 0.5	—	V <sub>CC</sub>	V
			Drive capacity LOW	I <sub>OH</sub> = -50 μA	V <sub>CC</sub> - 0.5	—	V <sub>CC</sub>	V
V <sub>OL</sub>	Output "L" voltage	Except P1_0 to P1_7, XOUT	I <sub>OL</sub> = 1 mA		—	—	0.5	V
		P1_0 to P1_7	Drive capacity HIGH	I <sub>OL</sub> = 5 mA	—	—	0.5	V
			Drive capacity LOW	I <sub>OL</sub> = 1 mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	I <sub>OL</sub> = 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I <sub>OL</sub> = 50 μA	—	—	0.5	V
V <sub>T+</sub> -V <sub>T-</sub>	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO			0.1	0.3	—	V
		RESET			0.1	0.4	—	V
I <sub>IH</sub>	Input "H" current		V <sub>I</sub> = 3 V, V <sub>CC</sub> = 3V		—	—	4.0	μA
I <sub>IL</sub>	Input "L" current		V <sub>I</sub> = 0 V, V <sub>CC</sub> = 3V		—	—	-4.0	μA
R <sub>PULLUP</sub>	Pull-up resistance		V <sub>I</sub> = 0 V, V <sub>CC</sub> = 3V		66	160	500	kΩ
R <sub>FXIN</sub>	Feedback resistance	XIN			—	3.0	—	MΩ
R <sub>FXCIN</sub>	Feedback resistance	XCIN			—	18	—	MΩ
V <sub>RAM</sub>	RAM hold voltage		During stop mode		1.8	—	—	V

**NOTE:**

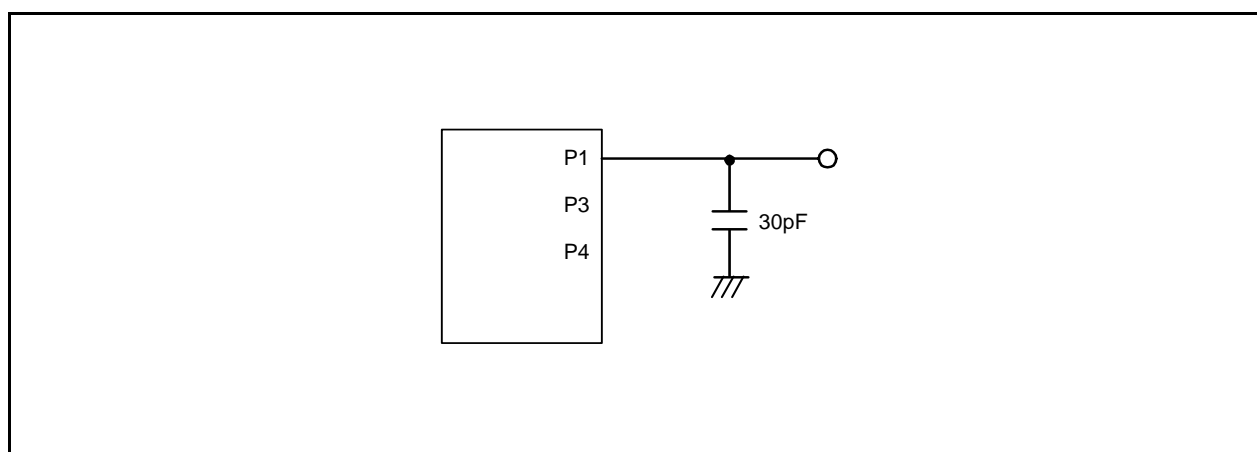
- V<sub>CC</sub> = 2.7 to 3.3 V at T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

**Table 5.36 A/D Converter Characteristics**

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		$V_{ref} = AV_{CC}$	—	—	10	Bits
—	Absolute accuracy	10-bit mode	$\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = AV_{CC} = 5.0 \text{ V}$	—	—	$\pm 3$	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = AV_{CC} = 5.0 \text{ V}$	—	—	$\pm 2$	LSB
		10-bit mode	$\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = AV_{CC} = 3.3 \text{ V}$	—	—	$\pm 5$	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = AV_{CC} = 3.3 \text{ V}$	—	—	$\pm 2$	LSB
$R_{ladder}$	Resistor ladder		$V_{ref} = AV_{CC}$	10	—	40	$k\Omega$
$t_{conv}$	Conversion time	10-bit mode	$\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = AV_{CC} = 5.0 \text{ V}$	3.3	—	—	$\mu\text{s}$
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$ , $V_{ref} = AV_{CC} = 5.0 \text{ V}$	2.8	—	—	$\mu\text{s}$
$V_{ref}$	Reference voltage			2.7	—	$AV_{CC}$	V
$V_{IA}$	Analog input voltage <sup>(2)</sup>			0	—	$AV_{CC}$	V
—	A/D operating clock frequency	Without sample and hold		0.25	—	10	MHz
		With sample and hold		1	—	10	MHz

## NOTES:

1.  $AV_{CC} = 2.7$  to  $5.5 \text{ V}$  at  $T_{opr} = -40$  to  $85^\circ\text{C}$  (J version) /  $-40$  to  $125^\circ\text{C}$  (K version), unless otherwise specified.
2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

**Figure 5.20 Ports P1, P3, and P4 Timing Measurement Circuit**

**Table 5.38 Flash Memory (Data flash Block A, Block B) Electrical Characteristics<sup>(4)</sup>**

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance <sup>(2)</sup>		10,000 <sup>(3)</sup>	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	50	400	μs
—	Byte program time (program/erase endurance > 1,000 times)		—	65	—	μs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	9	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	—	s
t <sub>d</sub> (SR-SUS)	Time delay from suspend request until suspend		—	—	97 + CPU clock × 6 cycles	μs
—	Interval from erase start/restart until following suspend request		650	—	—	μs
—	Interval from program start/restart until following suspend request		0	—	—	ns
—	Time from suspend until program/erase restart		—	—	3 + CPU clock × 4 cycles	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		2.7	—	5.5	V
—	Program, erase temperature		-40	—	85 <sup>(8)</sup>	°C
—	Data hold time <sup>(9)</sup>	Ambient temperature = 55°C	20	—	—	year

**NOTES:**

1. V<sub>CC</sub> = 2.7 to 5.5 V at T<sub>opr</sub> = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance  
The programming and erasure endurance is defined on a per-block basis.  
If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.  
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. 125°C for K version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

**Table 5.45 Timing Requirements of Clock Synchronous Serial I/O with Chip Select<sup>(1)</sup>**

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc <sup>(2)</sup>
tHI	SSCK clock "H" width			0.4	–	0.6	tsucyc
tLO	SSCK clock "L" width			0.4	–	0.6	tsucyc
tRISE	SSCK clock rising time	Master		–	–	1	tcyc <sup>(2)</sup>
		Slave		–	–	1	μs
tFALL	SSCK clock falling time	Master		–	–	1	tcyc <sup>(2)</sup>
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
tH	SSO, SSI data input hold time			1	–	–	tcyc <sup>(2)</sup>
tLEAD	$\overline{\text{SCS}}$ setup time	Slave		1tcyc + 50	–	–	ns
tLAG	$\overline{\text{SCS}}$ hold time	Slave		1tcyc + 50	–	–	ns
tOD	SSO, SSI data output delay time			–	–	1	tcyc <sup>(2)</sup>
tSA	SSI slave access time			–	–	1.5tcyc + 100	ns
tOR	SSI slave out open time			–	–	1.5tcyc + 100	ns

**NOTES:**

1.  $V_{CC} = 2.7$  to  $5.5$  V,  $V_{SS} = 0$  V at  $T_{opr} = -40$  to  $85^{\circ}\text{C}$  (J version) /  $-40$  to  $125^{\circ}\text{C}$  (K version), unless otherwise specified.
2.  $1\text{tcyc} = 1/f_1(\text{s})$

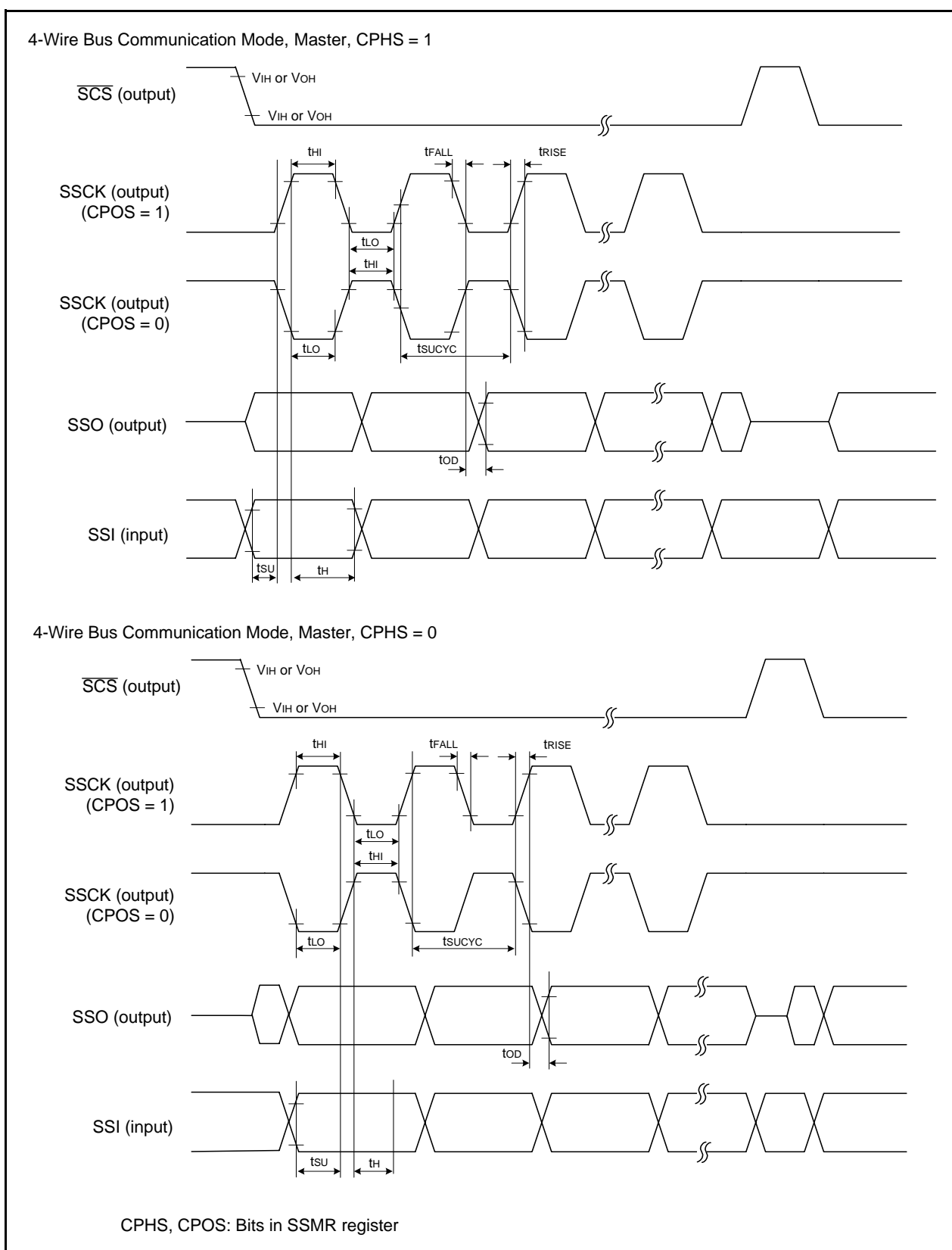


Figure 5.23 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

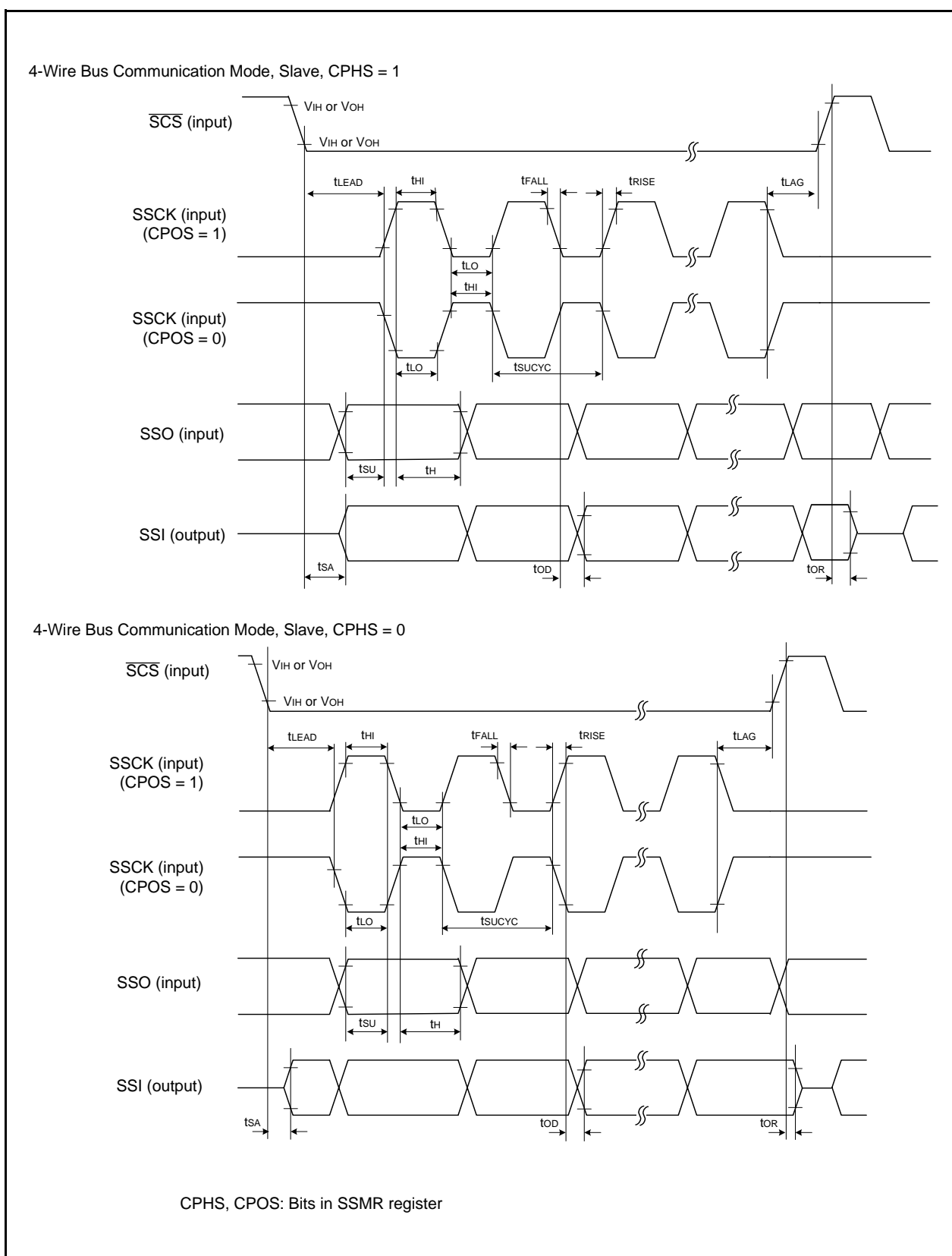


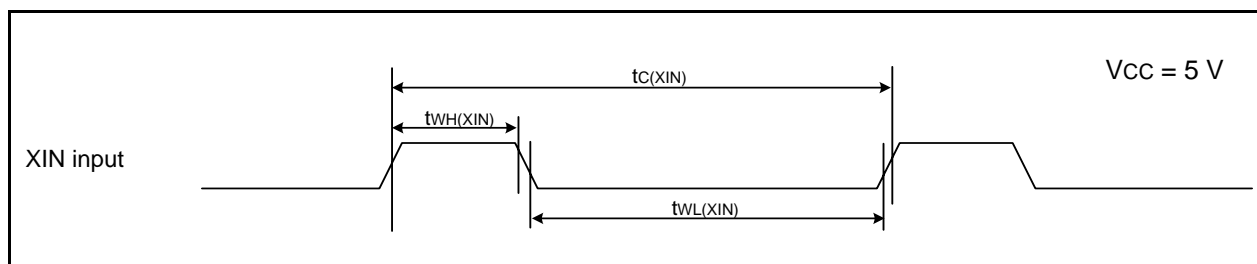
Figure 5.24 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

**Table 5.48 Electrical Characteristics (2) [Vcc = 5 V]**  
**(Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.)**

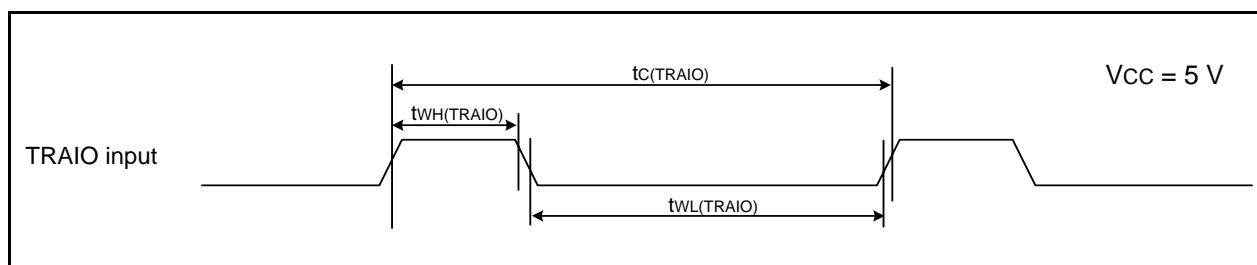
Symbol	Parameter	Condition			Standard			Unit
					Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	10	17	mA	
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	9	15	mA	
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	6	—	mA	
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	5	—	mA	
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	4	—	mA	
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.5	—	mA	
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz (J version) Low-speed on-chip oscillator on = 125 kHz No division	—	10	15	mA	
			XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz (J version) Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	4	—	mA	
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	5.5	10	mA	
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.5	—	mA	
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	—	130	300	μA	
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	25	75	μA	
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	23	60	μA	
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	0.8	3.0	μA	
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	1.2	—	μA	
			XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	4.0	—	μA	

**Timing Requirements****(Unless Otherwise Specified:  $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$  at  $T_{opr} = 25^{\circ}\text{C}$ ) [ $V_{CC} = 5\text{ V}$ ]****Table 5.49 XIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input "H" width	25	–	ns
$t_{WL(XIN)}$	XIN input "L" width	25	–	ns

**Figure 5.27 XIN Input Timing Diagram when  $V_{CC} = 5\text{ V}$** **Table 5.50 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	40	–	ns

**Figure 5.28 TRAIO Input Timing Diagram when  $V_{CC} = 5\text{ V}$**

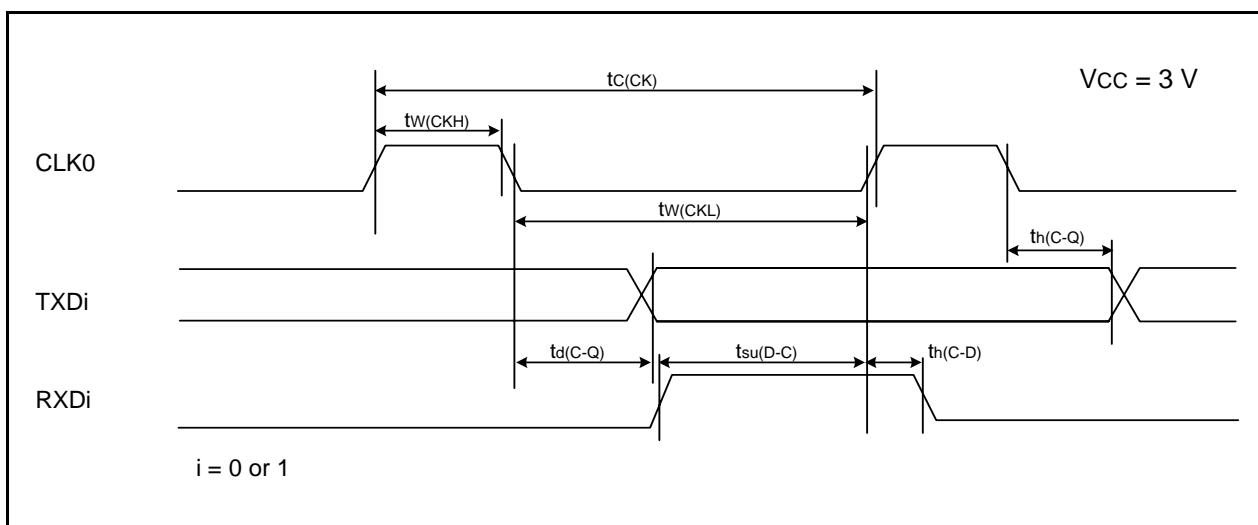
**Table 5.54 Electrical Characteristics (4) [V<sub>CC</sub> = 3 V]**  
**(T<sub>opr</sub> = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.)**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I <sub>CC</sub>	Power supply current (V <sub>CC</sub> = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V <sub>SS</sub>	High-speed clock mode	—	6	—	mA
		High-speed on-chip oscillator mode	—	2	—	mA
		High-speed on-chip oscillator mode	—	5	9	mA
		Low-speed on-chip oscillator mode	—	130	300	μA
		Wait mode	—	25	70	μA
		Stop mode	—	0.7	3.0	μA
		Stop mode	—	1.1	—	μA
		Stop mode	—	3.8	—	μA

**Table 5.57 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	—	ns
$t_{w(CKH)}$	CLK0 input "H" width	150	—	ns
$t_{w(CKL)}$	CLK0 Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

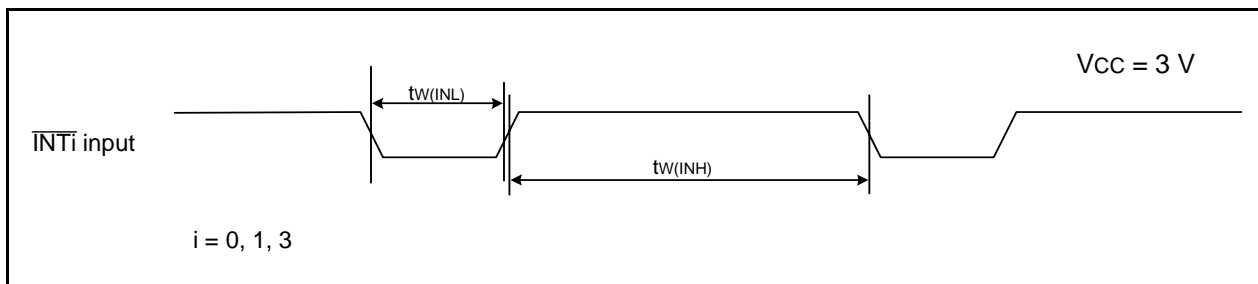
i = 0 or 1

**Figure 5.33 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.58 External Interrupt  $\overline{INTi}$  (i = 0, 1, 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	380 <sup>(1)</sup>	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	380 <sup>(2)</sup>	—	ns

**NOTES:**

1. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.34 External Interrupt  $\overline{INTi}$  Input Timing Diagram when Vcc = 3 V**