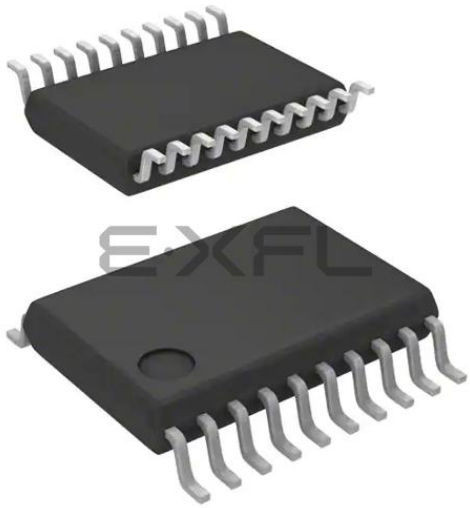

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21294ksp-u0

1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/28 Group and Table 1.2 outlines the Functions and Specifications for R8C/29 Group.

Table 1.1 Functions and Specifications for R8C/28 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) (other than K version) 62.5 ns (f(XIN) = 16 MHz, VCC = 3.0 to 5.5 V) (K version) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V) (N, D version)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to **Table 1.3 Product Information for R8C/28 Group**
Peripheral Functions	Ports	I/O ports: 13 pins, Input port: 3 pins
	LED drive ports	I/O ports: 8 pins (N, D version)
	Timers	Timer RA: 8 bits × 1 channel Timer RB: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer RC: 16 bits × 1 channel (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function (For J, K version, compare match function only.)
	Serial interfaces	1 channel (UART0): Clock synchronous serial I/O, UART 1 channel (UART1): UART
	Clock synchronous serial interface	1 channel I²C bus Interface(1) Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog timer	15 bits × 1 channel (with prescaler) Reset start selectable
	Interrupts	Internal: 15 sources (N, D version), Internal: 14 sources (J, K version) External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	3 circuits • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz) (N, D version) • Real-time clock (timer RE) (N, D version)
	Oscillation stop detection function	XIN clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip
Electrical Characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (N, D version)
	Current consumption (N, D version)	Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz) Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	100 times
Operating Ambient Temperature		-20 to 85°C (N version)
		-40 to 85°C (D, J version)(2), -40 to 125°C (K version)(2)
Package		20-pin molded-plastic LSSOP

NOTES:
1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D, K version if D, K version functions are to be used.

1.4 Product Information

Table 1.3 lists the Product Information for R8C/28 Group and Table 1.4 lists the Product Information for R8C/29 Group.

Table 1.3 Product Information for R8C/28 Group **Current of Sep. 2008**

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks	
R5F21282SNSP	8 Kbytes	512 bytes	PLSP0020JB-A	N version	
R5F21284SNSP	16 Kbytes	1 Kbyte	PLSP0020JB-A		
R5F21282SDSP	8 Kbytes	512 bytes	PLSP0020JB-A	D version	
R5F21284SDSP	16 Kbytes	1 Kbyte	PLSP0020JB-A		
R5F21284JSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	J version	
R5F21286JSP	32 Kbytes	1.5 Kbyte	PLSP0020JB-A		
R5F21284KSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	K version	
R5F21286KSP	32 Kbytes	1.5 Kbyte	PLSP0020JB-A		
R5F21282SNXXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	N version	Factory programming product(1)
R5F21284SNXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A		
R5F21282SDXXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	D version	
R5F21284SDXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A		
R5F21284JXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	J version	
R5F21286JXXXSP	32 Kbytes	1.5 Kbyte	PLSP0020JB-A		
R5F21284KXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	K version	
R5F21286KXXXSP	32 Kbytes	1.5 Kbyte	PLSP0020JB-A		

NOTE:
1. The user ROM is programmed before shipment.

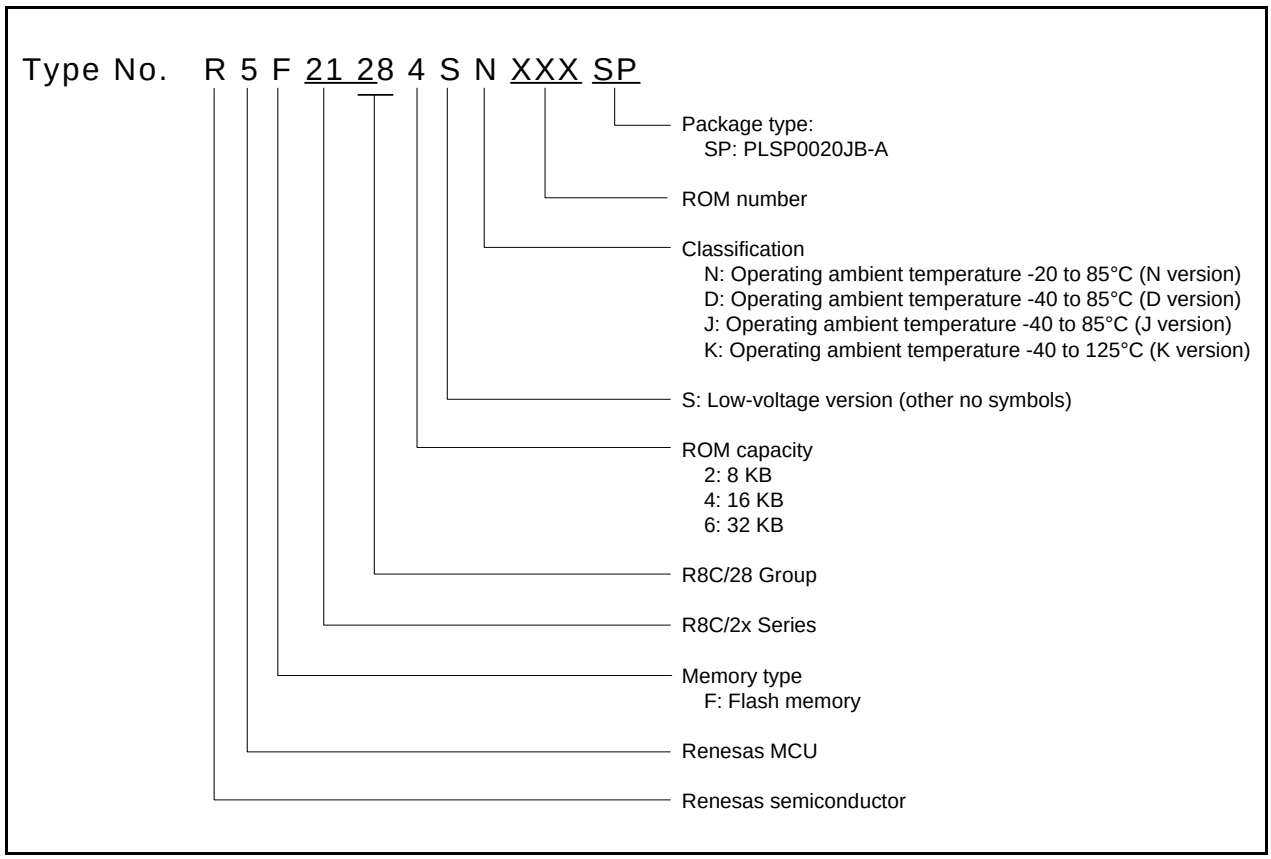
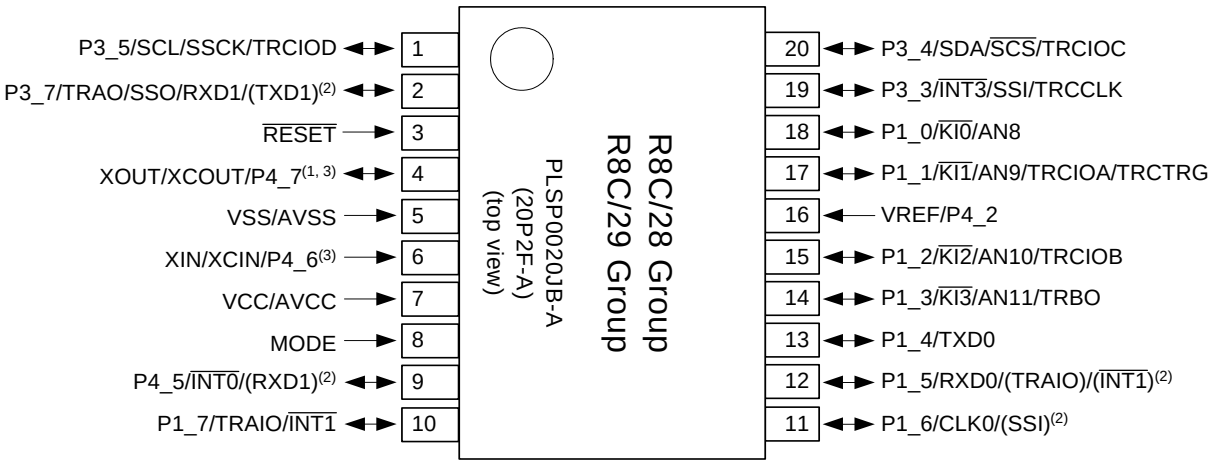


Figure 1.2 Type Number, Memory Size, and Package of R8C/28 Group

1.5 Pin Assignments

Figure 1.4 shows Pin Assignments (Top View).

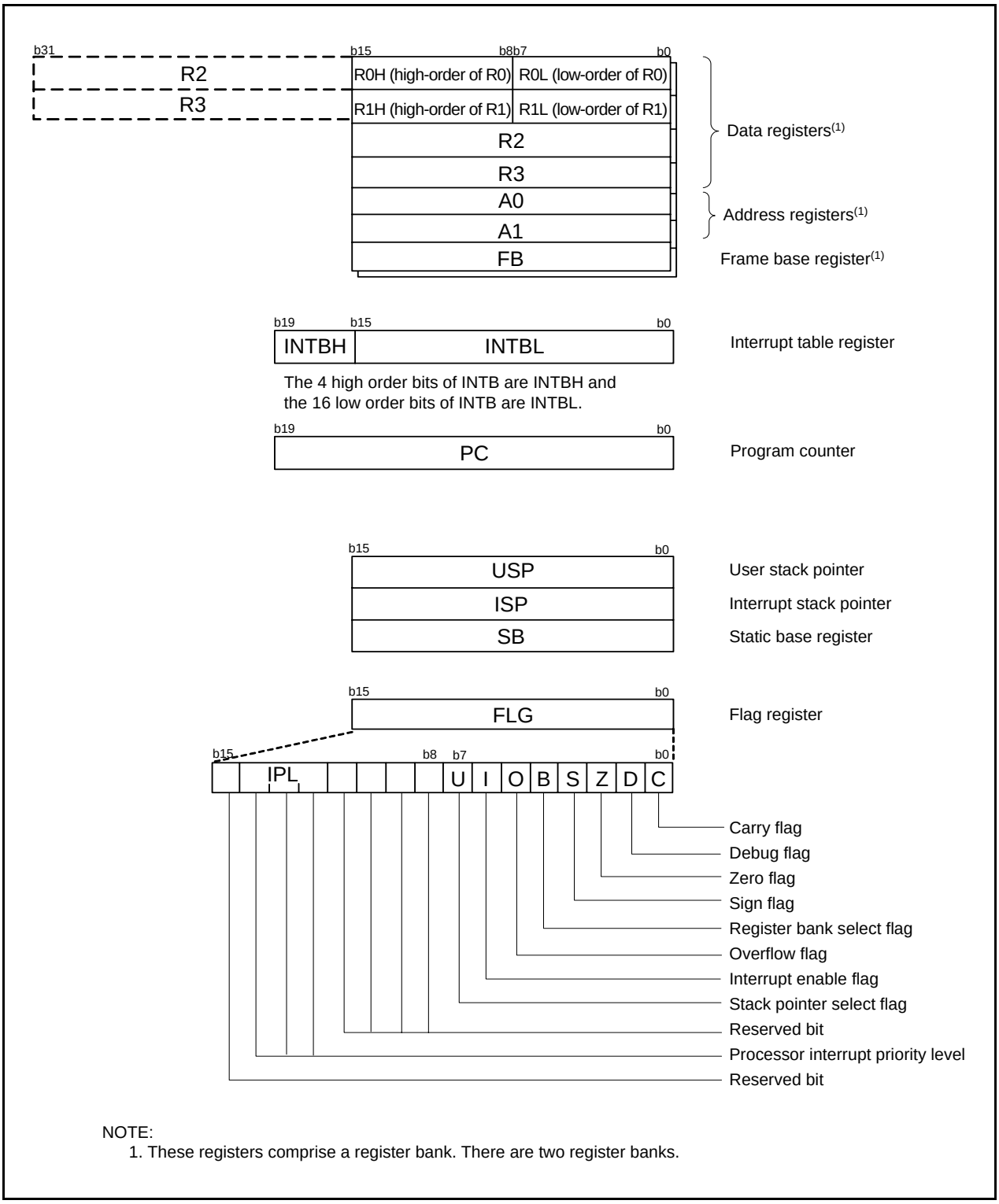


NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. XCIN, XCOUT can be used only for N or D version.
4. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.4 Pin Assignments (Top View)

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

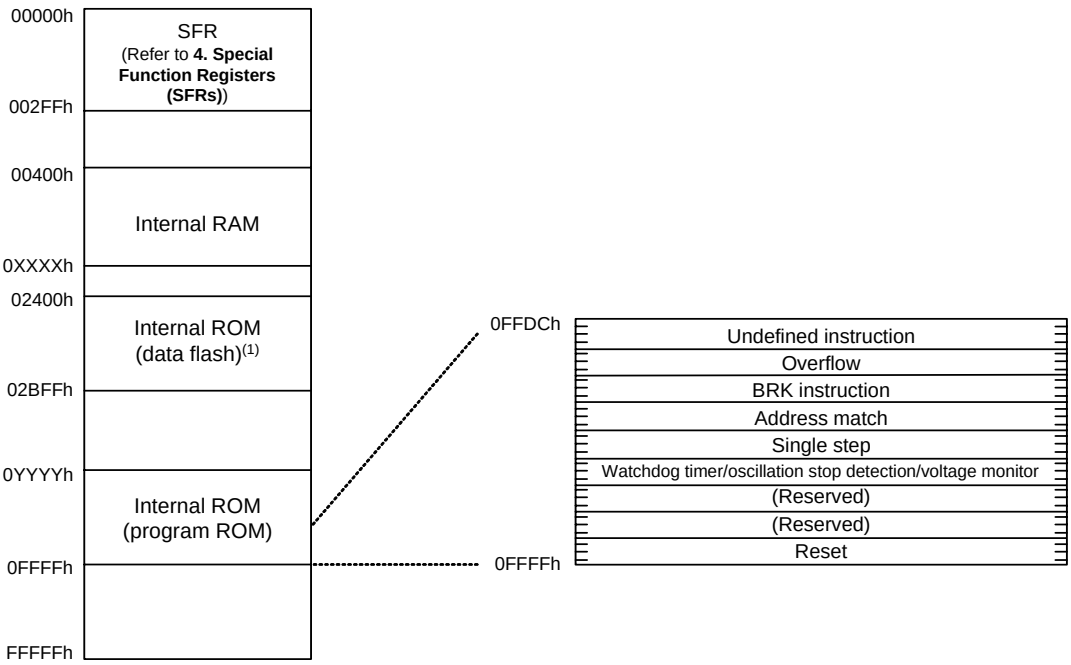


NOTE:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

3.2 R8C/29 Group

Figure 3.2 is a Memory Map of R8C/29 Group. The R8C/29 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F21292SNSP, R5F21292SDSP, R5F21292SNXXXSP, R5F21292SDXXXSP	8 Kbytes	0E000h	512 bytes	005FFh
R5F21294SNSP, R5F21294SDSP, R5F21294JSP, R5F21294KSP, R5F21294SNXXXSP, R5F21294SDXXXSP, R5F21294JXXXSP, R5F21294KXXXSP	16 Kbytes	0C000h	1 Kbyte	007FFh
R5F21296JSP, R5F21296KSP, R5F21296JXXXSP, R5F21296KXXXSP	32 Kbytes	08000h	1.5 Kbytes	009FFh

Figure 3.2 Memory Map of R8C/29 Group

Table 4.5 SFR Information (5)[1]

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register[2]	TREHR	00h
011Bh	Timer RE Day of Week Data Register[2]	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011111b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. In J, K version these regions are reserved. Do not access locations in these regions.

Table 4.7 SFR Information (7)(1)

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined

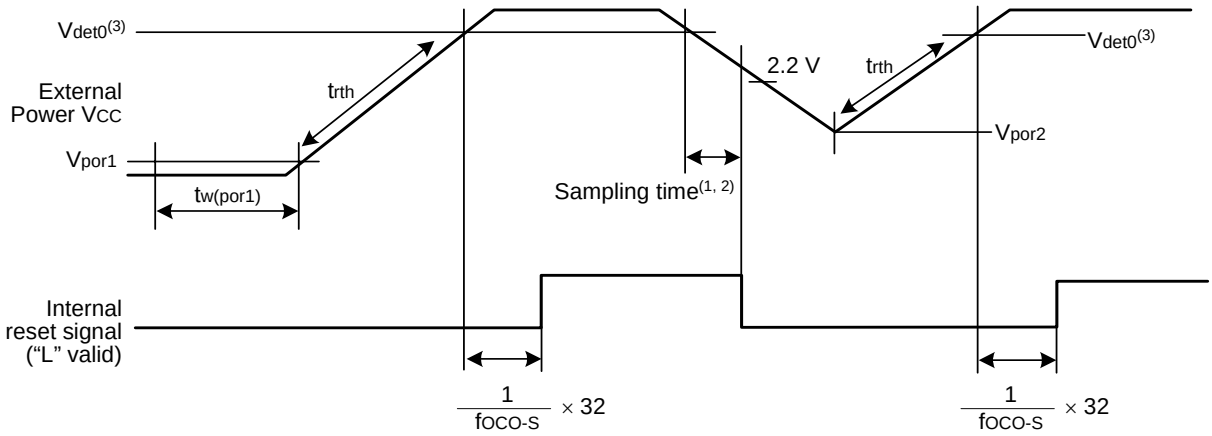
NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics(3)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage(4)		–	–	0.1	V
V_{por2}	Power-on reset or voltage monitor 0 reset valid voltage		0	–	V_{det0}	V
t_{rth}	External power V_{CC} rise gradient(2)		20	–	–	mV/msec

NOTES:
1. The measurement condition is T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if $V_{CC} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30 s or more if -20°C ≤ T_{opr} ≤ 85°C, maintain $t_{w(por1)}$ for 3,000 s or more if -40°C ≤ T_{opr} < -20°C.



NOTES:
1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
3. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 4.75 to 5.25 V 0°C ≤ T_{opr} ≤ 60°C(2)	39.2	40	40.8	MHz
		V_{CC} = 3.0 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(2)	38.8	40	41.2	MHz
		V_{CC} = 3.0 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(2)	38.4	40	41.6	MHz
		V_{CC} = 2.7 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(2)	38	40	42	MHz
		V_{CC} = 2.7 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(2)	37.6	40	42.4	MHz
		V_{CC} = 2.2 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(3)	35.2	40	44.8	MHz
		V_{CC} = 2.2 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(3)	34	40	46	MHz
		V_{CC} = 5.0 V ± 10% -20°C ≤ T_{opr} ≤ 85°C(2)	38.8	40	40.8	MHz
		V_{CC} = 5.0 V ± 10% -40°C ≤ T_{opr} ≤ 85°C(2)	38.4	40	40.8	MHz
	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register(4)	V_{CC} = 5.0 V, T_{opr} = 25°C	–	36.864	–	MHz
		V_{CC} = 3.0 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C	-3%	–	3%	%
–	Value in FRA1 register after reset		08h(3)	–	F7h(3)	–
–	Oscillation frequency adjustment unit of high-speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	–	+0.3	–	MHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	400	–	µA

NOTES:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.
3. These standard values show when the corrected value of the FRA6 register is written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	15	–	µA

NOTE:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

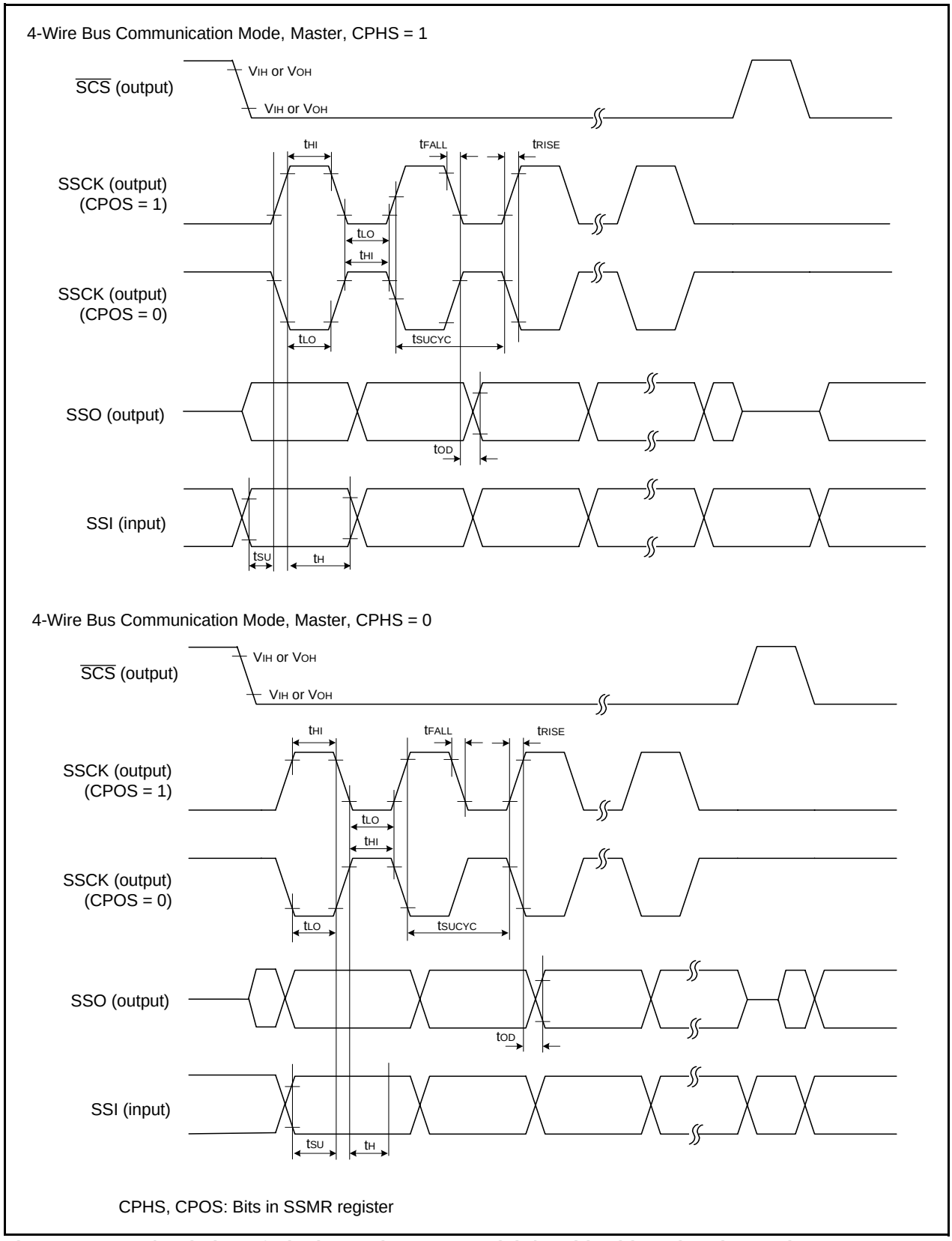


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

Table 5.14 Timing Requirements of I²C bus Interface(1)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC} + 600$(2)	–	–	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC} + 300$(2)	–	–	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC} + 500$(2)	–	–	ns
t_{sf}	SCL, SDA input fall time		–	–	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		–	–	$1t_{CYC}$(2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$(2)	–	–	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}$(2)	–	–	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{SDAS}	Data input setup time		$1t_{CYC} + 20$(2)	–	–	ns
t_{SDAH}	Data input hold time		0	–	–	ns

NOTES:
1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. $1t_{CYC} = 1/f1(s)$

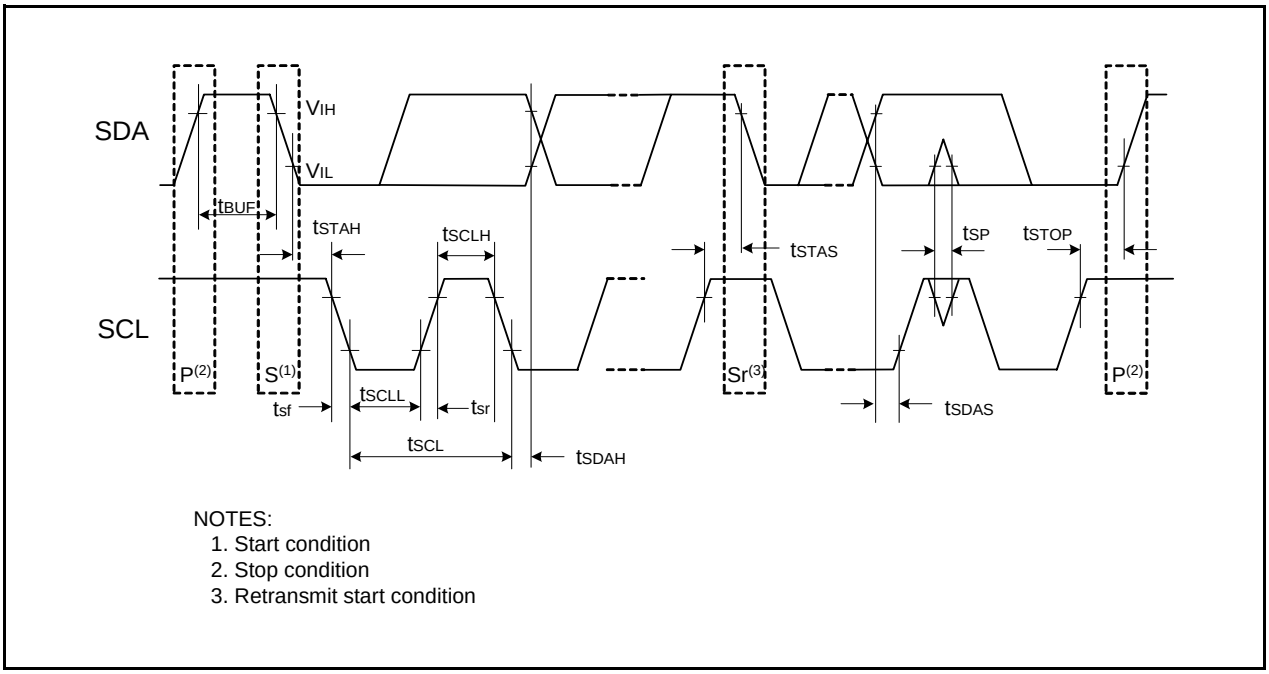


Figure 5.7 I/O Timing of I²C bus Interface

Table 5.17 Electrical Characteristics (3) [Vcc = 5 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are V_{SS}	Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	75	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	60	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	4.0	–	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	2.2	–	µA
		Stop mode	XIN clock off, T_{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.8	3.0	µA
			XIN clock off, T_{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.2	–	µA

Table 5.20 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	100	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

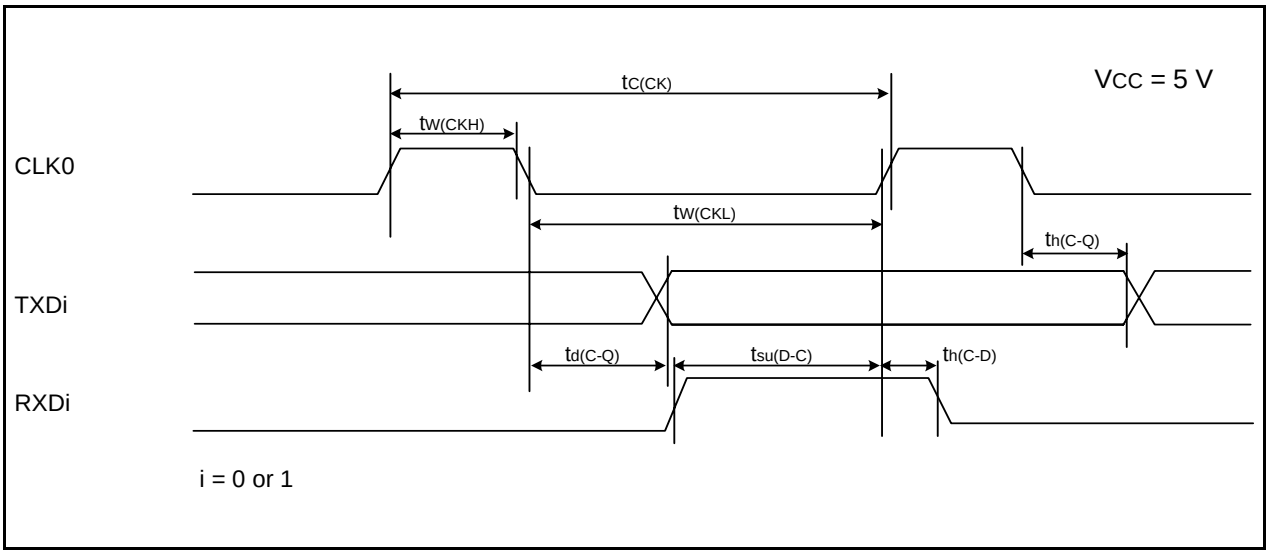


Figure 5.10 Serial Interface Timing Diagram when VCC = 5 V

Table 5.21 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

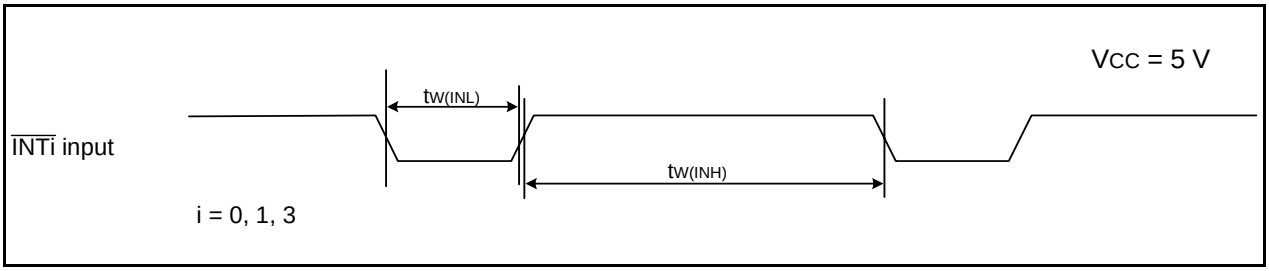


Figure 5.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 5 V

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	150	–	ns
$t_{W(CKL)}$	CLK0 Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

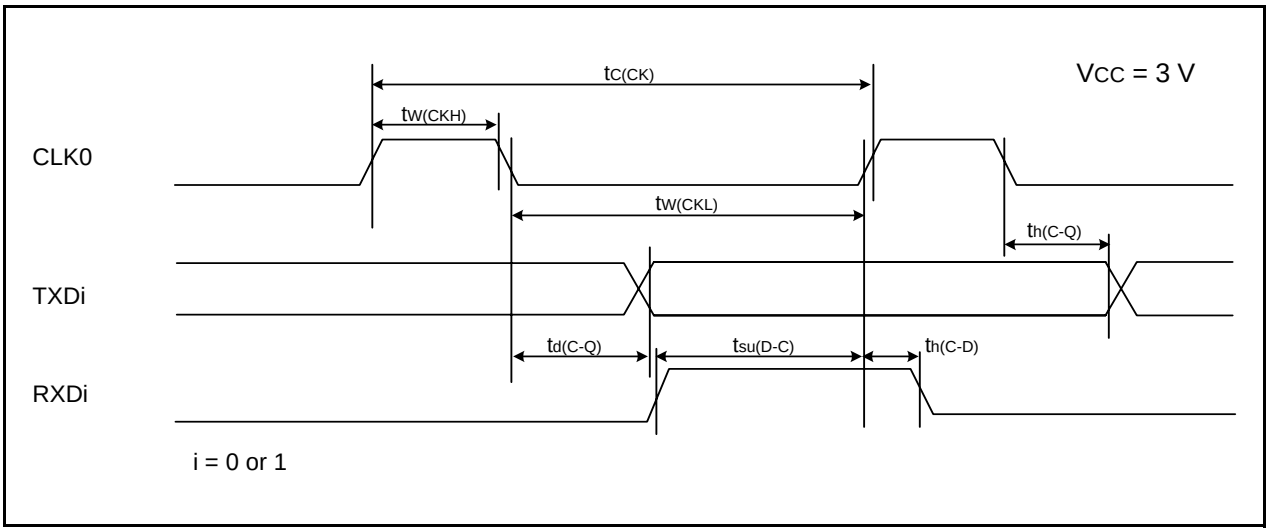


Figure 5.14 Serial Interface Timing Diagram when VCC = 3 V

Table 5.27 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

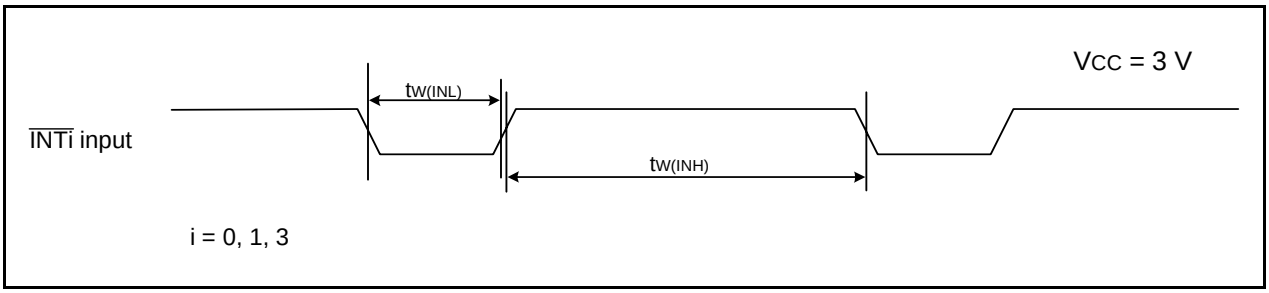


Figure 5.15 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 3 V

Table 5.38 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)

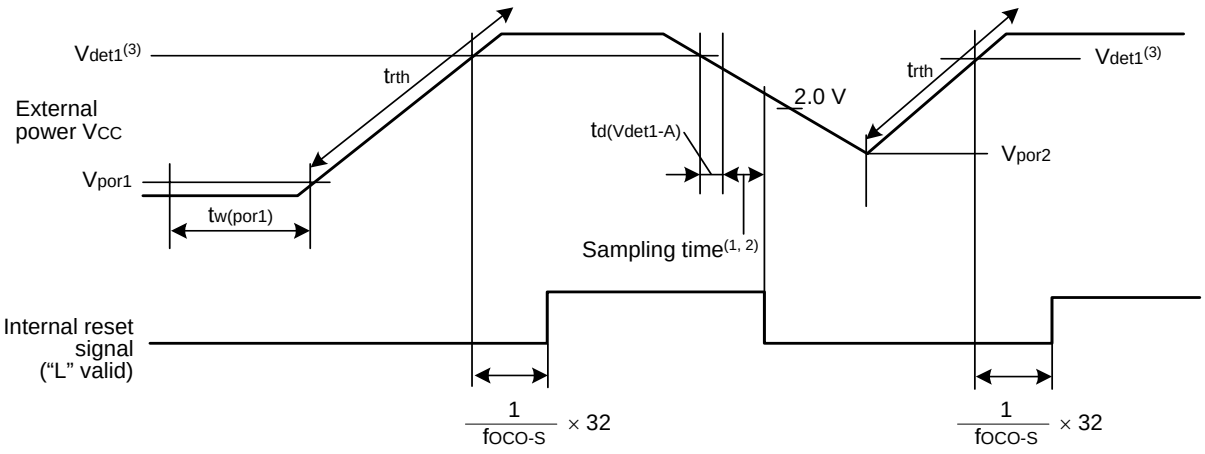
Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97 + CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		-40	–	85(8)	°C
–	Data hold time(9)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. 125°C for K version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.41 Power-on Reset Circuit, Voltage Monitor 1 Reset Electrical Characteristics(3)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage(4)		–	–	0.1	V
V_{por2}	Power-on reset or voltage monitor 1 reset valid voltage		0	–	V_{det1}	V
t_{rth}	External power V_{CC} rise gradient	$V_{CC} \leq 3.6$ V	20(2)	–	–	mV/msec
		$V_{CC} > 3.6$ V	20(2)	–	2,000	mV/msec

NOTES:
1. The measurement condition is T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. This condition (the minimum value of external power V_{CC} rise gradient) does not apply if $V_{por2} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 1 reset by setting the LVD1ON bit in the OFS register to 0, the VW1C0 and VW1C6 bits in the VW1C register to 1 respectively, and the VCA26 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30 s or more if -20°C ≤ T_{opr} ≤ 125°C, maintain $t_{w(por1)}$ for 3,000 s or more if -40°C ≤ T_{opr} < -20°C.



NOTES:
1. When using the voltage monitor 1 digital filter, ensure VCC is 2.0 V or higher during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
3. V_{det1} indicates the voltage detection level of the voltage detection 1 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.

Figure 5.22 Reset Circuit Electrical Characteristics

Table 5.42 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 4.75 to 5.25 V 0°C ≤ T_{opr} ≤ 60°C(2)	39.2	40	40.8	MHz
		V_{CC} = 3.0 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(2)	38.8	40	41.2	MHz
		V_{CC} = 3.0 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(2)	38.4	40	41.6	MHz
		V_{CC} = 3.0 to 5.5 V -40°C ≤ T_{opr} ≤ 125°C(2)	38	40	42	MHz
		V_{CC} = 2.7 to 5.5 V -40°C ≤ T_{opr} ≤ 125°C(2)	37.6	40	42.4	MHz
–	Value in FRA1 register after reset		08h	–	F7h	–
–	Oscillation frequency adjustment unit of high-speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	–	+0.3	–	MHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	400	–	µA

NOTES:
1. V_{CC} = 2.7 to 5.5 V, T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.

Table 5.43 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		40	125	250	kHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	15	–	µA

NOTE:
1. V_{CC} = 2.7 to 5.5 V, T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.

Table 5.44 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.51 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	100	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

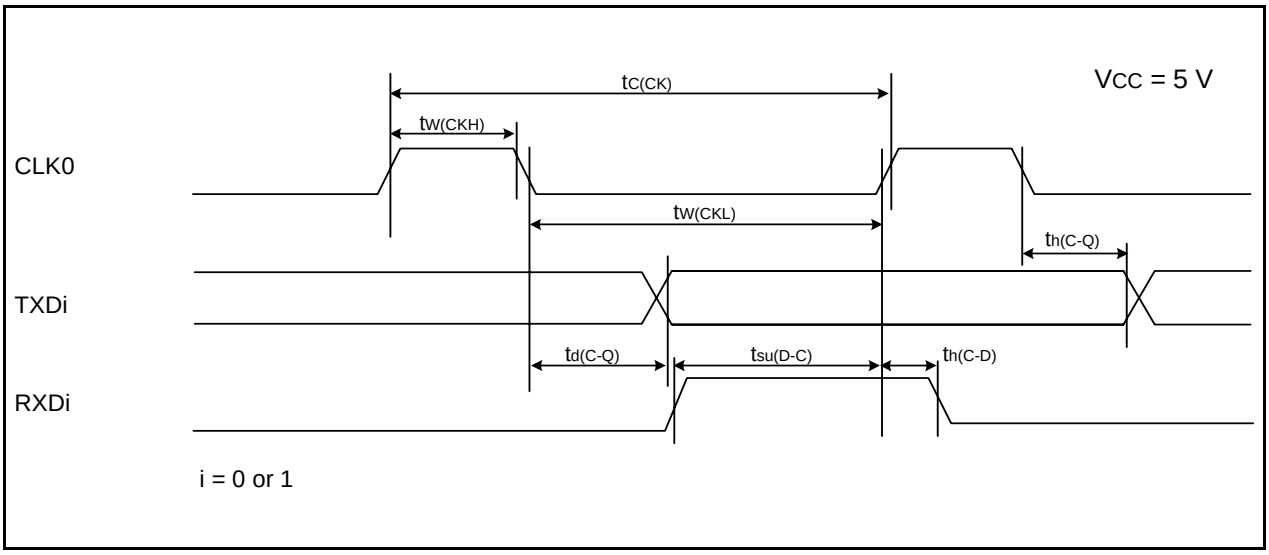


Figure 5.29 Serial Interface Timing Diagram when VCC = 5 V

Table 5.52 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

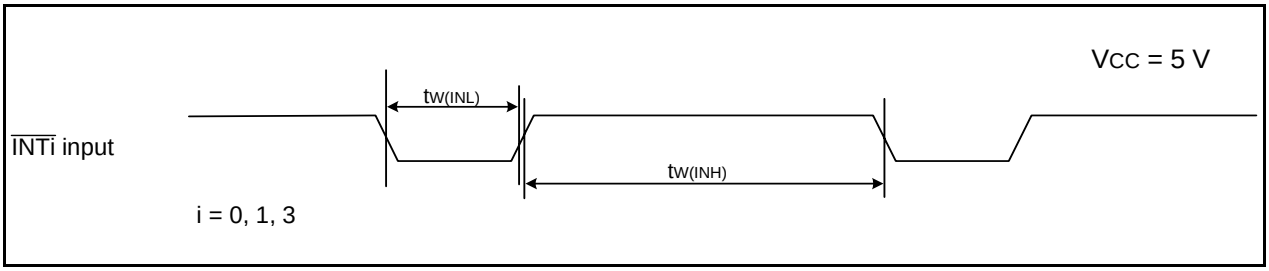


Figure 5.30 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 5 V

Table 5.54 Electrical Characteristics (4) [Vcc = 3 V]
(Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5	9	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	70	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	55	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.7	3.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.1	–	µA
			XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	3.8	–	µA

REVISION HISTORY	R8C/28 Group, R8C/29 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Nov 14, 2005	–	First Edition issued
0.30	Feb 28, 2006	all pages	"J, K version" added
		1	1.1 Applications revised
		2	Table 1.1 Functions and Specifications for R8C/28 Group revised
		3	Table 1.2 Functions and Specifications for R8C/29 Group revised
		4	Figure 1.1 Block Diagram; NOTE3 added
		5	Table 1.3 Product Information for R8C/28 Group and Figure 1.2 Type Number, Memory Size, and Package of R8C/28 Group revised
		6	Table 1.4 Product Information for R8C/29 Group and Figure 1.3 Type Number, Memory Size, and Package of R8C/29 Group revised
		7	Figure 1.4 Pin Assignments (Top View); NOTE3 added
		8	Table 1.5 Pin Functions revised
		9	Table 1.6 Pin Name Information by Pin Number; "XOUT" → "XOUT/XCOUT", "XIN" → "XIN/XCIN" revised and NOTE2 added
		13	Figure 3.1 Memory Map of R8C/28 Group; "R5F21284JSP, R5F21284KSP" added
		14	Figure 3.2 Memory Map of R8C/29 Group; "R5F21294JSP, R5F21294KSP" added
		15	Table 4.1 SFR Information (1); NOTE6 added
		18	Table 4.4 SFR Information (4); 00FEh: "DRR" → "P1DRR" symbol name revised
		22 to 66	5. Electrical Characteristics added
0.40	Mar 29, 2006	2	Table 1.1 Functions and Specifications for R8C/28 Group revised
		3	Table 1.2 Functions and Specifications for R8C/29 Group revised
		15	Table 4.1 SFR Information (1); - 0032h, 0036h, 0038h revised - NOTES 2 to 6 revised and NOTES 7 to 8 added
		19	Table 4.5 SFR Information (5); NOTE2 added
0.50	Apr 27, 2006	18	Table 4.4; 00FDh: revised
		46	Table 5.35; System clock Conditions: revised
1.00	Nov 08, 2006	All pages	"PRELIMINARY" deleted
		1	1 "J and K versions are under development...notice." added
		2	Table 1.1 revised
		3	Table 1.2 revised
		4	Figure 1.1 revised
		5	Table 1.3 revised
		6	Table 1.4 revised