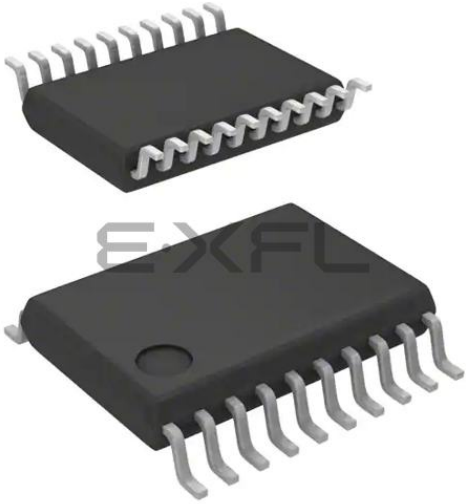


Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21294sdsp-u0

Table 1.4 Product Information for R8C/29 Group **Current of Sep. 2008**

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F21292SNSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	N version	
R5F21294SNSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A		
R5F21292SDSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	D version	
R5F21294SDSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A		
R5F21294JSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	J version	
R5F21296JSP	32 Kbytes	1 Kbyte × 2	1.5 Kbyte	PLSP0020JB-A		
R5F21294KSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	K version	
R5F21296KSP	32 Kbytes	1 Kbyte × 2	1.5 Kbyte	PLSP0020JB-A		
R5F21292SNXXXSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	N version	Factory programming product(1)
R5F21294SNXXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A		
R5F21292SDXXXSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	D version	
R5F21294SDXXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A		
R5F21294JXXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	J version	
R5F21296JXXXSP	32 Kbytes	1 Kbyte × 2	1.5 Kbyte	PLSP0020JB-A		
R5F21294KXXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	K version	
R5F21296KXXXSP	32 Kbytes	1 Kbyte × 2	1.5 Kbyte	PLSP0020JB-A		

NOTE:

1. The user ROM is programmed before shipment.

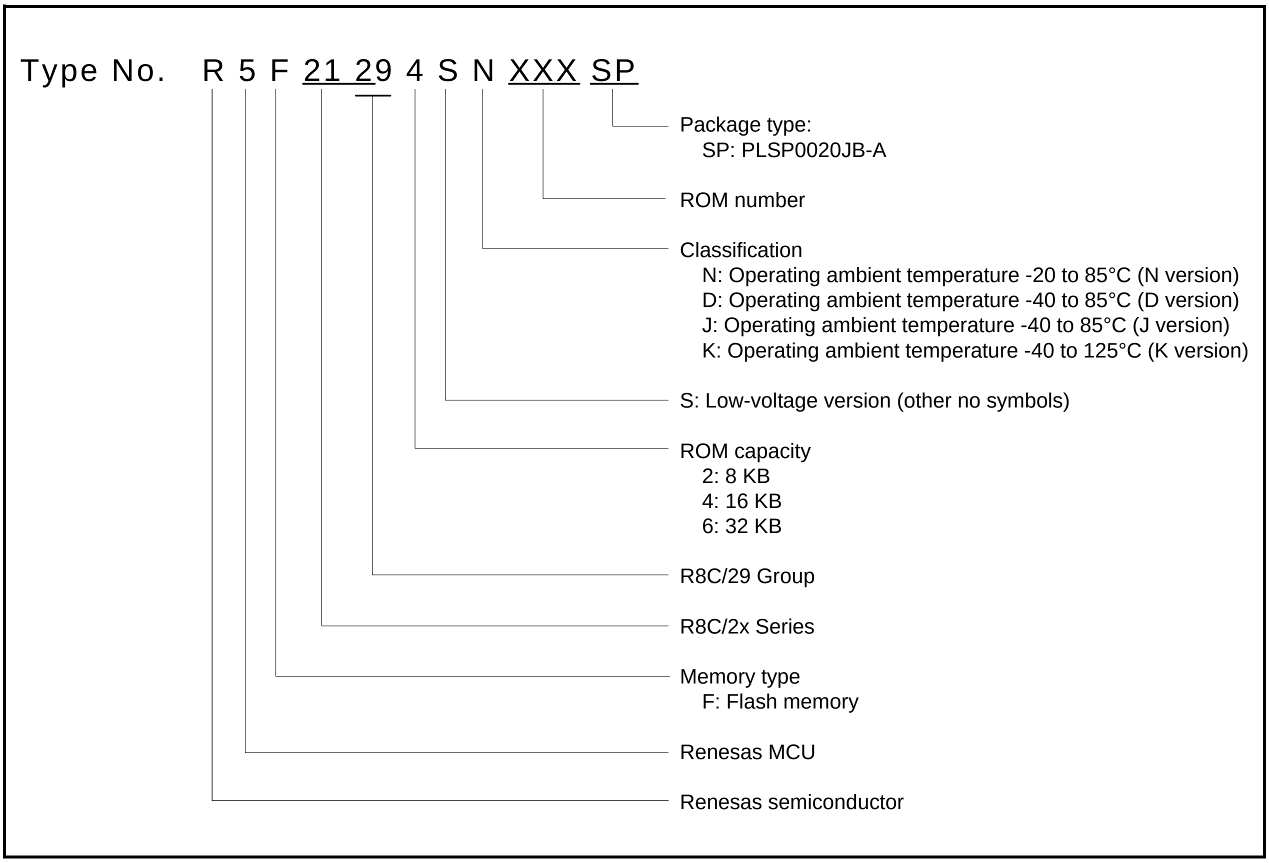


Figure 1.3 Type Number, Memory Size, and Package of R8C/29 Group

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

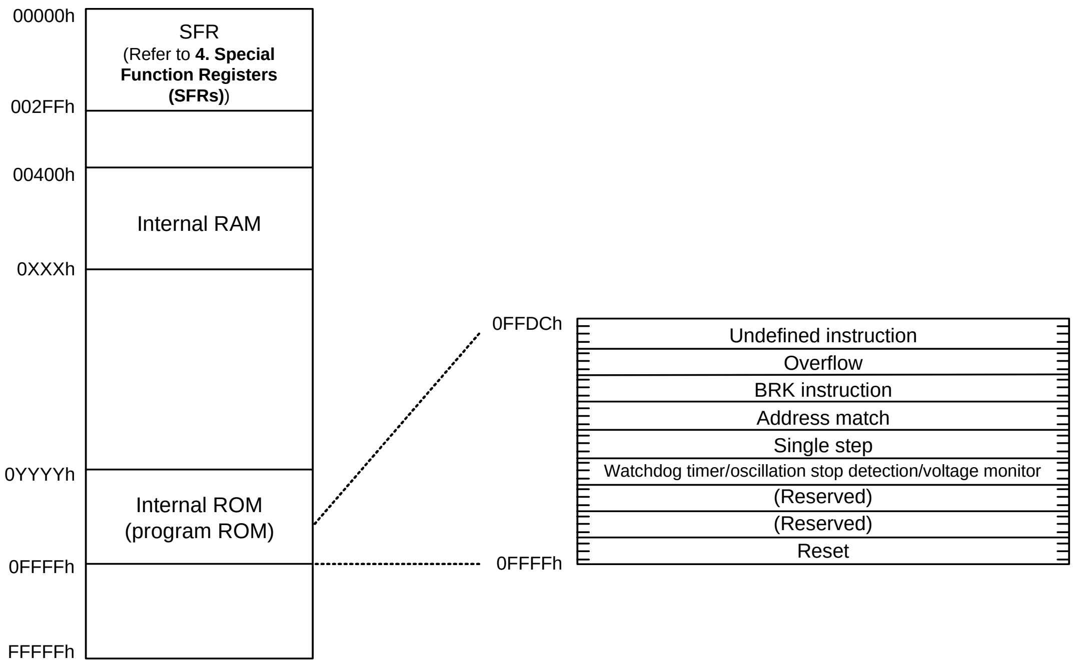
2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

3. Memory

3.1 R8C/28 Group

Figure 3.1 is a Memory Map of R8C/28 Group. The R8C/28 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F21282SNSP, R5F21282SDSP, R5F21282SNXXXSP, R5F21282SDXXXSP	8 Kbytes	0E000h	512 bytes	005FFh
R5F21284SNSP, R5F21284SDSP, R5F21284JSP, R5F21284KSP, R5F21284SNXXXSP, R5F21284SDXXXSP, R5F21284JXXXSP, R5F21284KXXXSP	16 Kbytes	0C000h	1 Kbyte	007FFh
R5F21286JSP, R5F21286KSP, R5F21286JXXXSP, R5F21286KXXXSP	32 Kbytes	08000h	1.5 Kbytes	009FFh

Figure 3.1 Memory Map of R8C/28 Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

Table 4.1 SFR Information (1)(1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b(2)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4(3)	FRA4	When shipping
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6(3)	FRA6	When shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7(3)	FRA7	When shipping
002Dh			
002Eh			
002Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The CSPROINI bit in the OFS register is set to 0.
3. In J, K version these regions are reserved. Do not access locations in these regions.

Table 4.2 SFR Information (2)(1)

Address	Register	Symbol	After reset
0030h			
0031h	Voltage Detection Register 1(2)	VCA1	00001000b
0032h	Voltage Detection Register 2(2)	VCA2	• N, D version 00h(3) 00100000b(4) • J, K version 00h(7) 01000000b(8)
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register(5)	VW1C	• N, D version 00001000b • J, K version 0000X000b(7) 0100X001b(8)
0037h	Voltage Monitor 2 Circuit Control Register(5)	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register(6)	VW0C	0000X000b(3) 0100X001b(4)
0039h			
003Fh			
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU/IIC bus Interrupt Control Register(9)	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
006Fh			
0070h			
007Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
   (J, K version) Software reset, watchdog timer reset, or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset, or the LVD0ON bit in the OFS register is set to 0 and hardware reset.
5. (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
   (J, K version) Software reset, watchdog timer reset, or voltage monitor 2 reset do not affect b2 and b3.
6. (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
   (J, K version) These regions are reserved. Do not access locations in these regions.
7. The LVD1ON bit in the OFS register is set to 1 and hardware reset.
8. Power-on reset, voltage monitor 1 reset, or the LVD1ON bit in the OFS register is set to 0 and hardware reset.
9. Selected by the IICSEL bit in the PMR register.

Table 4.6 SFR Information (6)[1]

Address	Register	Symbol	After reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		$V_{ref} = AV_{CC}$	–	–	10	Bits
–	Absolute accuracy	10-bit mode	ϕ_{AD} = 10 MHz, $V_{ref} = AV_{CC}$ = 5.0 V	–	–	±3	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, $V_{ref} = AV_{CC}$ = 5.0 V	–	–	±2	LSB
		10-bit mode	ϕ_{AD} = 10 MHz, $V_{ref} = AV_{CC}$ = 3.3 V	–	–	±5	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, $V_{ref} = AV_{CC}$ = 3.3 V	–	–	±2	LSB
		10-bit mode	ϕ_{AD} = 5 MHz, $V_{ref} = AV_{CC}$ = 2.2 V	–	–	±5	LSB
		8-bit mode	ϕ_{AD} = 5 MHz, $V_{ref} = AV_{CC}$ = 2.2 V	–	–	±2	LSB
R_{ladder}	Resistor ladder		$V_{ref} = AV_{CC}$	10	–	40	kΩ
t_{conv}	Conversion time	10-bit mode	ϕ_{AD} = 10 MHz, $V_{ref} = AV_{CC}$ = 5.0 V	3.3	–	–	µs
		8-bit mode	ϕ_{AD} = 10 MHz, $V_{ref} = AV_{CC}$ = 5.0 V	2.8	–	–	µs
V_{ref}	Reference voltage			2.2	–	AV_{CC}	V
V_{IA}	Analog input voltage(2)			0	–	AV_{CC}	V
–	A/D operating clock frequency	Without sample and hold	$V_{ref} = AV_{CC}$ = 2.7 to 5.5 V	0.25	–	10	MHz
		With sample and hold	$V_{ref} = AV_{CC}$ = 2.7 to 5.5 V	1	–	10	MHz
		Without sample and hold	$V_{ref} = AV_{CC}$ = 2.2 to 5.5 V	0.25	–	5	MHz
		With sample and hold	$V_{ref} = AV_{CC}$ = 2.2 to 5.5 V	1	–	5	MHz

NOTES:

1. AV_{CC} = 2.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

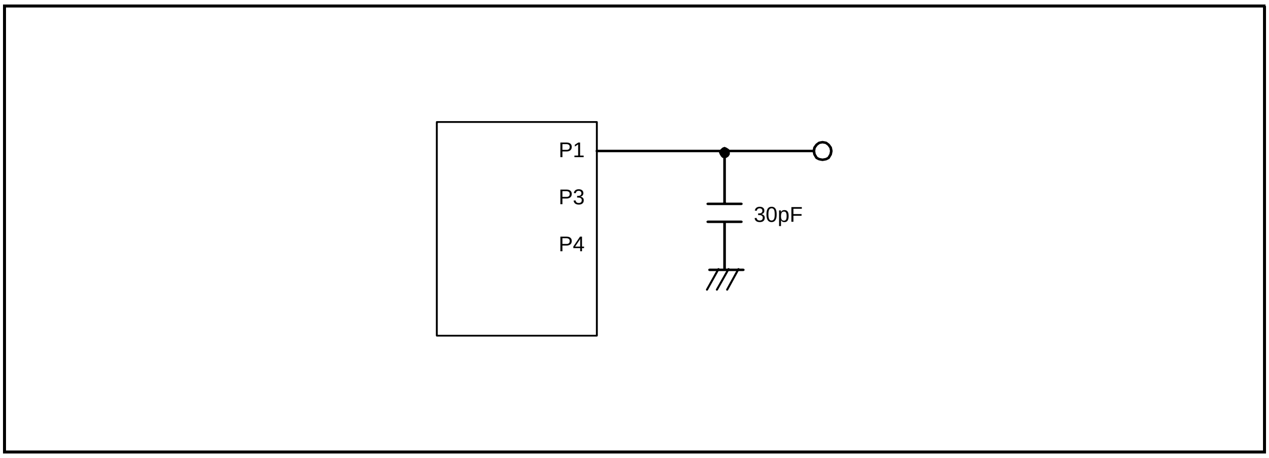


Figure 5.1 Ports P1, P3, and P4 Timing Measurement Circuit

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97 + CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		-20(8)	–	85	°C
–	Data hold time(9)	Ambient temperature = 55°C	20	–	–	year

NOTES:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. -40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

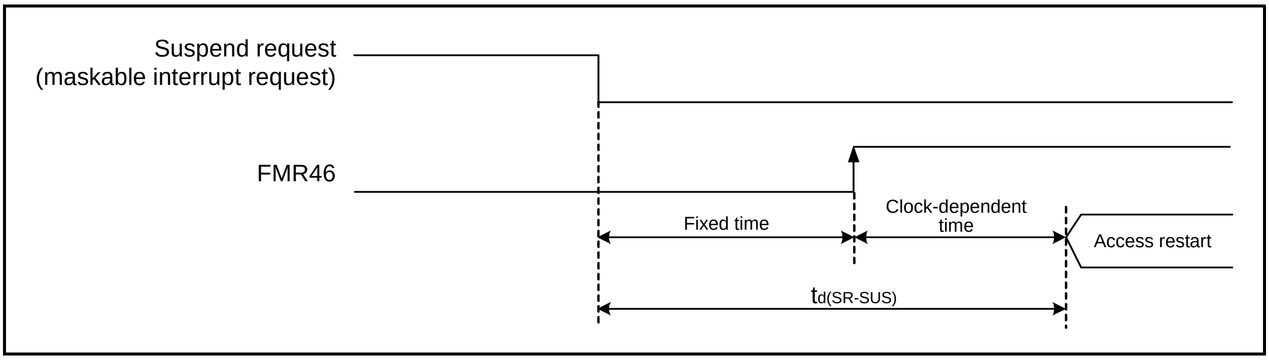


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard Min.	Standard Typ.	Standard Max.	Unit
V_{det0}	Voltage detection level		2.2	2.3	2.4	V
–	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	–	0.9	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(2)		–	–	300	µs
Vccmin	MCU operating voltage minimum value		2.2	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard Min.	Standard Typ.	Standard Max.	Unit
V_{det1}	Voltage detection level(4)		2.70	2.85	3.00	V
–	Voltage monitor 1 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
   The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard Min.	Standard Typ.	Standard Max.	Unit
V_{det2}	Voltage detection level		3.3	3.6	3.9	V
–	Voltage monitor 2 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.13 Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK clock "H" width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock "L" width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		$1t_{CYC} + 50$	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		$1t_{CYC} + 50$	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC}(2)
t_{SA}	SSI slave access time		$2.7\ V \leq V_{CC} \leq 5.5\ V$	–	–	$1.5t_{CYC} + 100$	ns
			$2.2\ V \leq V_{CC} < 2.7\ V$	–	–	$1.5t_{CYC} + 200$	ns
t_{OR}	SSI slave out open time		$2.7\ V \leq V_{CC} \leq 5.5\ V$	–	–	$1.5t_{CYC} + 100$	ns
			$2.2\ V \leq V_{CC} < 2.7\ V$	–	–	$1.5t_{CYC} + 200$	ns

NOTES:
1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)

Table 5.16 Electrical Characteristics (2) [Vcc = 5 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are V_{SS}	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10	17	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	9	15	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	10	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	130	300	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	30	–	µA

Table 5.20 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	100	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

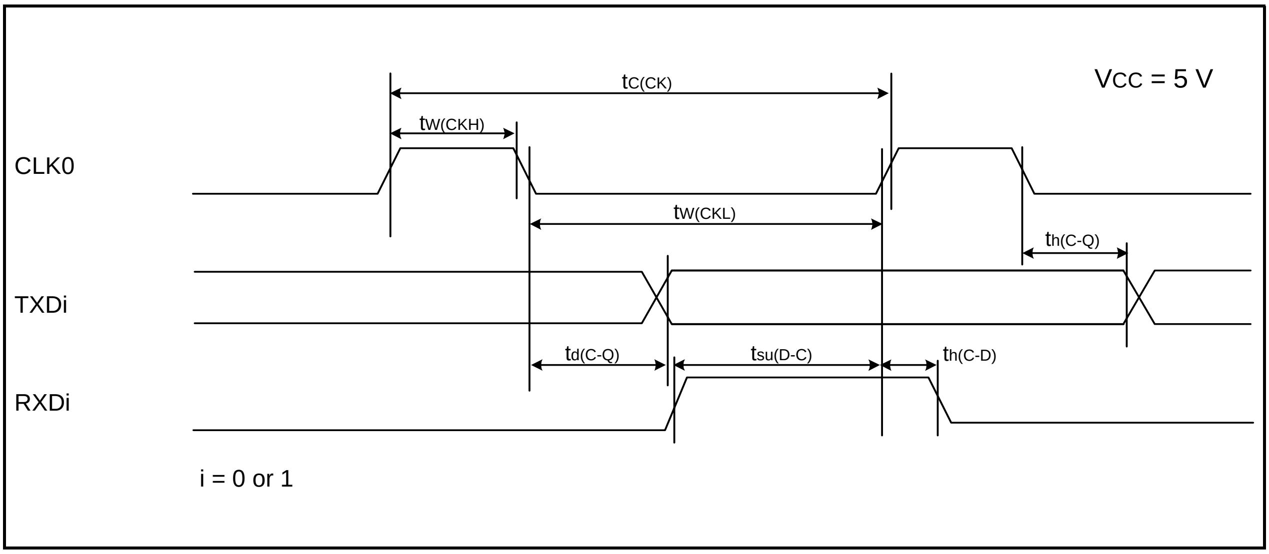


Figure 5.10 Serial Interface Timing Diagram when V_{CC} = 5 V

Table 5.21 External Interrupt $\overline{\text{INTi}}$ (i = 0, 1, 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{\text{INTi}}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{\text{INTi}}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

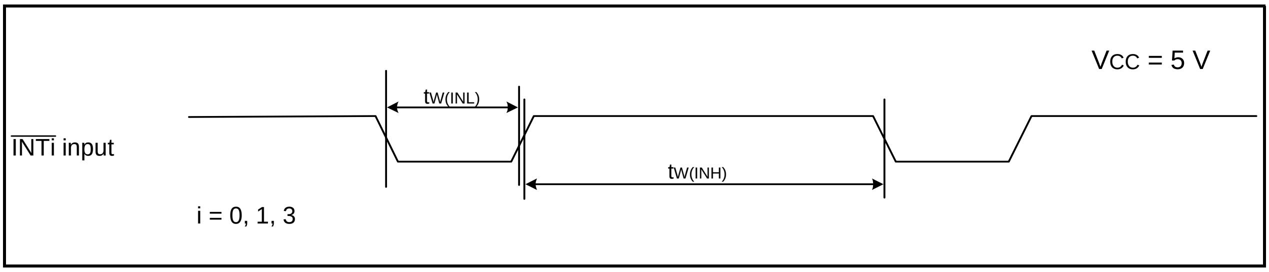


Figure 5.11 External Interrupt $\overline{\text{INTi}}$ Input Timing Diagram when V_{CC} = 5 V

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	150	–	ns
$t_{W(CKL)}$	CLK0 Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

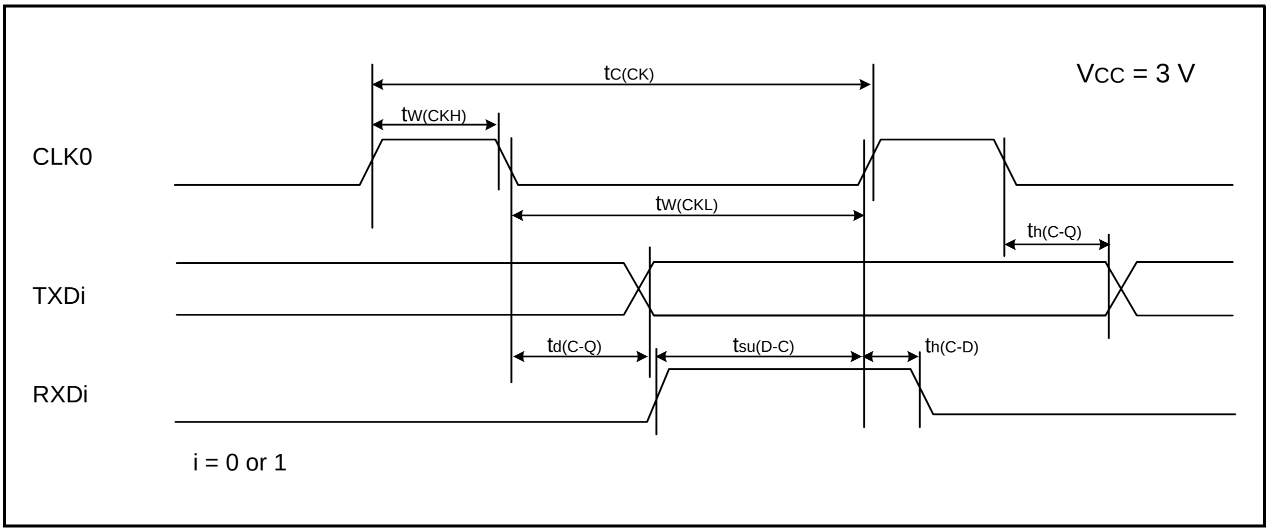


Figure 5.14 Serial Interface Timing Diagram when VCC = 3 V

Table 5.27 External Interrupt $\overline{\text{INTi}}$ (i = 0, 1, 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{\text{INTi}}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{\text{INTi}}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

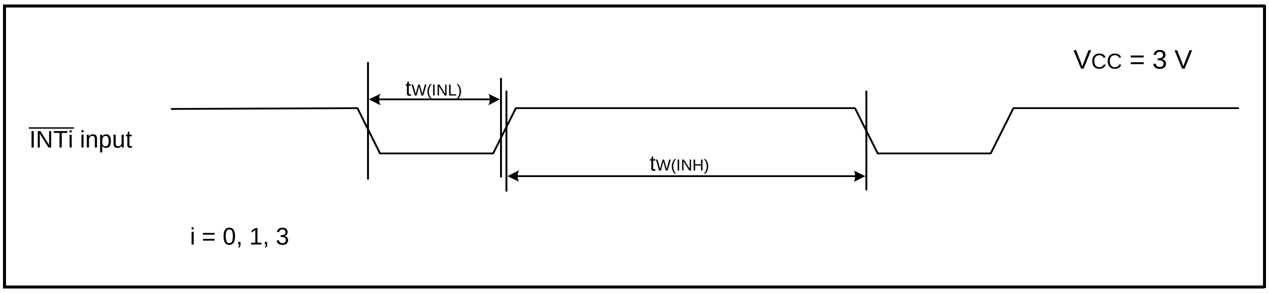


Figure 5.15 External Interrupt $\overline{\text{INTi}}$ Input Timing Diagram when VCC = 3 V

Timing requirements
(Unless Otherwise Specified: VCC = 2.2 V, VSS = 0 V at Topr = 25°C) [VCC = 2.2 V]

Table 5.30 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

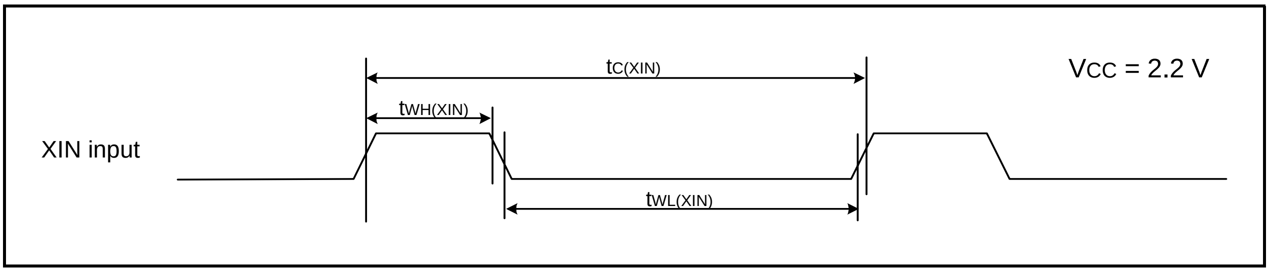


Figure 5.16 XIN Input and XCIN Input Timing Diagram when VCC = 2.2 V

Table 5.31 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	–	ns

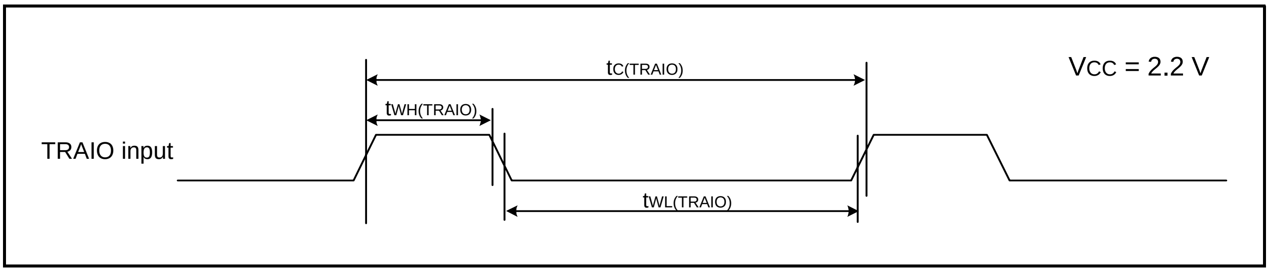


Figure 5.17 TRAIO Input Timing Diagram when VCC = 2.2 V

5.2 J, K Version

Table 5.34 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage		-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC} + 0.3	V
V_O	Output voltage		-0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	-40 °C ≤ T_{opr} ≤ 85 °C	300	mW
		85 °C ≤ T_{opr} ≤ 125 °C	125	mW
T_{opr}	Operating ambient temperature		-40 to 85 (J version) / -40 to 125 (K version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.35 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage			2.7	–	5.5	V
V_{SS}/AV_{SS}	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8 V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2 V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$		–	–	-60	mA
$I_{OH(peak)}$	Peak output “H” current			–	–	-10	mA
$I_{OH(avg)}$	Average output “H” current			–	–	-5	mA
$I_{OL(sum)}$	Peak sum output “L” currents	Sum of all pins $I_{OL(peak)}$		–	–	60	mA
$I_{OL(peak)}$	Peak output “L” currents			–	–	10	mA
$I_{OL(avg)}$	Average output “L” current			–	–	5	mA
$f_{(XIN)}$	XIN clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V (other than K version)	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V (K version)	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
–	System clock	OCD2 = 0 XIN clock selected	3.0 V ≤ V_{CC} ≤ 5.5 V (other than K version)	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V (K version)	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	–	125	–	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected (other than K version)	–	–	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected	–	–	10	MHz

NOTES:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.37 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance[2]	R8C/28 Group	100[3]	–	–	times
		R8C/29 Group	1,000[3]	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97 + CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time[7]	Ambient temperature = 55°C	20	–	–	year

NOTES:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

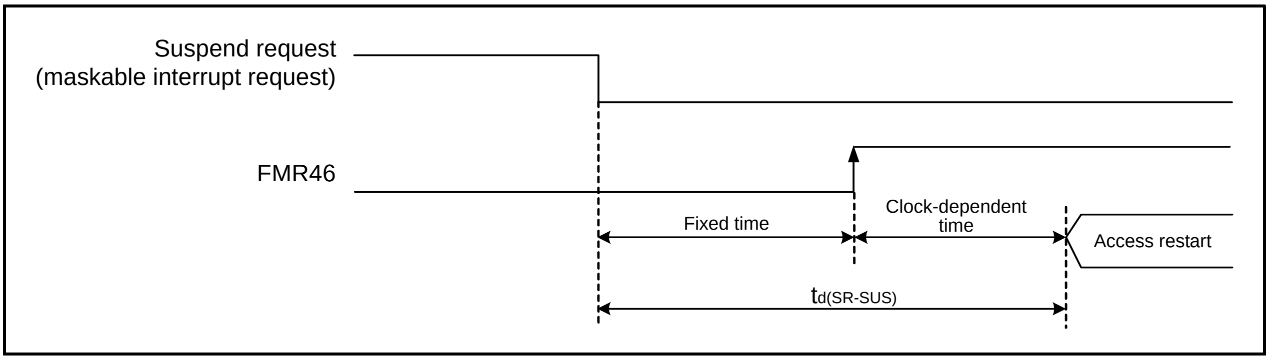


Figure 5.21 Time delay until Suspend

Table 5.39 Voltage Detection 1 Circuit Electrical Characteristics

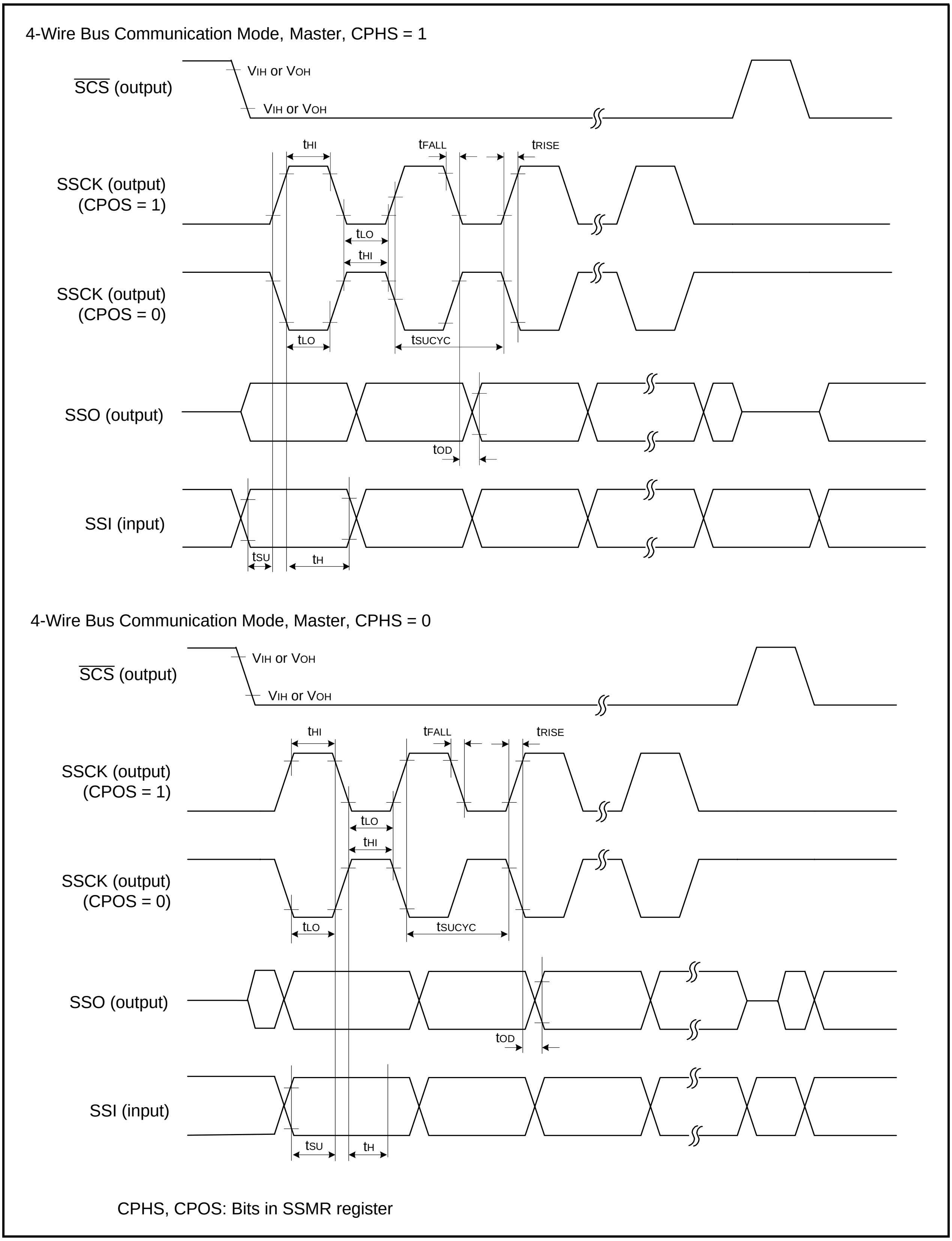
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level(2, 4)		2.70	2.85	3.0	V
$t_{d(Vdet1-A)}$	Voltage monitor 1 reset generation time(5)		–	40	200	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs
Vccmin	MCU operating voltage minimum value		2.70	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version).
2. Hold $V_{det2} > V_{det1}$.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
   The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.
5. Time until the voltage monitor 1 reset is generated after the voltage passes V_{det1} when V_{CC} falls. When using the digital filter, its sampling time is added to $t_{d(Vdet1-A)}$. When using the voltage monitor 1 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det1} when the power supply falls.

Table 5.40 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level(2)		3.3	3.6	3.9	V
$t_{d(Vdet2-A)}$	Voltage monitor 2 reset/interrupt request generation time(3., 5)		–	40	200	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(4)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version).
2. Hold $V_{det2} > V_{det1}$.
3. Time until the voltage monitor 2 reset/interrupt request is generated after the voltage passes V_{det2}.
4. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
5. When using the digital filter, its sampling time is added to $t_{d(Vdet2-A)}$. When using the voltage monitor 2 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det2} when the power supply falls.


4-Wire Bus Communication Mode, Master, CPHS = 1

4-Wire Bus Communication Mode, Master, CPHS = 0

CPHS, CPOS: Bits in SSMR register

Figure 5.23 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

Table 5.48 Electrical Characteristics (2) [Vcc = 5 V]
(T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are V_{SS}	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10	17	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	9	15	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz (J version) Low-speed on-chip oscillator on = 125 kHz No division	–	10	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz (J version) Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	75	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	60	µA
		Stop mode	XIN clock off, T_{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.8	3.0	µA
			XIN clock off, T_{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.2	–	µA
			XIN clock off, T_{opr} = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	4.0	–	µA

Table 5.53 Electrical Characteristics (3) [V_{CC} = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except XOUT	I_{OH} = -1 mA		V_{CC} - 0.5	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = -0.1 mA	V_{CC} - 0.5	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -50 μA	V_{CC} - 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except XOUT	I_{OL} = 1 mA		–	–	0.5	V
		XOUT	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO			0.1	0.3	–	V
		$\overline{RESET}$			0.1	0.4	–	V
I_{IH}	Input “H” current		VI = 3 V, V_{CC} = 3V		–	–	4.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 3V		–	–	-4.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	XIN			–	3.0	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		2.0	–	–	V

NOTE:

1. V_{CC} = 2.7 to 3.3 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), f(XIN) = 10 MHz, unless otherwise specified.