What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21294snsp-u0

1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C CPU core, and are packaged in a 20-pin molded-plastic LSSOP. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.

Furthermore, the R8C/29 Group has on-chip data flash (1 KB × 2 blocks).

The difference between the R8C/28 Group and R8C/29 Group is only the presence or absence of data flash. Their peripheral functions are the same.

1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer products, automotive, etc.

1.2   Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/28 Group and Table 1.2 outlines the Functions and Specifications for R8C/29 Group.

Table 1.1   Functions and Specifications for R8C/28 Group

	Item	Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) (other than K version) 62.5 ns (f(XIN) = 16 MHz, VCC = 3.0 to 5.5 V) (K version) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V) (N, D version)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to **Table 1.3 Product Information for R8C/28 Group**
Peripheral Functions	Ports	I/O ports: 13 pins, Input port: 3 pins
	LED drive ports	I/O ports: 8 pins (N, D version)

	Timers	Timer RA: 8 bits × 1 channel
		Timer RB: 8 bits × 1 channel
		                (Each timer equipped with 8-bit prescaler)
		Timer RC: 16 bits × 1 channel
		                (Input capture and output compare circuits)
		Timer RE: With real-time clock and compare match function
		                (For J, K version, compare match function only.)

	Serial interfaces	1 channel (UART0): Clock synchronous serial I/O, UART 1 channel (UART1): UART

	Clock synchronous serial interface	1 channel
		  I2C bus Interface[1]
		  Clock synchronous serial I/O with chip select

	LIN module	Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog timer	15 bits × 1 channel (with prescaler) Reset start selectable
	Interrupts	Internal: 15 sources (N, D version), Internal: 14 sources (J, K version) External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	3 circuits • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz) (N, D version) • Real-time clock (timer RE) (N, D version)
	Oscillation stop detection function	XIN clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip
Electrical Characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (N, D version)
	Current consumption (N, D version)	Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz) Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	100 times
Operating Ambient Temperature		-20 to 85°C (N version)
		-40 to 85°C (D, J version)[2], -40 to 125°C (K version)[2]
Package		20-pin molded-plastic LSSOP

NOTES:
  1. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
  2. Specify the D, K version if D, K version functions are to be used.

RENESAS

1.3 Block Diagram
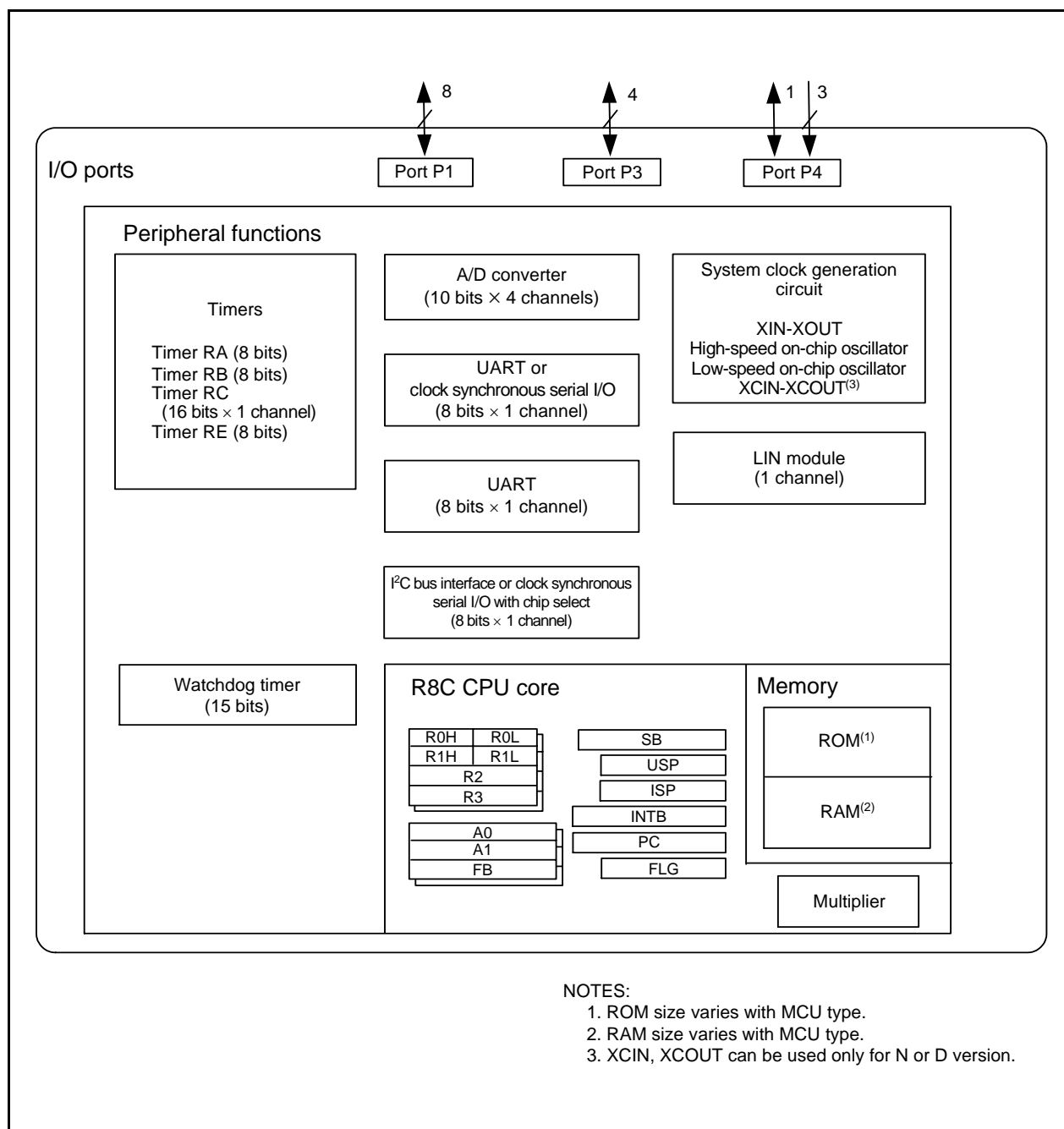
Figure 1.1 shows a Block Diagram.

Figure 1.1   Block Diagram

1.4 Product Information

Table 1.3 lists the Product Information for R8C/28 Group and Table 1.4 lists the Product Information for R8C/29 Group.

Table 1.3   Product Information for R8C/28 Group   **Current of Sep. 2008**

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks	
R5F21282SNSP	8 Kbytes	512 bytes	PLSP0020JB-A	N version	
R5F21284SNSP	16 Kbytes	1 Kbyte	PLSP0020JB-A		
R5F21282SDSP	8 Kbytes	512 bytes	PLSP0020JB-A	D version	
R5F21284SDSP	16 Kbytes	1 Kbyte	PLSP0020JB-A		
R5F21284JSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	J version	
R5F21286JSP	32 Kbytes	1.5 Kbyte	PLSP0020JB-A		
R5F21284KSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	K version	
R5F21286KSP	32 Kbytes	1.5 Kbyte	PLSP0020JB-A		
R5F21282SNXXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	N version	Factory programming product[1]
R5F21284SNXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A		
R5F21282SDXXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	D version	
R5F21284SDXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A		
R5F21284JXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	J version	
R5F21286JXXXSP	32 Kbytes	1.5 Kbyte	PLSP0020JB-A		
R5F21284KXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	K version	
R5F21286KXXXSP	32 Kbytes	1.5 Kbyte	PLSP0020JB-A		

NOTE:
1. The user ROM is programmed before shipment.

Type No. R 5 F 21 28 4 S N XXX SP

Package type:
　SP: PLSP0020JB-A

ROM number

Classification
　N: Operating ambient temperature -20 to 85°C (N version)
　D: Operating ambient temperature -40 to 85°C (D version)
　J: Operating ambient temperature -40 to 85°C (J version)
　K: Operating ambient temperature -40 to 125°C (K version)

S: Low-voltage version (other no symbols)

ROM capacity
　2: 8 KB
　4: 16 KB
　6: 32 KB

R8C/28 Group

R8C/2x Series

Memory type
　F: Flash memory

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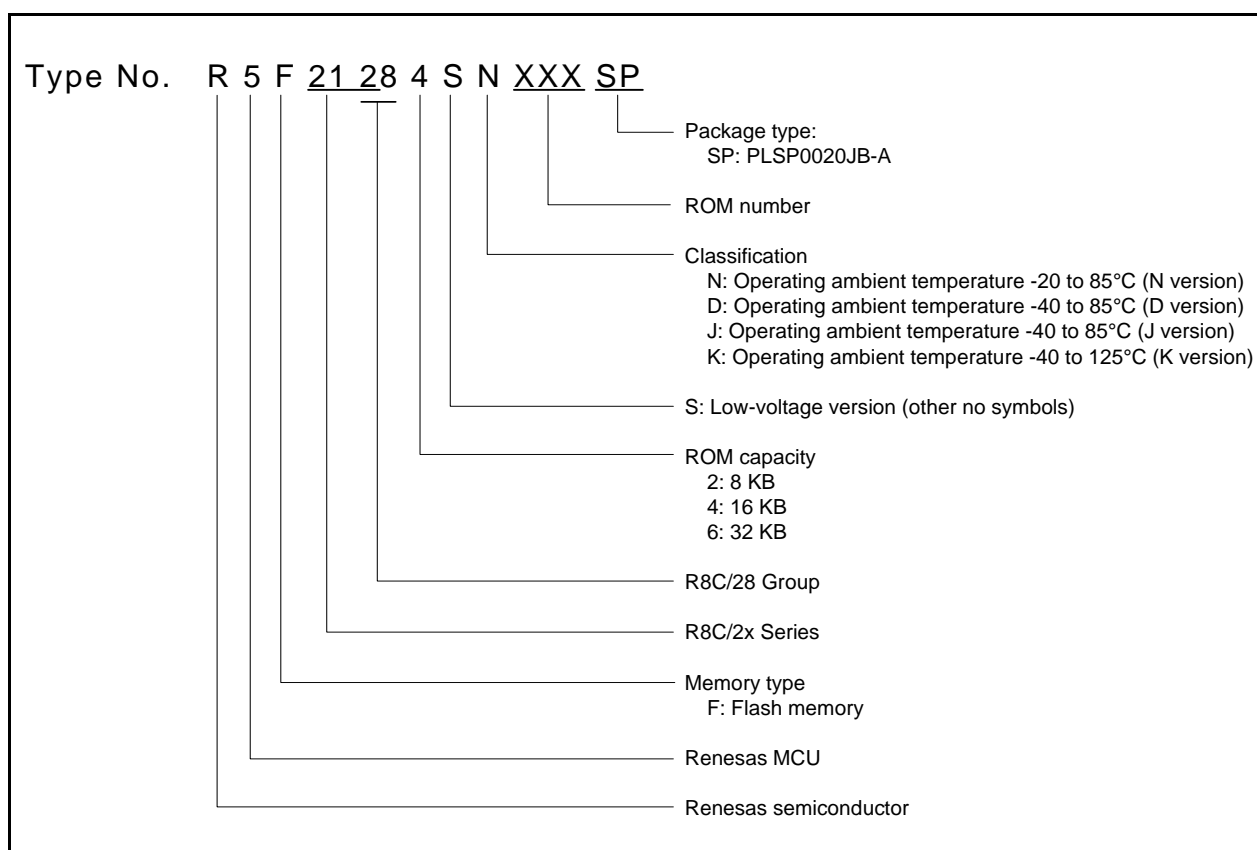
Figure 1.2   Type Number, Memory Size, and Package of R8C/28 Group

Table 1.4   Product Information for R8C/29 Group   Current of Sep. 2008

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F21292SNSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	N version	
R5F21294SNSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A		
R5F21292SDSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	D version	
R5F21294SDSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A		
R5F21294JSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	J version	
R5F21296JSP	32 Kbytes	1 Kbyte × 2	1.5 Kbyte	PLSP0020JB-A		
R5F21294KSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	K version	
R5F21296KSP	32 Kbytes	1 Kbyte × 2	1.5 Kbyte	PLSP0020JB-A		
R5F21292SNXXXSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	N version	Factory programming product[1]
R5F21294SNXXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A		
R5F21292SDXXXSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	D version	
R5F21294SDXXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A		
R5F21294JXXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	J version	
R5F21296JXXXSP	32 Kbytes	1 Kbyte × 2	1.5 Kbyte	PLSP0020JB-A		
R5F21294KXXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	K version	
R5F21296KXXXSP	32 Kbytes	1 Kbyte × 2	1.5 Kbyte	PLSP0020JB-A		

NOTE:
1. The user ROM is programmed before shipment.

Type No.   R 5 F 21 29 4 S N XXX SP

Package type:
    SP: PLSP0020JB-A

ROM number

Classification
    N: Operating ambient temperature -20 to 85°C (N version)
    D: Operating ambient temperature -40 to 85°C (D version)
    J: Operating ambient temperature -40 to 85°C (J version)
    K: Operating ambient temperature -40 to 125°C (K version)

S: Low-voltage version (other no symbols)

ROM capacity
    2: 8 KB
    4: 16 KB
    6: 32 KB

R8C/29 Group

R8C/2x Series

Memory type
    F: Flash memory

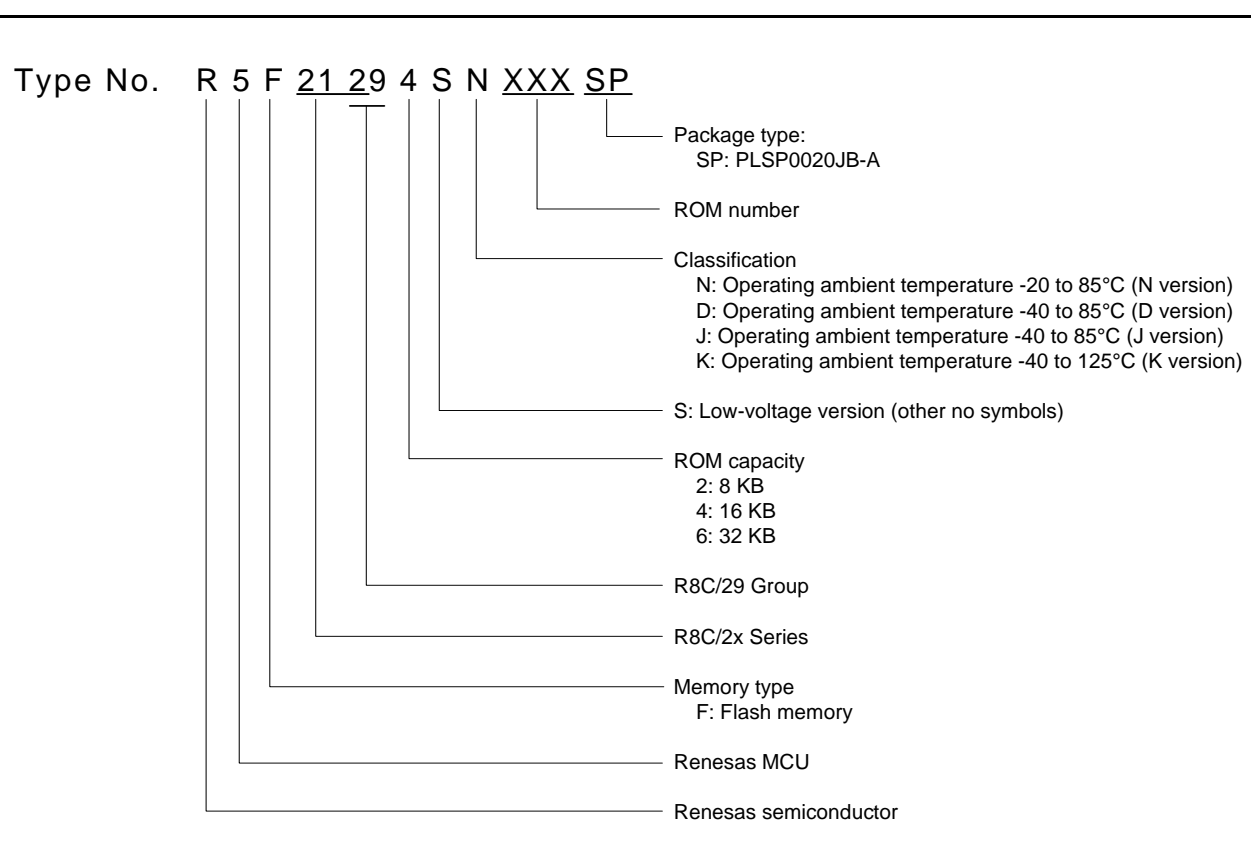Renesas MCU

Renesas semiconductor

Figure 1.3   Type Number, Memory Size, and Package of R8C/29 Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

Table 4.1 SFR Information (1)[1]

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b[2]
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4[3]	FRA4	When shipping
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6[3]	FRA6	When shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7[3]	FRA7	When shipping
002Dh			
002Eh			
002Fh			

X: Undefined
NOTES:
    1. The blank regions are reserved. Do not access locations in these regions.
    2. The CSPROINI bit in the OFS register is set to 0.
    3. In J, K version these regions are reserved. Do not access locations in these regions.

Table 4.2 SFR Information (2)[1]

Address	Register	Symbol	After reset
0030h			
0031h	Voltage Detection Register 1[2]	VCA1	00001000b
0032h	Voltage Detection Register 2[2]	VCA2	• N, D version 00h[3] 00100000b[4] • J, K version 00h[7] 01000000b[8]
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register[5]	VW1C	• N, D version 00001000b • J, K version 0000X000b[7] 0100X001b[8]
0037h	Voltage Monitor 2 Circuit Control Register[5]	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register[6]	VW0C	0000X000b[3] 0100X001b[4]
0039h			
003Fh			
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU/IIC bus Interrupt Control Register[9]	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
006Fh			
0070h			
007Fh			

X: Undefined

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
   (J, K version) Software reset, watchdog timer reset, or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset, or the LVD0ON bit in the OFS register is set to 0 and hardware reset.
5. (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
   (J, K version) Software reset, watchdog timer reset, or voltage monitor 2 reset do not affect b2 and b3.
6. (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
   (J, K version) These regions are reserved. Do not access locations in these regions.
7. The LVD1ON bit in the OFS register is set to 1 and hardware reset.
8. Power-on reset, voltage monitor 1 reset, or the LVD1ON bit in the OFS register is set to 0 and hardware reset.
9. Selected by the IICSEL bit in the PMR register.

Table 4.7   SFR Information (7)[1]

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined
NOTES:
   1. The blank regions are reserved. Do not access locations in these regions.
   2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

Table 5.13   Timing Requirements of Clock Synchronous Serial I/O with Chip Select[1]

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC}[2]
t_{HI}	SSCK clock "H" width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock "L" width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC}[2]
		Slave		–	–	1	μs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC}[2]
		Slave		–	–	1	μs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_{H}	SSO, SSI data input hold time			1	–	–	t_{CYC}[2]
t_{LEAD}	$\overline{SCS}$ setup time	Slave		$1t_{CYC}$ + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		$1t_{CYC}$ + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC}[2]
t_{SA}	SSI slave access time		2.7 V ≤ Vcc ≤ 5.5 V	–	–	$1.5t_{CYC}$ + 100	ns
			2.2 V ≤ Vcc < 2.7 V	–	–	$1.5t_{CYC}$ + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ Vcc ≤ 5.5 V	–	–	$1.5t_{CYC}$ + 100	ns
			2.2 V ≤ Vcc < 2.7 V	–	–	$1.5t_{CYC}$ + 200	ns

NOTES:
1. Vcc = 2.2 to 5.5 V, Vss = 0 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)
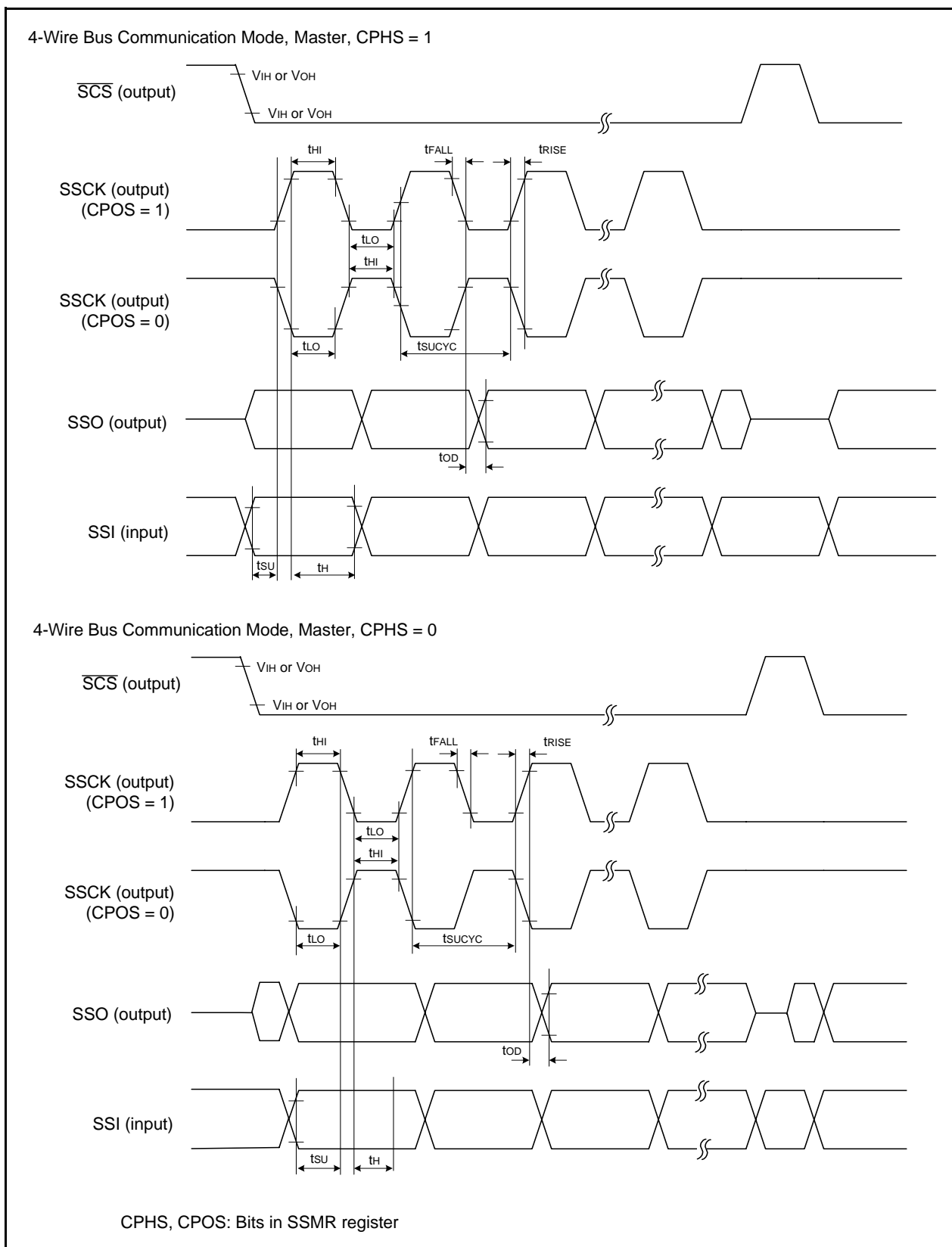
Figure 5.4   I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)
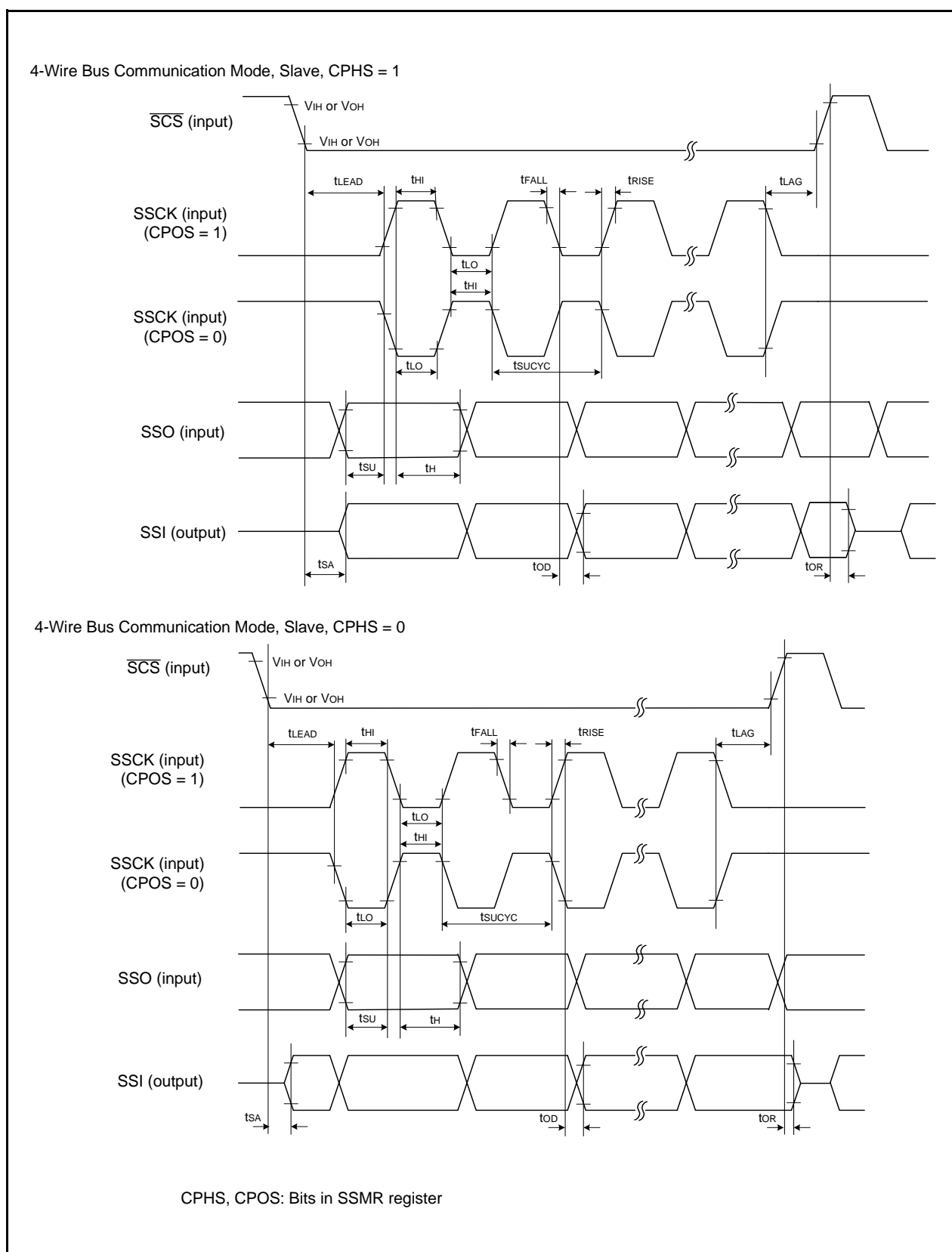
Figure 5.5   I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

Table 5.15 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output "H" voltage	Except P1_0 to P1_7, XOUT	IOH = -5 mA		Vcc - 2.0	–	Vcc	V
			IOH = -200 μA		Vcc - 0.5	–	Vcc	V
		P1_0 to P1_7	Drive capacity HIGH	IOH = -20 mA	Vcc - 2.0	–	Vcc	V
			Drive capacity LOW	IOH = -5 mA	Vcc - 2.0	–	Vcc	V
		XOUT	Drive capacity HIGH	IOH = -1 mA	Vcc - 2.0	–	Vcc	V
			Drive capacity LOW	IOH = -500 μA	Vcc - 2.0	–	Vcc	V
VOL	Output "L" voltage	Except P1_0 to P1_7, XOUT	IOL = 5 mA		–	–	2.0	V
			IOL = 200 μA		–	–	0.45	V
		P1_0 to P1_7	Drive capacity HIGH	IOL = 20 mA	–	–	2.0	V
			Drive capacity LOW	IOL = 5 mA	–	–	2.0	V
		XOUT	Drive capacity HIGH	IOL = 1 mA	–	–	2.0	V
			Drive capacity LOW	IOL = 500 μA	–	–	2.0	V
VT+-VT-	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO			0.1	0.5	–	V
		$\overline{RESET}$			0.1	1.0	–	V
IIH	Input "H" current		VI = 5 V, Vcc = 5V		–	–	5.0	μA
IIL	Input "L" current		VI = 0 V, Vcc = 5V		–	–	-5.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5V		30	50	167	kΩ
RfXIN	Feedback resistance	XIN			–	1.0	–	MΩ
RfXCIN	Feedback resistance	XCIN			–	18	–	MΩ
VRAM	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. Vcc = 4.2 to 5.5 V at Topr = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.26   Serial Interface

Symbol	Parameter	Standard Min.	Standard Max.	Unit
tc(CK)	CLK0 input cycle time	300	–	ns
tW(CKH)	CLK0 input "H" width	150	–	ns
tW(CKL)	CLK0 Input "L" width	150	–	ns
td(C-Q)	TXDi output delay time	–	80	ns
th(C-Q)	TXDi hold time	0	–	ns
tsu(D-C)	RXDi input setup time	70	–	ns
th(C-D)	RXDi input hold time	90	–	ns

i = 0 or 1
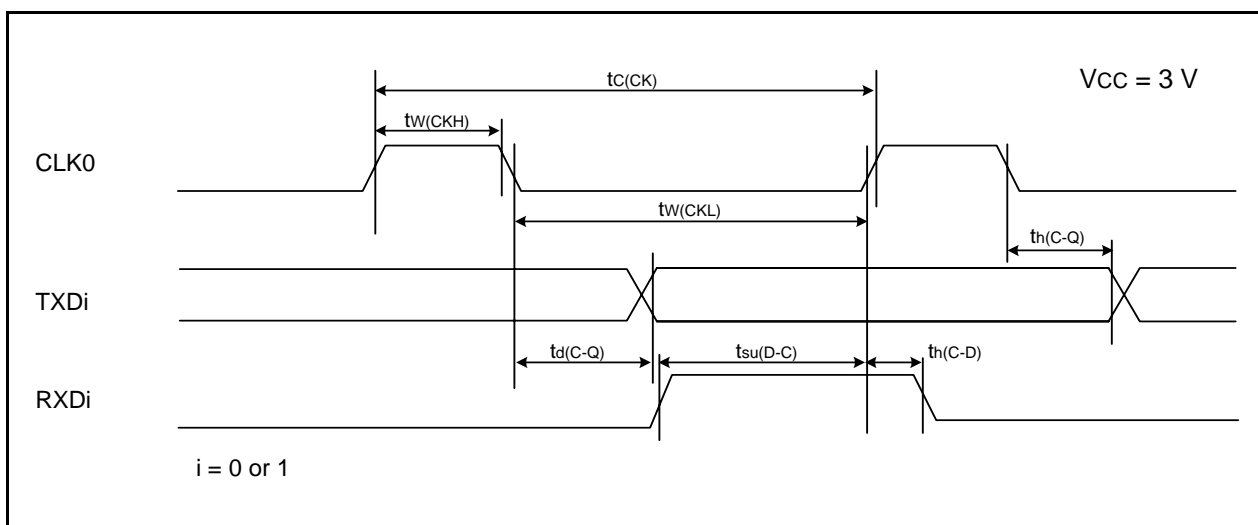
Figure 5.14   Serial Interface Timing Diagram when VCC = 3 V

Table 5.27   External Interrupt INTi (i = 0, 1, 3) Input

Symbol	Parameter	Standard Min.	Standard Max.	Unit
tW(INH)	INTi input "H" width	380[1]	–	ns
tW(INL)	INTi input "L" width	380[2]	–	ns

NOTES:
1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
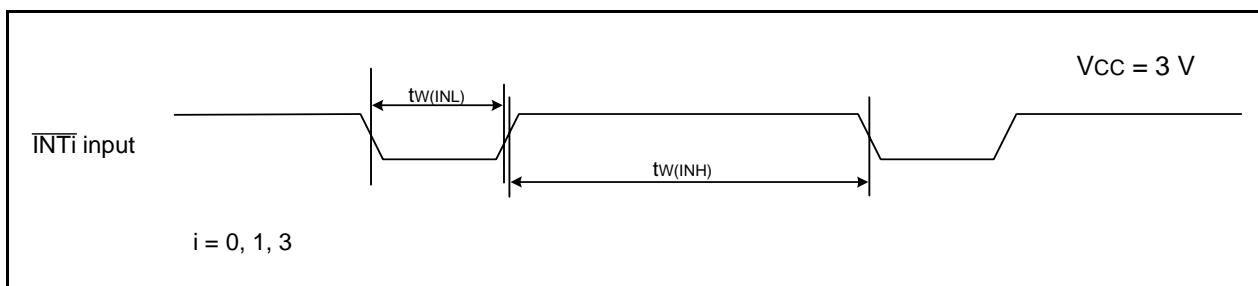
Figure 5.15   External Interrupt INTi Input Timing Diagram when VCC = 3 V

Timing requirements
(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C) [Vcc = 2.2 V]

Table 5.30   XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(XIN)}$	XIN input cycle time	200	–	ns
$t_{WH(XIN)}$	XIN input "H" width	90	–	ns
$t_{WL(XIN)}$	XIN input "L" width	90	–	ns
$t_{C(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input "H" width	7	–	μs
$t_{WL(XCIN)}$	XCIN input "L" width	7	–	μs
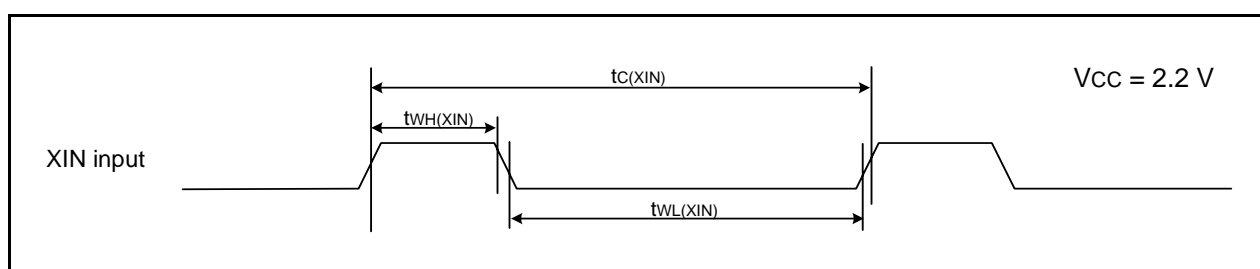
Figure 5.16   XIN Input and XCIN Input Timing Diagram when Vcc = 2.2 V

Table 5.31   TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	200	–	ns
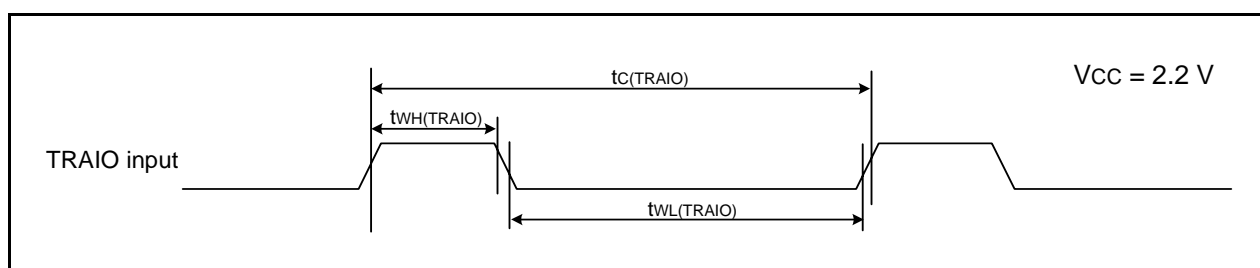
Figure 5.17   TRAIO Input Timing Diagram when Vcc = 2.2 V
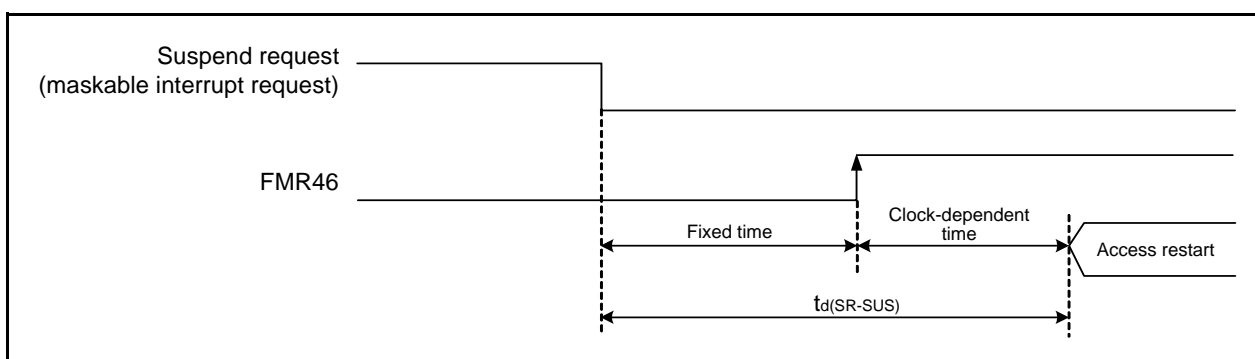
Figure 5.21   Time delay until Suspend

Table 5.39   Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level[2, 4]		2.70	2.85	3.0	V
$t_{d(Vdet1-A)}$	Voltage monitor 1 reset generation time[5]		–	40	200	μs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	0.6	–	μA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts[3]		–	–	100	μs
V_{ccmin}	MCU operating voltage minimum value		2.70	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version).
2. Hold V_{det2} > V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
   The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.
5. Time until the voltage monitor 1 reset is generated after the voltage passes V_{det1} when V_{CC} falls. When using the digital filter, its sampling time is added to $t_{d(Vdet1-A)}$. When using the voltage monitor 1 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det1} when the power supply falls.

Table 5.40   Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level[2]		3.3	3.6	3.9	V
$t_{d(Vdet2-A)}$	Voltage monitor 2 reset/interrupt request generation time[3., 5]		–	40	200	μs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	0.6	–	μA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts[4]		–	–	100	μs

NOTES:
1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version).
2. Hold V_{det2} > V_{det1}.
3. Time until the voltage monitor 2 reset/interrupt request is generated after the voltage passes V_{det2}.
4. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
5. When using the digital filter, its sampling time is added to $t_{d(Vdet2-A)}$. When using the voltage monitor 2 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det2} when the power supply falls.

Table 5.41   Power-on Reset Circuit, Voltage Monitor 1 Reset Electrical Characteristics[3]

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage[4]		–	–	0.1	V
V_{por2}	Power-on reset or voltage monitor 1 reset valid voltage		0	–	V_{det1}	V
t_{rth}	External power V_{CC} rise gradient	$V_{CC} \leq 3.6$ V	20[2]	–	–	mV/msec
		$V_{CC} > 3.6$ V	20[2]	–	2,000	mV/msec

NOTES:
1. The measurement condition is T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. This condition (the minimum value of external power V_{CC} rise gradient) does not apply if $V_{por2} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 1 reset by setting the LVD1ON bit in the OFS register to 0, the VW1C0 and VW1C6 bits in the VW1C register to 1 respectively, and the VCA26 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30 s or more if -20°C $\leq T_{opr} \leq$ 125°C, maintain $t_{w(por1)}$ for 3,000 s or more if -40°C $\leq T_{opr} <$ -20°C.

NOTES:
1. When using the voltage monitor 1 digital filter, ensure VCC is 2.0 V or higher during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
3. V_{det1} indicates the voltage detection level of the voltage detection 1 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.

Figure 5.22   Reset Circuit Electrical Characteristics

Figure 5.24   I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

Table 5.54   Electrical Characteristics (4) [Vcc = 3 V]
(Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5	9	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	70	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	55	μA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.7	3.0	μA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.1	–	μA
			XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	3.8	–	μA

		REVISION HISTORY	R8C/28 Group, R8C/29 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Nov 08, 2006	15	Table 4.1; • "0000h to 003Fh" → "0000h to 002Fh" revised • 000Fh: "000XXXXXb" → "00X11111b" revised • 001Ch: "00h" → "00h, 10000000b" revised • 0029h: "High-Speed On-Chip Oscillator Control Register 4, FRA4, When shipping" added • 002Bh: "High-Speed On-Chip Oscillator Control Register 6, FRA6, When shipping" added • NOTE2 revised, NOTE3 added
		16	Table 4.2; "0040h to 007Fh" → "0030h to 007Fh" revised
		18	Table 4.4; 00E1h, 00E5h, 00E8h "XXh" → "00h" revised
		22	Table 5.2 revised
		23	Figure 5.1 figure title revised
		24	Table 5.4 revised
		25	Table 5.5 revised
		26	Figure 5.2 figure title revised and Table 5.7 NOTE4 added
		27	Table 5.9 revised, Figure 5.3 revised
		28	Table 5.10, Table 5.11 revised
		34	Table 5.15 revised
		35	Table 5.16 revised
		36	Table 5.17 revised
		39	Table 5.22 revised
		40	Table 5.23 revised
		44	Table 5.29 revised
		47	5.2 "J and K versions are under development...notice." added Table 5.34, Table 5.35 revised
		48	Table 5.36 revised, Figure 5.20 figure title revised
		51	Figure 5.21 figure title revised
		52	Table 5.41, Figure 5.22 revised
		53	Table 5.42, Table 5.43 revised
		59	Table 5.47 revised
		60	Table 5.48 revised
		63	Table 5.53 revised
		64	Table 5.54 revised
		67	Package Dimensions; "Diagrams showing the latest...website." added
1.10	May 17, 2007	2	Table 1.1 revised
		3	Table 1.2 revised
		5	Table 1.3 and Figure 1.2 revised
		6	Table 1.4 and Figure 1.3 revised
		7	Figure 1.4 NOTE4 added

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