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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	40MHz
Non-Volatile Memory	External
On-Chip RAM	20kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2184lbstz-160

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting ADSP-218xL series members to fetch two operands in a single cycle, one from program memory and one from data memory. ADSP-218xL series members can fetch an operand from program memory and the next instruction in the same cycle.

In lieu of the address and data bus for external memory connection, ADSP-218xL series members can be configured for 16-bit Internal DMA port (IDMA port) connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSP's on-chip program and data RAM.

An interface to low cost, byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$, and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-218xL to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

ADSP-218xL series members can respond to eleven interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORT), the BDMA port, and the power-down circuitry. There is also a master $\overline{RESET}$ signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation. Each serial port can generate an internal programmable serial clock or accept an external serial clock.

ADSP-218xL series members provide up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, eight flags are programmable as inputs or outputs, and three flags are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) decrements every n processor cycle, where n is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

ADSP-218xL series members incorporate two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Following is a brief list of the capabilities of the ADSP-218xL SPORTs. For additional information on Serial Ports, refer to the *ADSP-218x DSP Hardware Reference*.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulse widths and timings.
- SPORTs support serial data word lengths from 3 bits to 16 bits and provide optional A-law and μ-law companding, according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24-word or 32-word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts ($\overline{IRQ0}$ and $\overline{IRQ1}$) and the FI and FO signals. The internally generated serial clock may still be used in this configuration.

MODES OF OPERATION

The ADSP-218xL series modes of operation appear in Table 2. Only the ADSP-2187L provides Mode D operation

Setting Memory Mode

Memory Mode selection for the ADSP-218xL series is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP's PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are active and passive.

Passive Configuration

Passive Configuration involves the use of a pull-up or pull-down resistor connected to the Mode C pin. To minimize power consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down resistance, on the order of 10 kΩ, can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor's output driver. For minimum power consumption

faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of n processor cycles).

SYSTEM INTERFACE

Figure 2 shows typical basic system configurations with the ADSP-218xL series, two serial devices, a byte-wide EPROM, and optional external program and data overlay memories (mode-selectable). Programmable wait state generation allows the processor to connect easily to slow peripheral devices. ADSP-218xL series members also provide four external interrupts and two serial ports or six external interrupts and one serial port. Host Memory Mode allows access to the full external data bus, but limits addressing to a single address bit (A0). Through the use of external hardware, additional system peripherals can be added in this mode to generate and latch address signals.

Clock Signals

ADSP-218xL series members can be clocked by either a crystal or a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation, nor operated below the specified frequency during normal operation. The only exception is while the processor is in the power-down state. For additional information, refer to the *ADSP-218x DSP Hardware Reference*, for detailed information on this power-down feature.

If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL pin must be left unconnected.

ADSP-218xL series members use an input clock with a frequency equal to half the instruction rate; a 40 MHz input clock yields a 12.5 ns processor cycle (which is equivalent to 80 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because ADSP-218xL series members include an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 3. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used. To provide an adequate feedback path around the internal amplifier circuit, place a resistor in parallel with the circuit, as shown in Figure 3.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 Autobuffer Control Register.

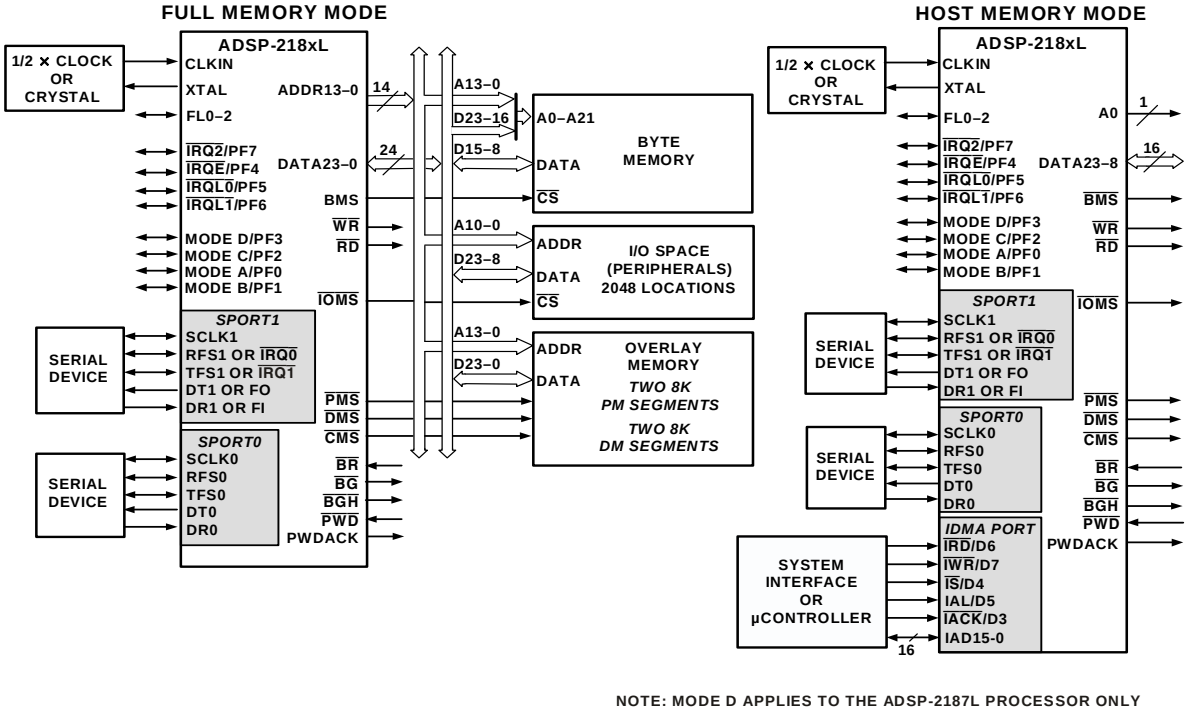

Figure 2. Basic System Interface

Table 4. PMOVLAY Bits

Processor	PMOVLAY	Memory	A13	A12–0
ADSP-2184L	No internal overlay region	Not Applicable	Not applicable	Not applicable
ADSP-2185L	0	Internal overlay	Not applicable	Not applicable
ADSP-2186L	No internal overlay region	Not applicable	Not applicable	Not applicable
ADSP-2187L	0, 4, 5	Internal overlay	Not applicable	Not applicable
All Processors	1	External overlay 1	0	13 LSBs of address between 0x2000 and 0x3FFF
All Processors	2	External overlay 2	1	13 LSBs of address between 0x2000 and 0x3FFF

Table 5. DMOVLAY Bits

Processor	DMOVLAY	Memory	A13	A12–0
ADSP-2184L	No internal overlay region	Not applicable	Not applicable	Not applicable
ADSP-2185L	0	Internal overlay	Not applicable	Not applicable
ADSP-2186L	No internal overlay region	Not applicable	Not applicable	Not applicable
ADSP-2187L	0, 4, 5	Internal overlay	Not applicable	Not applicable
All Processors	1	External overlay 1	0	13 LSBs of address between 0x0000 and 0x1FFF
All Processors	2	External overlay 2	1	13 LSBs of address between 0x0000 and 0x1FFF

I/O Space (Full Memory Mode)

ADSP-218xL series members support an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit wide data. The lower eleven bits of the external address bus are used; the upper three bits are undefined.

Two instructions were added to the core ADSP-2100 family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated 3-bit wait state registers, IOWAIT0–3 as shown in Figure 8, which specify up to seven wait states to be automatically generated for each of four regions. The wait states act on address ranges, as shown in Table 6.

Note: In Full Memory Mode, all 2048 locations of I/O space are directly addressable. In Host Memory Mode, only address pin A0 is available; therefore, additional logic is required externally to achieve complete addressability of the 2048 I/O space locations.

Table 6. Wait States

Address Range	Wait State Register
0x000–0x1FF	IOWAIT0
0x200–0x3FF	IOWAIT1
0x400–0x5FF	IOWAIT2
0x600–0x7FF	IOWAIT3

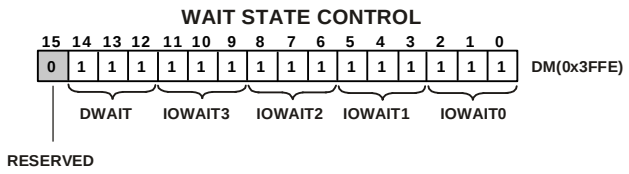

Figure 8. Wait State Control Register

Composite Memory Select

ADSP-218xL series members have a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality. Each bit in the CMSSEL register, when set, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory, and use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All enable bits default to 1 at reset, except the $\overline{\text{BMS}}$ bit.

create a destination word, it is transferred to or from on-chip memory. The transfer takes one DSP cycle. DSP accesses to external memory have priority over BDMA byte memory accesses.

The BDMA Context Reset bit (BCR) controls whether the processor is held off while the BDMA accesses are occurring. Setting the BCR bit to 0 allows the processor to continue operations. Setting the BCR bit to 1 causes the processor to stop execution while the BDMA accesses are occurring, to clear the context of the processor, and start execution at address 0 when the BDMA accesses have completed.

The BDMA overlay bits specify the OVLAY memory blocks to be accessed for internal memory. Set these bits as indicated in Figure 11.

Note: BDMA cannot access external overlay memory regions 1 and 2.

The BMWAIT field, which has 3 bits on ADSP-218xL series members, allows selection of up to 7 wait states for BDMA transfers.

Internal Memory DMA Port (IDMA Port; Host Memory Mode)

The IDMA Port provides an efficient means of communication between a host system and ADSP-218xL series members. The port is used to access the on-chip program memory and data memory of the DSP with only one DSP cycle per word overhead. The IDMA port cannot, however, be used to write to the DSP's memory-mapped control registers. A typical IDMA transfer process is shown as follows:

1. Host starts IDMA transfer.
2. Host checks $\overline{\text{IACK}}$ control line to see if the DSP is busy.
3. Host uses $\overline{\text{IS}}$ and IAL control lines to latch either the DMA starting address (IDMAA) or the PM/DM OVLAY selection into the DSP's IDMA control registers. If Bit 15 = 1, the values of Bits 7–0 represent the IDMA overlay; Bits 14–8 must be set to 0. If Bit 15 = 0, the value of Bits 13–0 represent the starting address of internal memory to be accessed and Bit 14 reflects PM or DM for access. Set IDDMOVLAY and IDPMOVLAY bits in the IDMA overlay register as indicted in Table 8.
4. Host uses $\overline{\text{IS}}$ and $\overline{\text{IRD}}$ (or $\overline{\text{IWR}}$) to read (or write) DSP internal memory (PM or DM).
5. Host checks $\overline{\text{IACK}}$ line to see if the DSP has completed the previous IDMA operation.
6. Host ends IDMA transfer.

Table 8. IDMA/BDMA Overlay Bits

Processor	IDMA/BDMA PMOVLAY	IDMA/BDMA DMOVLAY
ADSP-2184L	0	0
ADSP-2185L	0	0
ADSP-2186L	0	0
ADSP-2187L	0, 4, 5	0, 4, 5

The IDMA port has a 16-bit multiplexed address and data bus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written while the ADSP-218xL is operating at full speed.

The DSP memory address is latched and then automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location, the destination type specifies whether it is a DM or PM access. The falling edge of the IDMA address latch signal (IAL) or the missing edge of the IDMA select signal ($\overline{\text{IS}}$) latches this value into the IDMAA register.

Once the address is stored, data can be read from, or written to, the ADSP-218xL's on-chip memory. Asserting the select line ($\overline{\text{IS}}$) and the appropriate read or write line ($\overline{\text{IRD}}$ and $\overline{\text{IWR}}$ respectively) signals the ADSP-218xL that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented, and another access can occur.

Through the IDMAA register, the DSP can also specify the starting address and data format for DMA operation. Asserting the IDMA port select ($\overline{\text{IS}}$) and address latch enable (IAL) directs the ADSP-218xL to write the address onto the IAD14–0 bus into the IDMA Control Register (Figure 12). If Bit 15 is set to 0, IDMA latches the address. If Bit 15 is set to 1, IDMA latches into the OVLAY register. This register, also shown in Figure 12, is memory-mapped at address DM (0x3FE0). Note that the latched address (IDMAA) cannot be read back by the host. The IDMA Overlay register applies to The ADSP-2187L processor only.

When Bit 14 in 0x3FE7 is set to zero, short reads use the timing shown in Figure 26 on Page 34. When Bit 14 in 0x3FE7 is set to 1, timing in Figure 27 on Page 35 applies for short reads in Short Read Only Mode. Set IDDMOVLAY and IDPMOVLAY bits in the IDMA overlay register as indicated in Table 8. Refer to the *ADSP-218x DSP Hardware Reference* for additional details.

Note: In Full Memory Mode, all locations of 4M-byte memory space are directly addressable. In Host Memory Mode, only address pin A0 is available, requiring additional external logic to provide address information for the byte.

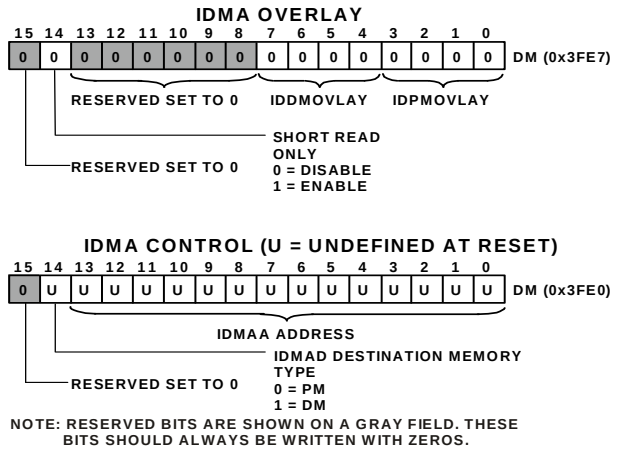

Figure 12. IDMA OVLAY/Control Registers

Bootstrap Loading (Booting)

ADSP-218xL series members have two mechanisms to allow automatic loading of the internal program memory after reset. The method for booting is controlled by the Mode A, Mode B, and Mode C configuration bits.

When the mode pins specify BDMA booting, the ADSP-218xL initiates a BDMA boot sequence when reset is released.

The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD, and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24-bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory. These 32 words are used to set up the BDMA to load in the remaining program code. The BCR bit is also set to 1, which causes program execution to be held off until all 32 words are loaded into on-chip program memory. Execution then begins at address 0.

The ADSP-2100 Family development software (Revision 5.02 and later) fully supports the BDMA booting feature and can generate byte memory space-compatible boot code.

The IDLE instruction can also be used to allow the processor to hold off execution while booting continues through the BDMA interface. For BDMA accesses while in Host Mode, the addresses to boot memory must be constructed externally to the ADSP-218xL. The only memory address bit provided by the processor is A0.

IDMA Port Booting

ADSP-218xL series members can also boot programs through its internal DMA port. If Mode C = 1, Mode B = 0, and Mode A = 1, the ADSP-218xL boots from the IDMA port. IDMA feature can load as much on-chip memory as desired. Program execution is held off until the host writes to on-chip program memory location 0.

BUS REQUEST AND BUS GRANT

ADSP-218xL series members can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the Bus Request ($\overline{BR}$) signal. If the ADSP-218xL is not performing an external memory access, it responds to the active $\overline{BR}$ input in the following processor cycle by:

- Three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- Asserting the bus grant ($\overline{BG}$) signal, and
- Halting program execution.

If Go Mode is enabled, the ADSP-218xL will not halt program execution until it encounters an instruction that requires an external memory access.

If an ADSP-218xL series member is performing an external memory access when the external device asserts the $\overline{BR}$ signal, it will not three-state the memory interfaces nor assert the $\overline{BG}$ signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, re-enables the output drivers, and continues program execution from the point at which it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The $\overline{BGH}$ pin is asserted when an ADSP-218xL series member requires the external bus for a memory or BDMA access, but is stopped. The other device can release the bus by deasserting bus request. Once the bus is released, the ADSP-218xL deasserts $\overline{BG}$ and $\overline{BGH}$ and executes the external memory access.

FLAG I/O PINS

ADSP-218xL series members have eight general-purpose programmable input/output flag pins. They are controlled by two memory-mapped registers. The PFTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the ADSP-218xL's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

In addition to the programmable flags, ADSP-218xL series members have five fixed-mode flags, FI, FO, FL0, FL1, and FL2. FL0 to FL2 are dedicated output flags. FI and FO are available as an alternate configuration of SPORT1.

Note: Pins PF0, PF1, PF2, and PF3 are also used for device configuration during reset.

- Complete assembly and disassembly of instructions
- C source-level debugging

Designing an EZ-ICE-Compatible System

ADSP-218xL series members have on-chip emulation support and an ICE-Port, a special set of pins that interface to the EZ-ICE. These features allow in-circuit emulation without replacing the target system processor by using only a 14-pin connection from the target system to the EZ-ICE. Target systems must have a 14-pin connector to accept the EZ-ICE's in-circuit probe, a 14-pin plug.

Issuing the chip reset command during emulation causes the DSP to perform a full chip reset, including a reset of its memory mode. Therefore, it is vital that the mode pins are set correctly PRIOR to issuing a chip reset command from the emulator user interface. If a passive method of maintaining mode information is being used (as discussed in Setting Memory Mode on Page 4), it does not matter that the mode information is latched by an emulator reset. However, if the $\overline{\text{RESET}}$ pin is being used as a method of setting the value of the mode pins, the effects of an emulator reset must be taken into consideration.

One method of ensuring that the values located on the mode pins are those desired is to construct a circuit like the one shown in Figure 13. This circuit forces the value located on the Mode A pin to logic high, regardless of whether it is latched via the $\overline{\text{RESET}}$ or $\overline{\text{ERESET}}$ pin.

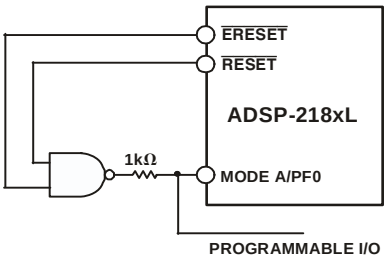

Figure 13. Mode A Pin/EZ-ICE Circuit

The ICE-Port interface consists of the following ADSP-218xL pins: $\overline{\text{EBR}}$, $\overline{\text{EINT}}$, EE, $\overline{\text{EBG}}$, ECLK, $\overline{\text{ERESET}}$, ELIN, $\overline{\text{EMS}}$, and ELOUT.

These ADSP-218xL pins must be connected only to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the ADSP-218xL and the connector must be kept as short as possible, no longer than 3 inches.

The following pins are also used by the EZ-ICE: $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{RESET}}$, and GND.

The EZ-ICE uses the EE (emulator enable) signal to take control of the ADSP-218xL in the target system. This causes the processor to use its $\overline{\text{ERESET}}$, $\overline{\text{EBR}}$, and $\overline{\text{EBG}}$ pins instead of the $\overline{\text{RESET}}$, $\overline{\text{BR}}$, and $\overline{\text{BG}}$ pins. The $\overline{\text{BG}}$ output is three-stated. These signals do not need to be jumper-isolated in the system.

The EZ-ICE connects to the target system via a ribbon cable and a 14-pin female plug. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.

Target Board Connector for EZ-ICE Probe

The EZ-ICE connector (a standard pin strip header) is shown in Figure 14. This connector must be added to the target board design to use the EZ-ICE. Be sure to allow enough room in the system to fit the EZ-ICE probe onto the 14-pin connector.

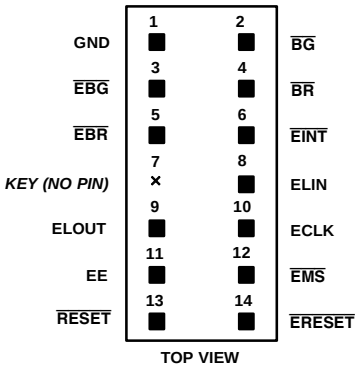

Figure 14. Target Board Connector for EZ-ICE

The 14-pin, 2-row pin strip header is keyed at the Pin 7 location—Pin 7 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inch. The pin strip header must have at least 0.15 inch clearance on all sides to accept the EZ-ICE probe plug.

Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

Target Memory Interface

For the target system to be compatible with the EZ-ICE emulator, it must comply with the following memory interface guidelines:

Design the Program Memory (PM), Data Memory (DM), Byte Memory (BM), I/O Memory (IOM), and Composite Memory (CM) external interfaces to comply with worst-case device timing requirements and switching characteristics as specified in this data sheet. The performance of the EZ-ICE may approach published worst-case specification for some memory access timing requirements and switching characteristics.

Note: If the target does not meet the worst-case chip specification for memory access parameters, the circuitry may not be able to be emulated at the desired CLKIN frequency. Depending on the severity of the specification violation, the system may be difficult to manufacture, as DSP components statistically vary in switching characteristic and timing requirements, within published limits.

Restriction: All memory strobe signals on the ADSP-218xL ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{CMS}}$, and $\overline{\text{IOMS}}$) used in the target system must have 10 kΩ pull-up resistors connected when the EZ-ICE is being used. The pull-up resistors are necessary

Table 9. Common-Mode Pins (Continued)

Pin Name	No. of Pins	I/O	Function
V_{DDINT}	4	I	Internal V_{DD} (3.3 V) Power (BGA)
V_{DDEXT}	7	I	External V_{DD} (3.3 V) Power (BGA)
GND	20	I	Ground (BGA)
EZ-Port	9	I/O	For Emulation Use

[1] Interrupt/Flag pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices or set as a programmable flag.
[2] This mode applies to the ADSP-2187L only.
[3] SPORT configuration determined by the DSP System Control Register. Software configurable.

MEMORY INTERFACE PINS

ADSP-218xL series members can be used in one of two modes: Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities.

The operating mode is determined by the state of the Mode C pin during $\overline{\text{RESET}}$ and cannot be changed while the processor is running. Table 10 and Table 11 list the active signals at specific pins of the DSP during either of the two operating modes (Full Memory or Host). A signal in one table shares a pin with a signal from the other table, with the active signal determined by the mode that is set. For the shared pins and their alternate signals (e.g., A4/IAD3), refer to the package pinouts in Table 29 on Page 44 and Table 30 on Page 45.

Table 10. Full Memory Mode Pins (Mode C = 0)

Pin Name	No. of Pins	I/O	Function
A13–0	14	O	Address Output Pins for Program, Data, Byte, and I/O Spaces
D23–0	24	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces (8 MSBs are also used as Byte Memory Addresses.)

Table 11. Host Mode Pins (Mode C = 1)

Pin Name	No. of Pins	I/O	Function
IAD15–0	16	I/O	IDMA Port Address/Data Bus
A0	1	O	Address Pin for External I/O, Program, Data, or Byte Access[1]
D23–8	16	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces
$\overline{\text{IWR}}$	1	I	IDMA Write Enable
$\overline{\text{IRD}}$	1	I	IDMA Read Enable
IAL	1	I	IDMA Address Latch Pin
$\overline{\text{IS}}$	1	I	IDMA Select
$\overline{\text{IACK}}$	1	O	IDMA Port Acknowledge Configurable in Mode D[2]; Open Drain

[1] In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{\text{CMS}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{IOMS}}$ signals.
[2] Mode D function available on ADSP-2187L only.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed below may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Rating
Supply Voltage (V_{DD})	–0.3 V to +4.6 V
Input Voltage[1]	–0.5 V to V_{DD} + 0.5 V
Output Voltage Swing[2]	–0.5 V to V_{DD} +0.5 V
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C

[1] Applies to bidirectional pins (D23–0, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A13–1, PF7–0) and input only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).
[2] Applies to output pins ($\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$).

PACKAGE INFORMATION

The information presented in Figure 15 provides details about the package branding for the ADSP-218xL processors. For a complete listing of product availability, see Ordering Guide on Page 47.

Figure 15. Typical Package Brand

Table 13. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHs Compliant Option (optional)
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

General Notes

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, parameters cannot be added up meaningfully to derive longer times.

Timing Notes

Switching characteristics specify how the processor changes its signals. Designers have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell what the processor will do in a given circumstance. Switching characteristics can also be used to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Frequency Dependency For Timing Specifications

t_{CK} is defined as 0.5 t_{CKI}. The ADSP-218xL uses an input clock with a frequency equal to half the instruction rate. For example, a 26 MHz input clock (which is equivalent to 38 ns) yields a 19 ns processor cycle (equivalent to 52 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain the specification value.

Example: t_{CKH} = 0.5 t_{CK} – 7 ns = 0.5 (19) – 7 ns = 2.5 ns

Clock Signals and Reset

Table 14. Clock Signals and Reset

Parameter		ADSP-2184L, ADSP-2186L Min	ADSP-2184L, ADSP-2186L Max	ADSP-2185L, ADSP-2187L Min	ADSP-2185L, ADSP-2187L Max	Unit
Timing Requirements:						
t_{CKI}	CLKIN Period	50	150	38	100	ns
t_{CKIL}	CLKIN Width Low	20		15		ns
t_{CKIH}	CLKIN Width High	20		15		ns
Switching Characteristics:						
t_{CKL}	CLKOUT Width Low	$0.5t_{CK} - 7$		$0.5t_{CK} - 7$		ns
t_{CKH}	CLKOUT Width High	$0.5t_{CK} - 7$		$0.5t_{CK} - 7$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	0	20	ns
Control Signals Timing Requirements:						
t_{RSP}	$\overline{\text{RESET}}$ Width Low[1]	$5t_{CK}$		$5t_{CK}$		ns
t_{MS}	Mode Setup Before $\overline{\text{RESET}}$ High	2		2		ns
t_{MH}	Mode Hold After $\overline{\text{RESET}}$ High	5		5		ns

[1] Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles, assuming stable CLKIN (not including crystal oscillator start-up time).

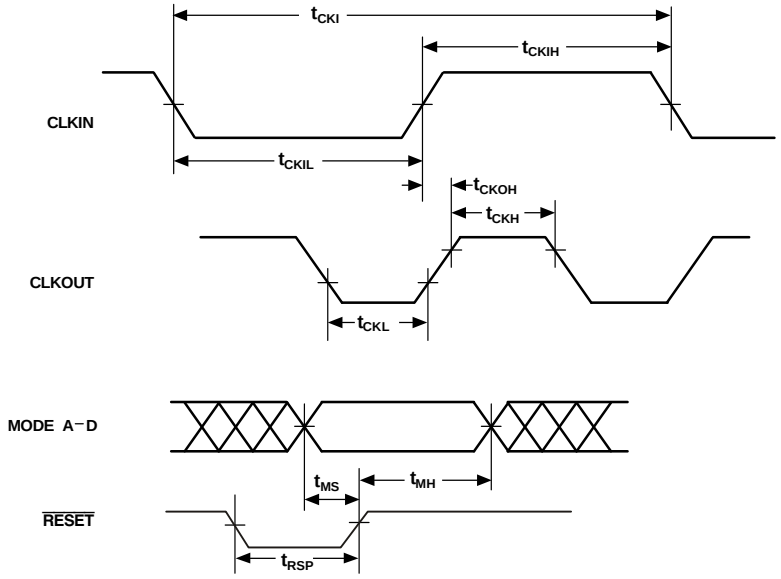

Figure 16. Clock Signals and Reset

Bus Request–Bus Grant

Table 16. Bus Request—Bus Grant

Parameter		Min	Max	Unit
Timing Requirements:				
t_{BH}	$\overline{BR}$ Hold After CLKOUT High[1]	$0.25t_{CK} + 2$		ns
t_{BS}	$\overline{BR}$ Setup Before CLKOUT Low[1]	$0.25t_{CK} + 17$		ns
Switching Characteristics:				
t_{SD}	CLKOUT High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable[2]		$0.25t_{CK} + 10$	ns
t_{SDB}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High[3]	$0.25t_{CK} - 7$		ns
t_{SDBH}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[4]	0		ns
t_{SEH}	$\overline{BGH}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable[4]	0		ns

[1] $\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual* for $\overline{BR}$/BG cycle relationships.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.
[3] For the ADSP-2187L, this specification is $0.25t_{CK}$ – 4 ns min.
[4] $\overline{BGH}$ is asserted when the bus is granted and the processor or BDMA requires control of the bus to continue.

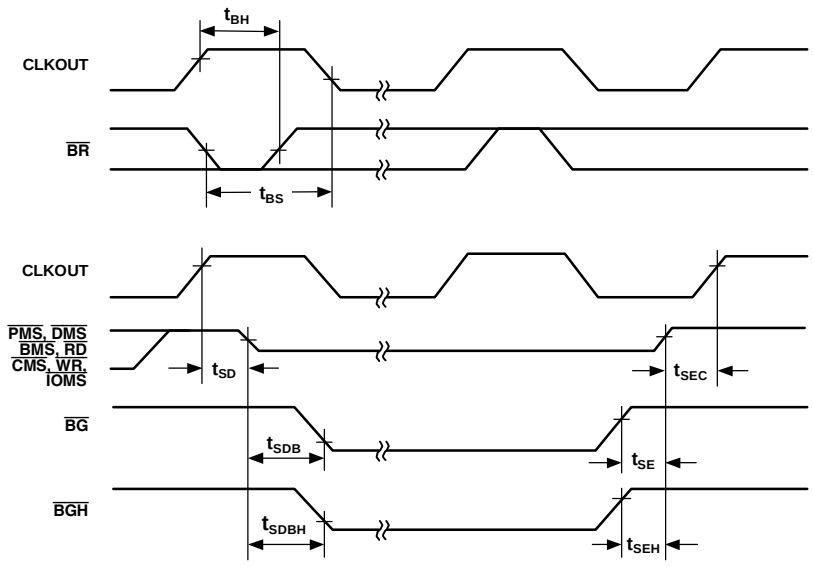

Figure 18. Bus Request—Bus Grant

Memory Write

Table 18. Memory Write

Parameter		Min	Max	Unit
Switching Characteristics:				
t_{DW}	Data Setup Before $\overline{WR}$ High[1]	$0.5t_{CK}$– 7 + w		ns
t_{DH}	Data Hold After $\overline{WR}$ High	$0.25t_{CK}$ – 2		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK}$ – 5 + w		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A13–0, $\overline{xMS}$ Setup Before $\overline{WR}$ Low[2]	$0.25t_{CK}$ – 6		ns
t_{DDR}	Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK}$ – 7		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK}$ – 5	$0.25t_{CK}$ + 7	ns
t_{AW}	A13–0, $\overline{xMS}$ Setup Before $\overline{WR}$ Deasserted	$0.75t_{CK}$ – 9 + w		ns
t_{WRA}	A13–0, $\overline{xMS}$ Hold After $\overline{WR}$ Deasserted	$0.25t_{CK}$ – 3		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK}$ – 5		ns

[1] w = wait states × t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

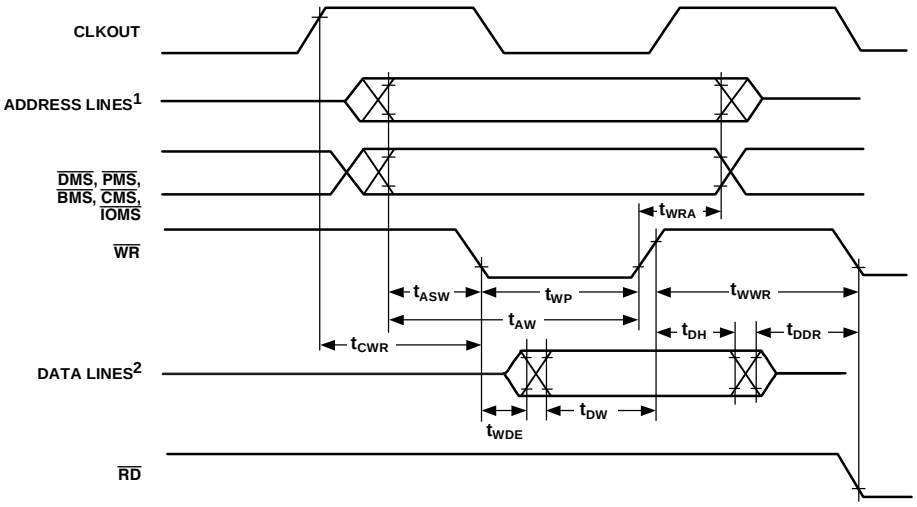

Figure 20. Memory Write

Serial Ports

Table 19. Serial Ports

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SCK}	SCLK Period[1]	50		ns
t_{SCS}	DR/TFS/RFS Setup Before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold After SCLK Low[2]	8		ns
t_{SCP}	SCLKIN Width[3]	20		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to SCLKOUT	$0.25t_{CK}$	$0.25t_{CK} + 10$	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		15	ns
t_{RH}	TFS/RFS_{OUT} Hold After SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		15	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		14	ns
t_{SCDD}	SCLK High to DT Disable		15	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		15	ns

[1] For the ADSP-2187L, this specification is 38 ns min.
[2] For the ADSP-2187L, this specification is 7 ns min.
[3] For the ADSP-2185L, and the ADSP-2187L, this specification is 15 ns min.

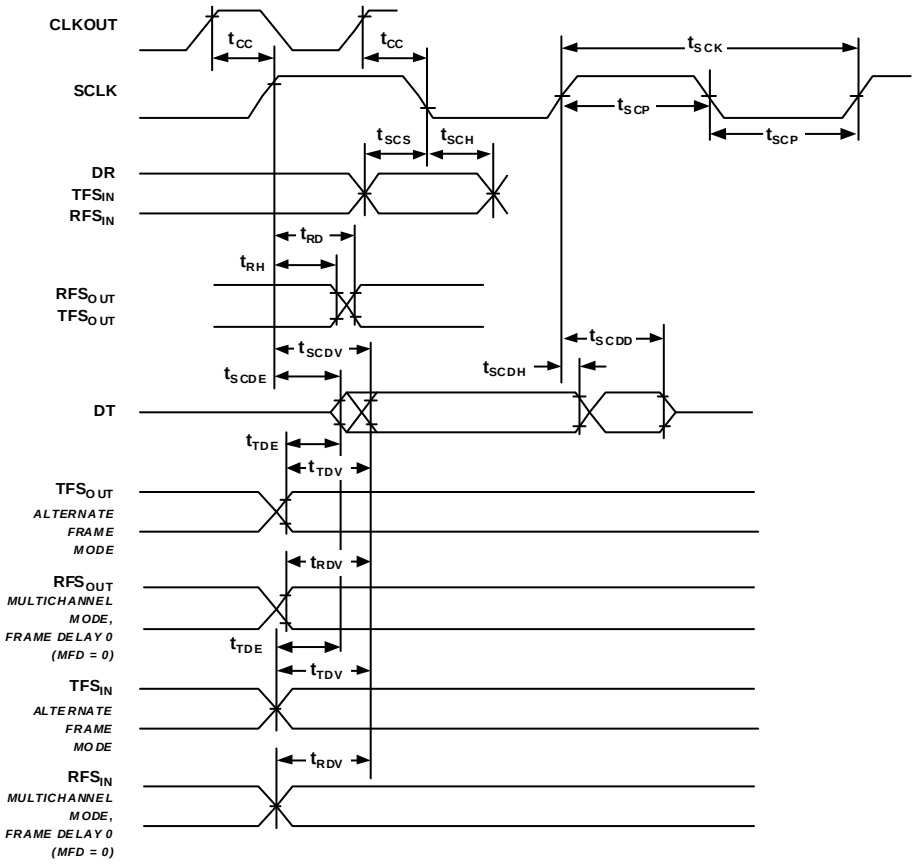

Figure 21. Serial Ports

IDMA Write, Long Write Cycle

Table 22. IDMA Write, Long Write Cycle

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low Before Start of Write[1]	0		ns
t_{IKSU}	IAD15–0 Data Setup Before End of Write[2, 3, 4]	$0.5t_{CK} + 10$		ns
t_{IKH}	IAD15–0 Data Hold After End of Write[2, 3, 4]	2		ns
Switching Characteristics:				
t_{IKLW}	Start of Write to $\overline{IACK}$ Low[4]	$1.5t_{CK}$		ns
t_{IKHW}	Start of Write to $\overline{IACK}$ High[5]		17	ns

[1] Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2] If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[3] If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.
[4] This is the earliest time for $\overline{IACK}$ Low from Start of Write. For IDMA Write cycle relationships, please refer to the *ADSP-2100 Family User's Manual*.
[5] For the ADSP-2185L, and the ADSP-2187L, this specification is 4 ns min., and 15 ns max.

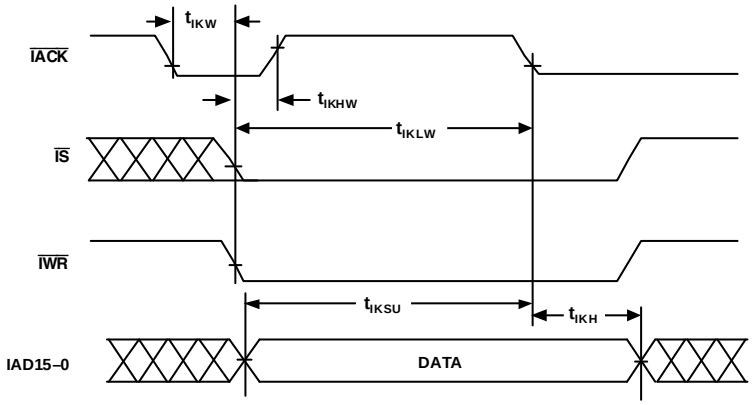

Figure 24. IDMA Write, Long Write Cycle

IDMA Read, Short Read Cycle in Short Read Only Mode

Table 25. IDMA Read, Short Read Cycle in Short Read Only Mode[1]

Parameter[2]		Min	Max	Unit
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low Before Start of Read[3]	0		ns
t_{IRP}	Duration of Read[4]	10		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High After Start of Read[3]		10	ns
t_{IKDH}	IAD15–0 Previous Data Hold After End of Read[4]	0		ns
t_{IKDD}	IAD15–0 Previous Data Disabled After End of Read[4]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled After Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid After Start of Read		10	ns

[1] Applies to the ADSP-2187L only.
[2] Short Read Only is enabled by setting Bit 14 of the IDMA overlay Register to 1 (0x3FE7). Short Read Only can be enabled by the processor core writing to the register or by an external host writing to the register. Disabled by default.
[3] Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low. Previous data remains until end of read.
[4] End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

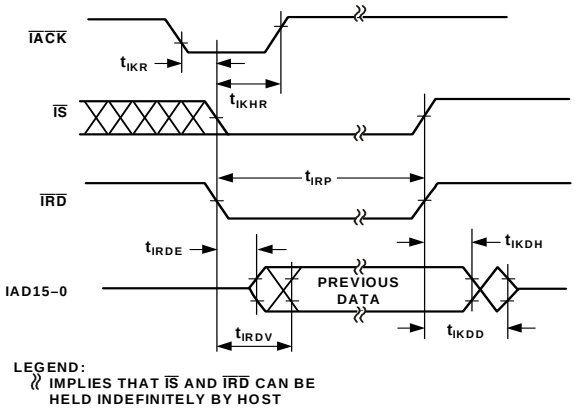

Figure 27. IDMA Read, Short Read Cycle in Short Read Only Mode

OUTPUT DRIVE CURRENTS

Figure 32 through Figure 35 show typical I-V characteristics for the output drivers on the ADSP-218xL processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

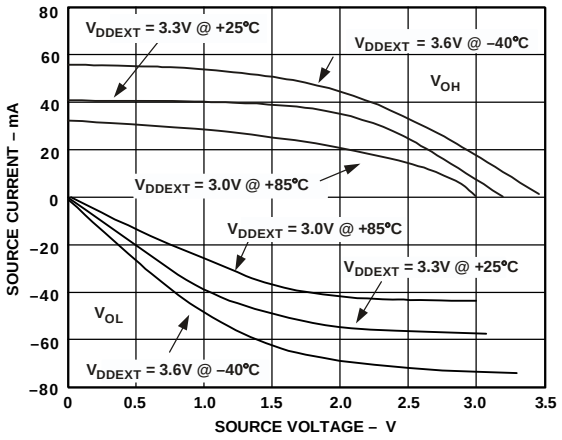

Figure 32. Typical Output Driver Characteristics (ADSP-2184L)

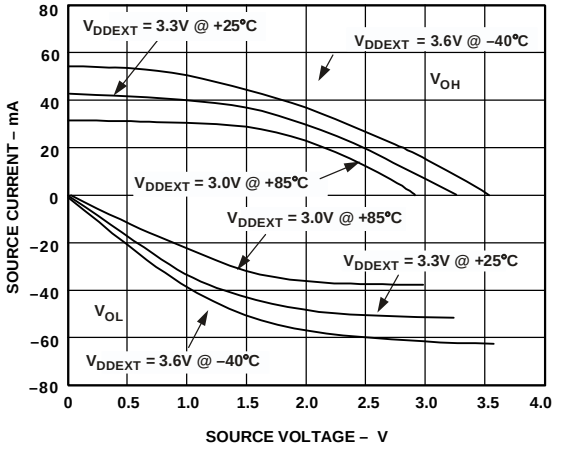

Figure 33. Typical Output Driver Characteristics (ADSP-2185L)

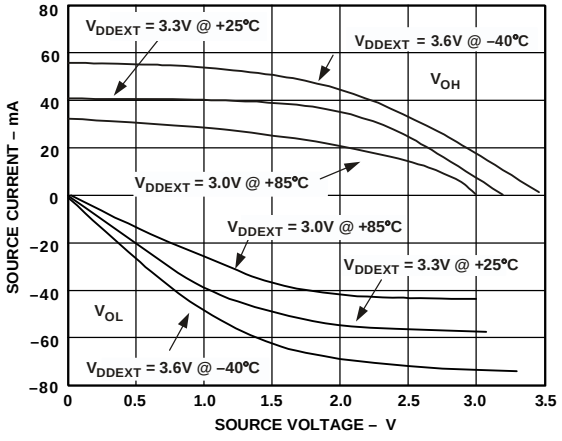

Figure 34. Typical Output Driver Characteristics (ADSP-2186L)

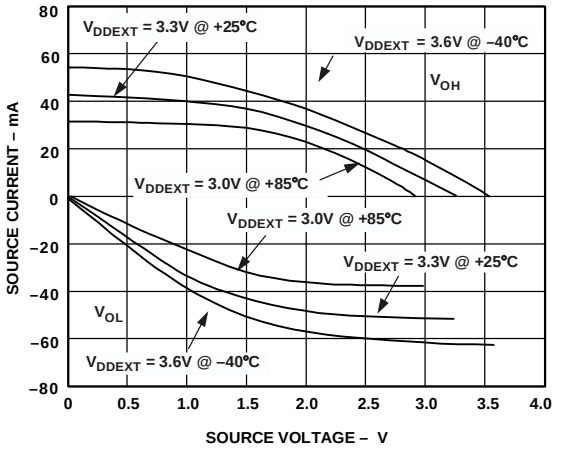

Figure 35. Typical Output Driver Characteristics (ADSP-2187L)

CAPACITIVE LOADING – ADSP-2184L, ADSP-2186L

Figure 40 and Figure 41 show the capacitive loading characteristics of the ADSP-2184L and ADSP-2186L.

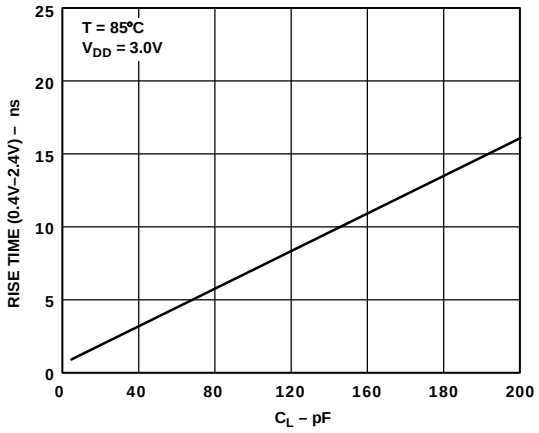

Figure 40. Typical Output Rise Time vs. Load Capacitance (at Maximum Ambient Operating Temperature)

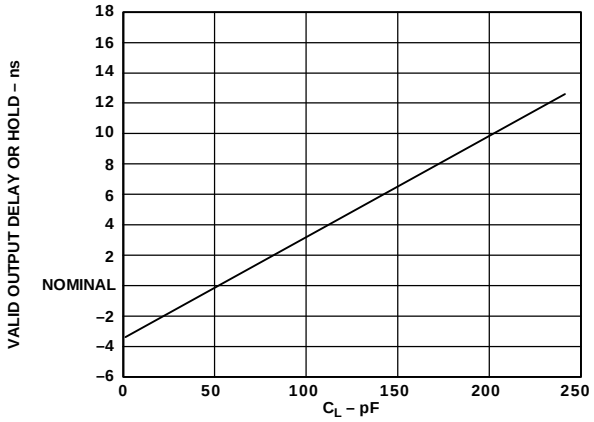

Figure 41. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

CAPACITIVE LOADING – ADSP-2185L, ADSP-2187L

Figure 42 and Figure 43 show the capacitive loading characteristics of the ADSP-2185L and ADSP-2187L.

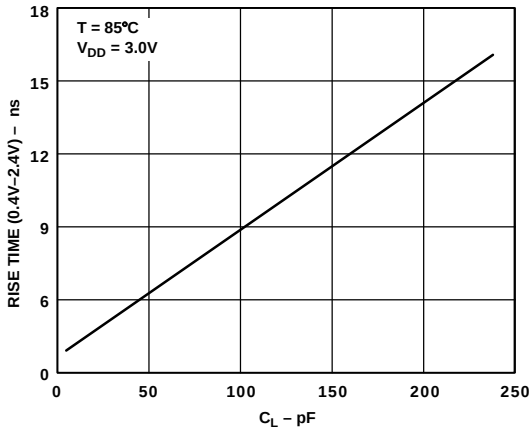

Figure 42. Typical Output Rise Time vs. Load Capacitance (at Maximum Ambient Operating Temperature)

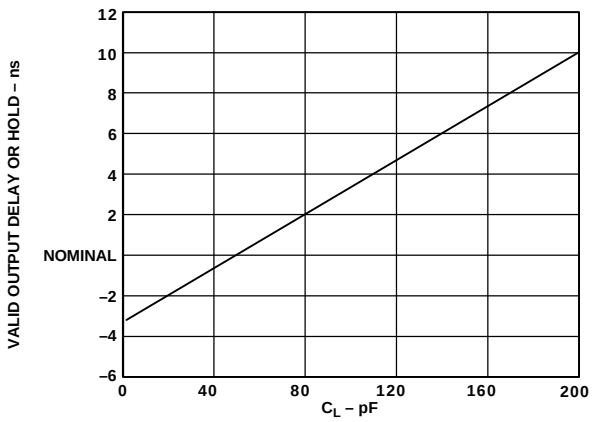

Figure 43. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

Figure 44 shows voltage reference levels for all ac measurements (except output disable/enable).

Figure 44. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 45. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 45. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

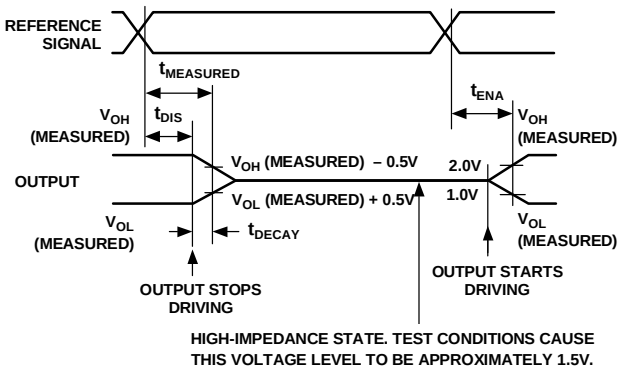

Figure 45. Output Enable/Disable

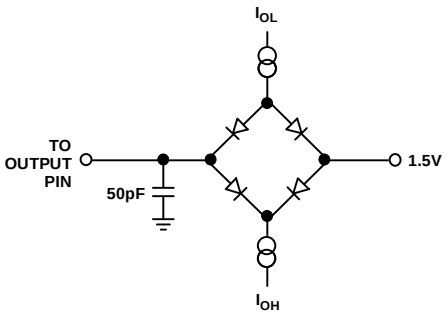

Figure 46. Equivalent Loading for AC Measurements (Including All Fixtures)

ENVIRONMENTAL CONDITIONS

Table 28. Thermal Resistance

Rating Description[1]	Symbol	LQFP (°C/W)	BGA (°C/W)
Thermal Resistance (Case-to-Ambient)	θ_{CA}	48	63.3
Thermal Resistance (Junction-to-Ambient)	θ_{JA}	50	70.7
Thermal Resistance (Junction-to-Case)	θ_{JC}	2	7.4

[1] Where the ambient temperature rating (T_{AMB}) is:
$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = case temperature in °C
PD = power dissipation in W

BGA PACKAGE PINOUT

The BGA package pinout is shown in Table 30. Pin names in bold text in the table replace the plain text named functions when Mode C equals 1. A plus sign (+) separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$. The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default upon reset.

Table 30. BGA Pin Assignments

Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name
A01	A2/**IAD1**	D01	NC	G01	XTAL	K01	NC
A02	A1/**IAD0**	D02	$\overline{\text{WR}}$	G02	NC	K02	NC
A03	GND	D03	NC	G03	GND	K03	NC
A04	A0	D04	$\overline{\text{BGH}}$	G04	A10/**IAD9**	K04	$\overline{\text{BMS}}$
A05	NC	D05	A9/**IAD8**	G05	NC	K05	$\overline{\text{DMS}}$
A06	GND	D06	PF1 [MODE B]	G06	NC	K06	RFS0
A07	NC	D07	PF2 [MODE C]	G07	NC	K07	TFS1/$\overline{\text{IRQ1}}$
A08	NC	D08	NC	G08	D6/**$\overline{\text{IRD}}$**	K08	SCLK1
A09	NC	D09	D13	G09	D5/**IAL**	K09	$\overline{\text{ERESET}}$
A10	D22	D10	D12	G10	NC	K10	$\overline{\text{EBR}}$
A11	GND	D11	NC	G11	NC	K11	$\overline{\text{BR}}$
A12	GND	D12	GND	G12	D4/**$\overline{\text{IS}}$**	K12	$\overline{\text{EBG}}$
B01	A4/**IAD3**	E01	V_{DDEXT}	H01	CLKIN	L01	$\overline{\text{IRQE}}$ + PF4
B02	A3/**IAD2**	E02	V_{DDEXT}	H02	GND	L02	NC
B03	GND	E03	A8/**IAD7**	H03	GND	L03	$\overline{\text{IRQL1}}$ + PF6
B04	NC	E04	FL0	H04	GND	L04	$\overline{\text{IOMS}}$
B05	NC	E05	PF0 [MODE A]	H05	V_{DDINT}	L05	GND
B06	GND	E06	FL2	H06	DT0	L06	$\overline{\text{PMS}}$
B07	V_{DDEXT}	E07	PF3 [MODE D[1]]	H07	TFS0	L07	DR0
B08	D23	E08	GND	H08	D2/**IAD15**	L08	GND
B09	D20	E09	GND	H09	D3/**$\overline{\text{IACK}}$**	L09	$\overline{\text{RESET}}$
B10	D18	E10	V_{DDEXT}	H10	GND	L10	ELIN
B11	D17	E11	GND	H11	NC	L11	ELOUT
B12	D16	E12	D10	H12	GND	L12	$\overline{\text{EINT}}$
C01	PWDACK	F01	A13/**IAD12**	J01	CLKOUT	M01	$\overline{\text{IRQL0}}$ + PF5
C02	A6/**IAD5**	F02	NC	J02	V_{DDINT}	M02	$\overline{\text{IRQL2}}$ + PF7
C03	$\overline{\text{RD}}$	F03	A12/**IAD11**	J03	NC	M03	NC
C04	A5/**IAD4**	F04	A11/**IAD10**	J04	V_{DDEXT}	M04	$\overline{\text{CMS}}$
C05	A7/**IAD6**	F05	FL1	J05	V_{DDEXT}	M05	GND
C06	$\overline{\text{PWD}}$	F06	NC	J06	SCLK0	M06	DT1/FO
C07	V_{DDEXT}	F07	NC	J07	D0/**IAD13**	M07	DR1/FI
C08	D21	F08	D7/**$\overline{\text{IWR}}$**	J08	RFS1/$\overline{\text{IRQ0}}$	M08	GND
C09	D19	F09	D11	J09	$\overline{\text{BG}}$	M09	NC
C10	D15	F10	D8	J10	D1/**IAD14**	M10	$\overline{\text{EMS}}$
C11	NC	F11	NC	J11	V_{DDINT}	M11	EE
C12	D14	F12	D9	J12	V_{DDINT}	M12	ECLK

[1] Mode D function available on ADSP-2187L only.

SURFACE MOUNT DESIGN

Table 31 is provided as an aid to PCB design to accommodate BGA style surface mount packages. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard.*

Table 31. BGA Data for Use with Surface Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
144-Ball BGA (BC-144-6)	Solder Mask Defined	0.40 mm diameter	0.50 mm diameter

ORDERING GUIDE

Model	Temperature Range[1]	Instruction Rate (MHz)	Package Description	Package Option
ADSP-2184LBST-160	–40°C to +85°C	40	100-Lead LQFP	ST-100-1
ADSP-2184LBSTZ-160[2]	–40°C to +85°C	40	100-Lead LQFP	ST-100-1
ADSP-2185LKST-115	0°C to 70°C	28.8	100-Lead LQFP	ST-100-1
ADSP-2185LKST-133	0°C to 70°C	32.2	100-Lead LQFP	ST-100-1
ADSP-2185LKST-160	0°C to 70°C	40	100-Lead LQFP	ST-100-1
ADSP-2185LKST-210	0°C to 70°C	52.5	100-Lead LQFP	ST-100-1
ADSP-2185LKSTZ-210[2]	0°C to 70°C	52.5	100-Lead LQFP	ST-100-1
ADSP-2185LBST-115	–40°C to +85°C	28.8	100-Lead LQFP	ST-100-1
ADSP-2185LBST-133	–40°C to +85°C	32.2	100-Lead LQFP	ST-100-1
ADSP-2185LBSTZ-133[2]	–40°C to +85°C	32.2	100-Lead LQFP	ST-100-1
ADSP-2185LBST-160	–40°C to +85°C	40	100-Lead LQFP	ST-100-1
ADSP-2185LBSTZ-160[2]	–40°C to +85°C	40	100-Lead LQFP	ST-100-1
ADSP-2185LBST-210	–40°C to +85°C	52.5	100-Lead LQFP	ST-100-1
ADSP-2185LBSTZ-210[2]	–40°C to +85°C	52.5	100-Lead LQFP	ST-100-1
ADSP-2186LKST-115	0°C to 70°C	28.8	100-Lead LQFP	ST-100-1
ADSP-2186LKST-115R[3]	0°C to 70°C	28.8	100-Lead LQFP	ST-100-1
ADSP-2186LKST-133	0°C to 70°C	32.2	100-Lead LQFP	ST-100-1
ADSP-2186LKSTZ-133[2]	0°C to 70°C	32.2	100-Lead LQFP	ST-100-1
ADSP-2186LBST-115	–40°C to +85°C	28.8	100-Lead LQFP	ST-100-1
ADSP-2186LBSTZ-115[2]	–40°C to +85°C	28.8	100-Lead LQFP	ST-100-1
ADSP-2186LBST-160[2]	–40°C to +85°C	40	100-Lead LQFP	ST-100-1
ADSP-2186LBCA-160R[3]	–40°C to +85°C	40	144-Ball BGA	BC-144-6
ADSP-2187LKST-160	0°C to 70°C	40	100-Lead LQFP	ST-100-1
ADSP-2187LKSTZ-160[2]	0°C to 70°C	40	100-Lead LQFP	ST-100-1
ADSP-2187LKST-210	0°C to 70°C	52.5	100-Lead LQFP	ST-100-1
ADSP-2187LKSTZ-210[2]	0°C to 70°C	52.5	100-Lead LQFP	ST-100-1
ADSP-2187LBST-160	–40°C to +85°C	40	100-Lead LQFP	ST-100-1
ADSP-2187LBSTZ-160[2]	–40°C to +85°C	40	100-Lead LQFP	ST-100-1
ADSP-2187LBST-210	–40°C to +85°C	52.5	100-Lead LQFP	ST-100-1
ADSP-2187LBSTZ-210[2]	–40°C to +85°C	52.5	100-Lead LQFP	ST-100-1

[1] Ranges shown represent ambient temperature.
[2] Z = RoHS Compliant Part.
[3] R = Tape and Reel.