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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	52MHz
Non-Volatile Memory	External
On-Chip RAM	80kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2185lbstz-210

TABLE OF CONTENTS

REVISION HISTORY

1/08—Rev. C

This revision of the ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L processor data sheet combines the ADSP-2184L, ADSP-2185L, ADSP-2186L, and ADSP-2187L. This version also contains new RoHS compliant packages.

GENERAL DESCRIPTION

The ADSP-218xL series consists of four single chip microcomputers optimized for digital signal processing applications. The functional block diagram for the ADSP-218xL series members appears in Figure 1 on Page 1. All series members are pin-compatible and are differentiated solely by the amount of on-chip SRAM. This feature, combined with ADSP-21xx code compatibility, provides a great deal of flexibility in the design decision. Specific family members are shown in Table 1.

Table 1. ADSP-218xL DSP Microcomputer Family

Device	Program Memory (K words)	Data Memory (K words)
ADSP-2184L	4	4
ADSP-2185L	16	16
ADSP-2186L	8	8
ADSP-2187L	32	32

ADSP-218xL series members combine the ADSP-2100 family base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, flag I/O, extensive interrupt capabilities, and on-chip program and data memory.

ADSP-218xL series members integrate up to 160K bytes of on-chip memory configured as up to 32K words (24-bit) of program RAM, and up to 32K words (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery-operated portable equipment. The ADSP-218xL is available in 100-lead LQFP and 144-ball BGA packages.

Fabricated using high-speed, low-power, CMOS processes, ADSP-218xL series members operate with a 19 ns instruction cycle time (ADSP-2185L and ADSP-2187L) or a a 25 ns instruction cycle time (ADSP-2184L and ADSP-2186L). Every instruction can execute in a single processor cycle.

The ADSP-218xL's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle, ADSP-218xL series members can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This takes place while the processor continues to:

- Receive and transmit data through the two serial ports
- Receive and/or transmit data through the internal DMA port
- Receive and/or transmit data through the byte DMA port
- Decrement timer

ARCHITECTURE OVERVIEW

The ADSP-218xL series instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-218xL assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

The functional block diagram is an overall block diagram of the ADSP-218xL series. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations.

The shifter can be used to efficiently implement numeric format control, including multiword and block floating-point representations.

The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, ADSP-218xL series members execute looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Five internal buses provide efficient data transfer:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

Individual interrupt requests are logically AND'ed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

ADSP-218xL series members mask all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ external interrupts to be either edge- or level-sensitive. The $\overline{\text{IRQE}}$ pin is an external edge-sensitive interrupt and can be forced and cleared. The $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ pins are external level sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are 12 levels deep to allow interrupt, loop, and subroutine nesting. The following instructions allow global enable or disable servicing of the interrupts (including power-down), regardless of the state of IMASK:

```
ENA INTS;
DIS INTS;
```

Disabling the interrupts does not affect serial port autobuffering or DMA. When the processor is reset, interrupt servicing is enabled.

LOW POWER OPERATION

ADSP-218xL series members have three low-power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

ADSP-218xL series members have a low-power feature that lets the processor enter a very low-power dormant state through hardware or software control. Following is a brief list of power-down features. Refer to the *ADSP-218x DSP Hardware Reference*, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 400 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 400 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits approximately 4096 CLKIN cycles for the crystal oscillator to start or stabilize), and letting the oscillator run to allow 400 CLKIN cycle start-up.
- Power-down is initiated by either the power-down pin ($\overline{\text{PWD}}$) or the software power-down force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate power-down.
- Power-down acknowledge pin (PWDACK) indicates when the processor has entered power-down.

Idle

When the ADSP-218xL is in the Idle Mode, the processor waits indefinitely in a low-power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle Mode IDMA, BDMA, and autobuffer cycle steals still occur.

Slow Idle

The IDLE instruction is enhanced on ADSP-218xL series members to let the processor's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction.

The format of the instruction is:

```
IDLE (n);
```

where n = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT, and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the IDLE (n) instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by n, the clock divisor. When an enabled interrupt is received, ADSP-218xL series members remain in the idle state for up to a maximum of n processor cycles (n = 16, 32, 64, or 128) before resuming normal operation.

When the IDLE (n) instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a

faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of n processor cycles).

SYSTEM INTERFACE

Figure 2 shows typical basic system configurations with the ADSP-218xL series, two serial devices, a byte-wide EPROM, and optional external program and data overlay memories (mode-selectable). Programmable wait state generation allows the processor to connect easily to slow peripheral devices. ADSP-218xL series members also provide four external interrupts and two serial ports or six external interrupts and one serial port. Host Memory Mode allows access to the full external data bus, but limits addressing to a single address bit (A0). Through the use of external hardware, additional system peripherals can be added in this mode to generate and latch address signals.

Clock Signals

ADSP-218xL series members can be clocked by either a crystal or a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation, nor operated below the specified frequency during normal operation. The only exception is while the processor is in the power-down state. For additional information, refer to the *ADSP-218x DSP Hardware Reference*, for detailed information on this power-down feature.

If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL pin must be left unconnected.

ADSP-218xL series members use an input clock with a frequency equal to half the instruction rate; a 40 MHz input clock yields a 12.5 ns processor cycle (which is equivalent to 80 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because ADSP-218xL series members include an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 3. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used. To provide an adequate feedback path around the internal amplifier circuit, place a resistor in parallel with the circuit, as shown in Figure 3.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 Autobuffer Control Register.

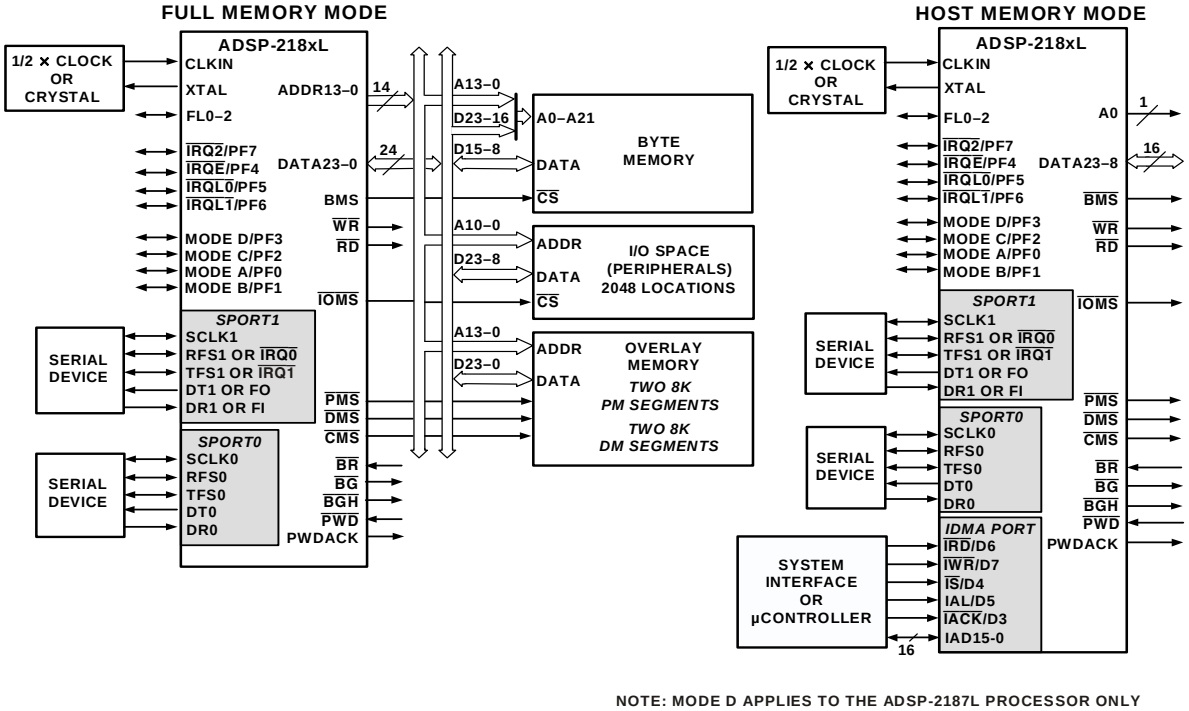


Figure 2. Basic System Interface

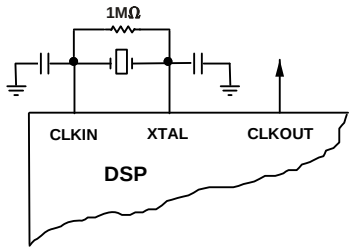


Figure 3. External Crystal Connections

RESET

The $\overline{\text{RESET}}$ signal initiates a master reset of the ADSP-218xL. The $\overline{\text{RESET}}$ signal must be asserted during the power-up sequence to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked, but does not include the crystal oscillator start-up time. During this power-up sequence, the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse width specification (t_{RSP}).

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if an RC circuit is used to generate the $\overline{\text{RESET}}$ signal, the use of an external Schmitt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts, and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting, the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

MEMORY ARCHITECTURE

The ADSP-218xL series provides a variety of memory and peripheral interface options. The key functional groups are Program Memory, Data Memory, Byte Memory, and I/O. Refer to Figure 4 through Figure 7 for PM and DM memory allocations in the ADSP-218xL series.

Program Memory

Program Memory (Full Memory Mode) is a 24-bit-wide space for storing both instruction opcodes and data. The member DSPs of this series have up to 32K words of Program Memory RAM on chip, and the capability of accessing up to two 8K external memory overlay spaces, using the external data bus.

Program Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0). External program execution is not available in Host Mode due to a restricted data bus that is only 16 bits wide.

Data Memory

Data Memory (Full Memory Mode) is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-218xL series has up to 32K words of Data Memory RAM on-chip. Part of this space is used by 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external data bus.

All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register.

Data Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0).

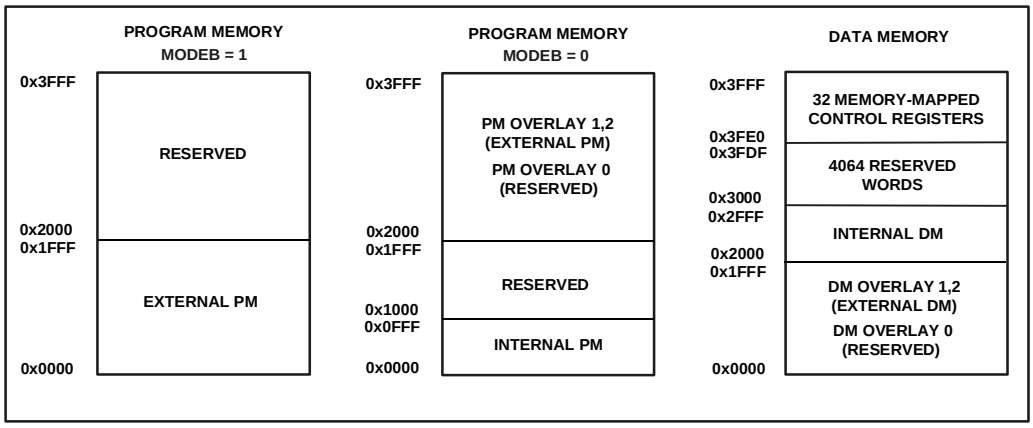


Figure 4. ADSP-2184 Memory Architecture

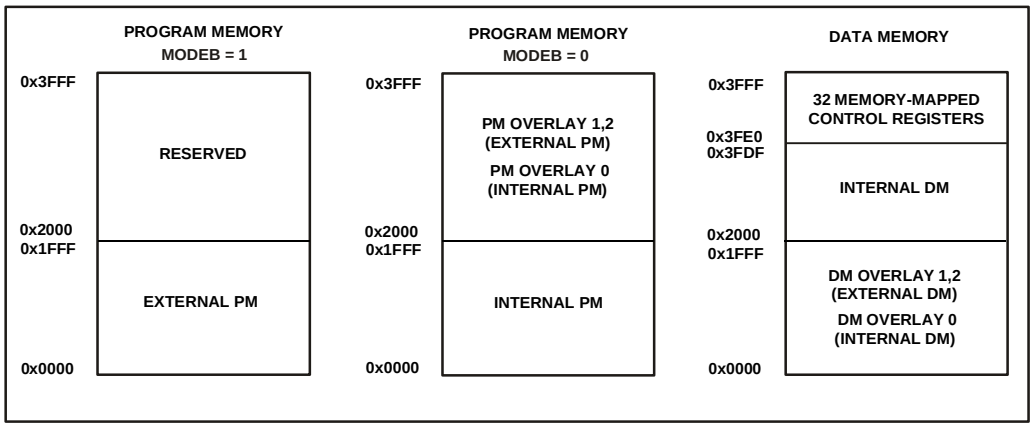


Figure 5. ADSP-2185 Memory Architecture

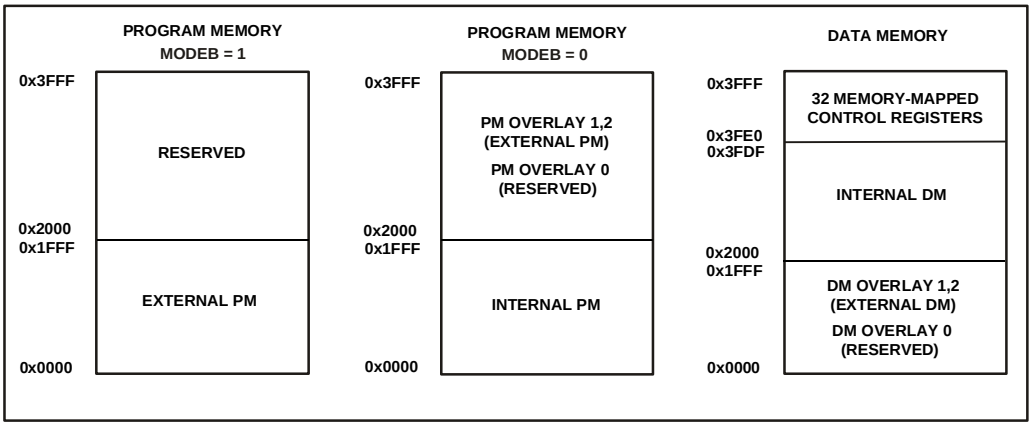


Figure 6. ADSP-2186 Memory Architecture

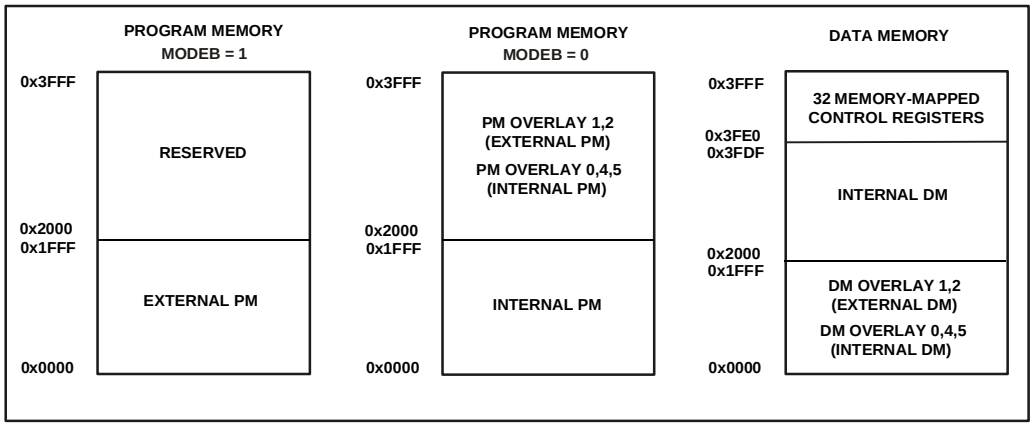


Figure 7. ADSP-2187 Memory Architecture

Table 4. PMOVLAY Bits

Processor	PMOVLAY	Memory	A13	A12–0
ADSP-2184L	No internal overlay region	Not Applicable	Not applicable	Not applicable
ADSP-2185L	0	Internal overlay	Not applicable	Not applicable
ADSP-2186L	No internal overlay region	Not applicable	Not applicable	Not applicable
ADSP-2187L	0, 4, 5	Internal overlay	Not applicable	Not applicable
All Processors	1	External overlay 1	0	13 LSBs of address between 0x2000 and 0x3FFF
All Processors	2	External overlay 2	1	13 LSBs of address between 0x2000 and 0x3FFF

Table 5. DMOVLAY Bits

Processor	DMOVLAY	Memory	A13	A12–0
ADSP-2184L	No internal overlay region	Not applicable	Not applicable	Not applicable
ADSP-2185L	0	Internal overlay	Not applicable	Not applicable
ADSP-2186L	No internal overlay region	Not applicable	Not applicable	Not applicable
ADSP-2187L	0, 4, 5	Internal overlay	Not applicable	Not applicable
All Processors	1	External overlay 1	0	13 LSBs of address between 0x0000 and 0x1FFF
All Processors	2	External overlay 2	1	13 LSBs of address between 0x0000 and 0x1FFF

I/O Space (Full Memory Mode)

ADSP-218xL series members support an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit wide data. The lower eleven bits of the external address bus are used; the upper three bits are undefined.

Two instructions were added to the core ADSP-2100 family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated 3-bit wait state registers, IOWAIT0–3 as shown in Figure 8, which specify up to seven wait states to be automatically generated for each of four regions. The wait states act on address ranges, as shown in Table 6.

Note: In Full Memory Mode, all 2048 locations of I/O space are directly addressable. In Host Memory Mode, only address pin A0 is available; therefore, additional logic is required externally to achieve complete addressability of the 2048 I/O space locations.

Table 6. Wait States

Address Range	Wait State Register
0x000–0x1FF	IOWAIT0
0x200–0x3FF	IOWAIT1
0x400–0x5FF	IOWAIT2
0x600–0x7FF	IOWAIT3

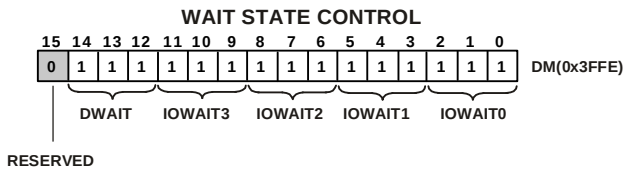


Figure 8. Wait State Control Register

Composite Memory Select

ADSP-218xL series members have a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality. Each bit in the CMSSEL register, when set, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory, and use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All enable bits default to 1 at reset, except the $\overline{\text{BMS}}$ bit.

Note: In Full Memory Mode, all locations of 4M-byte memory space are directly addressable. In Host Memory Mode, only address pin A0 is available, requiring additional external logic to provide address information for the byte.

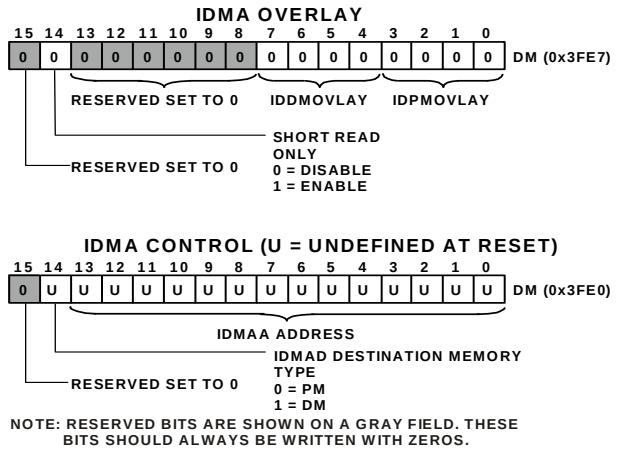


Figure 12. IDMA OVLAY/Control Registers

Bootstrap Loading (Booting)

ADSP-218xL series members have two mechanisms to allow automatic loading of the internal program memory after reset. The method for booting is controlled by the Mode A, Mode B, and Mode C configuration bits.

When the mode pins specify BDMA booting, the ADSP-218xL initiates a BDMA boot sequence when reset is released.

The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD, and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24-bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory. These 32 words are used to set up the BDMA to load in the remaining program code. The BCR bit is also set to 1, which causes program execution to be held off until all 32 words are loaded into on-chip program memory. Execution then begins at address 0.

The ADSP-2100 Family development software (Revision 5.02 and later) fully supports the BDMA booting feature and can generate byte memory space-compatible boot code.

The IDLE instruction can also be used to allow the processor to hold off execution while booting continues through the BDMA interface. For BDMA accesses while in Host Mode, the addresses to boot memory must be constructed externally to the ADSP-218xL. The only memory address bit provided by the processor is A0.

IDMA Port Booting

ADSP-218xL series members can also boot programs through its internal DMA port. If Mode C = 1, Mode B = 0, and Mode A = 1, the ADSP-218xL boots from the IDMA port. IDMA feature can load as much on-chip memory as desired. Program execution is held off until the host writes to on-chip program memory location 0.

BUS REQUEST AND BUS GRANT

ADSP-218xL series members can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the Bus Request ($\overline{BR}$) signal. If the ADSP-218xL is not performing an external memory access, it responds to the active $\overline{BR}$ input in the following processor cycle by:

- Three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- Asserting the bus grant ($\overline{BG}$) signal, and
- Halting program execution.

If Go Mode is enabled, the ADSP-218xL will not halt program execution until it encounters an instruction that requires an external memory access.

If an ADSP-218xL series member is performing an external memory access when the external device asserts the $\overline{BR}$ signal, it will not three-state the memory interfaces nor assert the $\overline{BG}$ signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, re-enables the output drivers, and continues program execution from the point at which it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The $\overline{BGH}$ pin is asserted when an ADSP-218xL series member requires the external bus for a memory or BDMA access, but is stopped. The other device can release the bus by deasserting bus request. Once the bus is released, the ADSP-218xL deasserts $\overline{BG}$ and $\overline{BGH}$ and executes the external memory access.

FLAG I/O PINS

ADSP-218xL series members have eight general-purpose programmable input/output flag pins. They are controlled by two memory-mapped registers. The PFTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the ADSP-218xL's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

In addition to the programmable flags, ADSP-218xL series members have five fixed-mode flags, FI, FO, FL0, FL1, and FL2. FL0 to FL2 are dedicated output flags. FI and FO are available as an alternate configuration of SPORT1.

Note: Pins PF0, PF1, PF2, and PF3 are also used for device configuration during reset.

INSTRUCTION SET DESCRIPTION

The ADSP-218xL series assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize on-chip memory and conform to the ADSP-218xL's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction, with up to two fetches or one write to processor memory space, during a single instruction cycle.

DEVELOPMENT SYSTEM

Analog Devices' wide range of software and hardware development tools supports the ADSP-218xL series. The DSP tools include an integrated development environment, an evaluation kit, and a serial port emulator.

VisualDSP++®† is an integrated development environment, allowing for fast and easy development, debugging, and deployment. The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy-to-use assembler that is based on an algebraic syntax; an archiver (librarian/library builder); a linker; a PROM-splitter utility; a cycle-accurate, instruction-level simulator; a C compiler; and a C run-time library that includes DSP and mathematical functions.

Debugging both C and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C and assembly code (interleaved source and object information)
- Insert break points
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- Fill and dump memory
- Source level debugging

The VisualDSP++ IDE lets programmers define and manage DSP software development. The dialog boxes and property pages let programmers configure and manage all of the ADSP-218xL development tools, including the syntax highlighting in the VisualDSP++ editor. This capability controls how the development tools process inputs and generate outputs.

The ADSP-2189M EZ-KIT Lite®‡ provides developers with a cost-effective method for initial evaluation of the powerful ADSP-218xL DSP family architecture. The ADSP-2189M EZ-KIT Lite includes a standalone ADSP-2189M DSP board supported by an evaluation suite of VisualDSP++. With this EZ-KIT Lite, users can learn about DSP hardware and software development and evaluate potential applications of the ADSP-218xL series. The ADSP-2189M EZ-KIT Lite provides an evaluation suite of the VisualDSP++ development environment with the C compiler, assembler, and linker. The size of the DSP executable that can be built using the EZ-KIT Lite tools is limited to 8K words.

The EZ-KIT Lite includes the following features:

- 75 MHz ADSP-2189M
- Full 16-Bit Stereo Audio I/O with AD73322 Codec
- RS-232 Interface
- EZ-ICE® Connector for Emulator Control
- DSP Demonstration Programs
- Evaluation Suite of VisualDSP++

The ADSP-218x EZ-ICE§ Emulator provides an easier and more cost-effective method for engineers to develop and optimize DSP systems, shortening product development cycles for faster time-to-market. ADSP-218xL series members integrate on-chip emulation support with a 14-pin ICE-Port™ interface. This interface provides a simpler target board connection that requires fewer mechanical clearance considerations than other ADSP-2100 Family EZ-ICEs. ADSP-218xL series members need not be removed from the target system when using the EZ-ICE, nor are any adapters needed. Due to the small footprint of the EZ-ICE connector, emulation can be supported in final board designs.The EZ-ICE performs a full range of functions, including:

- In-target operation
- Up to 20 breakpoints
- Single-step or full-speed operation
- Registers and memory values can be examined and altered
- PC upload and download functions
- Instruction-level emulation of program booting and execution

† VisualDSP++ is a registered trademark of Analog Devices, Inc.

‡ EZ-KIT Lite is a registered trademark of Analog Devices, Inc.

§ EZ-ICE is a registered trademark of Analog Devices, Inc.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed below may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Rating
Supply Voltage (V_{DD})	–0.3 V to +4.6 V
Input Voltage[1]	–0.5 V to V_{DD} + 0.5 V
Output Voltage Swing[2]	–0.5 V to V_{DD} +0.5 V
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C

[1] Applies to bidirectional pins (D23–0, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A13–1, PF7–0) and input only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).
[2] Applies to output pins ($\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$).

PACKAGE INFORMATION

The information presented in Figure 15 provides details about the package branding for the ADSP-218xL processors. For a complete listing of product availability, see Ordering Guide on Page 47.

Figure 15. Typical Package Brand

Table 13. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHs Compliant Option (optional)
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

General Notes

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, parameters cannot be added up meaningfully to derive longer times.

Timing Notes

Switching characteristics specify how the processor changes its signals. Designers have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell what the processor will do in a given circumstance. Switching characteristics can also be used to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Frequency Dependency For Timing Specifications

t_{CK} is defined as 0.5 t_{CKI}. The ADSP-218xL uses an input clock with a frequency equal to half the instruction rate. For example, a 26 MHz input clock (which is equivalent to 38 ns) yields a 19 ns processor cycle (equivalent to 52 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain the specification value.

Example: t_{CKH} = 0.5 t_{CK} – 7 ns = 0.5 (19) – 7 ns = 2.5 ns

Clock Signals and Reset

Table 14. Clock Signals and Reset

Parameter		ADSP-2184L, ADSP-2186L Min	ADSP-2184L, ADSP-2186L Max	ADSP-2185L, ADSP-2187L Min	ADSP-2185L, ADSP-2187L Max	Unit
Timing Requirements:						
t_{CKI}	CLKIN Period	50	150	38	100	ns
t_{CKIL}	CLKIN Width Low	20		15		ns
t_{CKIH}	CLKIN Width High	20		15		ns
Switching Characteristics:						
t_{CKL}	CLKOUT Width Low	$0.5t_{CK} - 7$		$0.5t_{CK} - 7$		ns
t_{CKH}	CLKOUT Width High	$0.5t_{CK} - 7$		$0.5t_{CK} - 7$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	0	20	ns
Control Signals Timing Requirements:						
t_{RSP}	$\overline{\text{RESET}}$ Width Low[1]	$5t_{CK}$		$5t_{CK}$		ns
t_{MS}	Mode Setup Before $\overline{\text{RESET}}$ High	2		2		ns
t_{MH}	Mode Hold After $\overline{\text{RESET}}$ High	5		5		ns

[1] Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles, assuming stable CLKIN (not including crystal oscillator start-up time).

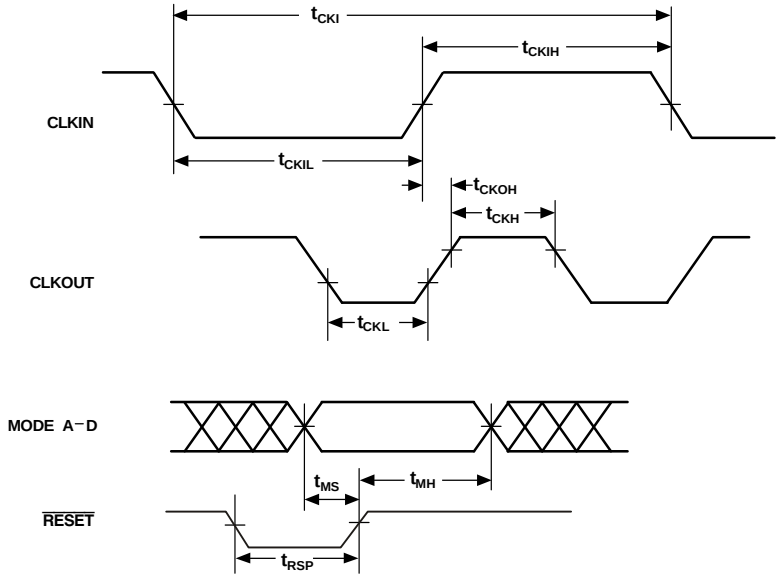


Figure 16. Clock Signals and Reset

Memory Read

Table 17. Memory Read

Parameter		Min	Max	Unit
Timing Requirements:				
t_{RDD}	$\overline{RD}$ Low to Data Valid[1]		$0.5t_{CK} - 9 + w$	ns
t_{AA}	A13–0, $\overline{xMS}$ to Data Valid[2]		$0.75t_{CK} - 12.5 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High[3]	1		ns
Switching Characteristics:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 5 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 7$	ns
t_{ASR}	A13–0, $\overline{xMS}$ Setup Before $\overline{RD}$ Low	$0.25t_{CK} - 6$		ns
t_{RDA}	A13–0, $\overline{xMS}$ Hold After $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

[1] w = wait states × t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.
[3] For the ADSP-2187L, this specification is 0 ns min.

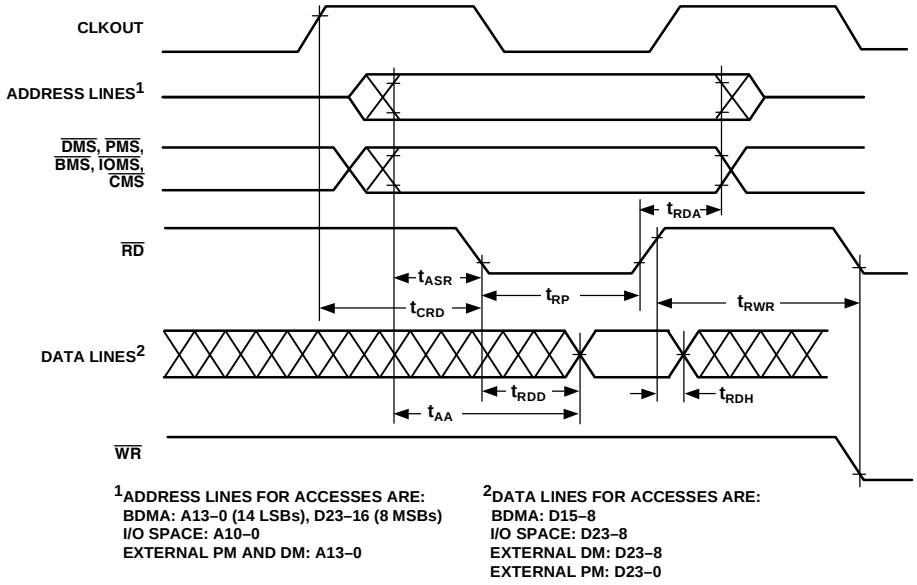


Figure 19. Memory Read

Serial Ports

Table 19. Serial Ports

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SCK}	SCLK Period[1]	50		ns
t_{SCS}	DR/TFS/RFS Setup Before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold After SCLK Low[2]	8		ns
t_{SCP}	SCLKIN Width[3]	20		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to SCLKOUT	$0.25t_{CK}$	$0.25t_{CK} + 10$	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		15	ns
t_{RH}	TFS/RFS_{OUT} Hold After SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		15	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		14	ns
t_{SCDD}	SCLK High to DT Disable		15	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		15	ns

[1] For the ADSP-2187L, this specification is 38 ns min.
[2] For the ADSP-2187L, this specification is 7 ns min.
[3] For the ADSP-2185L, and the ADSP-2187L, this specification is 15 ns min.

IDMA Write, Short Write Cycle

Table 21. IDMA Write, Short Write Cycle

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low Before Start of Write[1]	0		ns
t_{IWP}	Duration of Write[1, 2]	15		ns
t_{IDSU}	IAD15–0 Data Setup Before End of Write[2, 3, 4]	5		ns
t_{IDH}	IAD15–0 Data Hold After End of Write[2, 3, 4]	2		ns
Switching Characteristic:				
t_{IKHW}	Start of Write to $\overline{IACK}$ High[5]		17	ns

[1] Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2] End of Write = $\overline{IS}$ High or $\overline{IWR}$ High.
[3] If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[4] If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.
[5] For the ADSP-2185L, and the ADSP-2187L, this specification is 4 ns min., and 15 ns max.

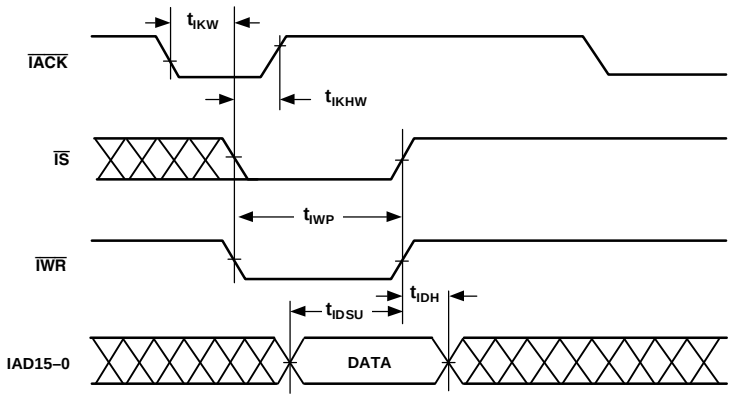


Figure 23. IDMA Write, Short Write Cycle

IDMA Write, Long Write Cycle

Table 22. IDMA Write, Long Write Cycle

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low Before Start of Write[1]	0		ns
t_{IKSU}	IAD15–0 Data Setup Before End of Write[2, 3, 4]	$0.5t_{CK} + 10$		ns
t_{IKH}	IAD15–0 Data Hold After End of Write[2, 3, 4]	2		ns
Switching Characteristics:				
t_{IKLW}	Start of Write to $\overline{IACK}$ Low[4]	$1.5t_{CK}$		ns
t_{IKHW}	Start of Write to $\overline{IACK}$ High[5]		17	ns

[1] Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2] If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[3] If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.
[4] This is the earliest time for $\overline{IACK}$ Low from Start of Write. For IDMA Write cycle relationships, please refer to the *ADSP-2100 Family User's Manual*.
[5] For the ADSP-2185L, and the ADSP-2187L, this specification is 4 ns min., and 15 ns max.

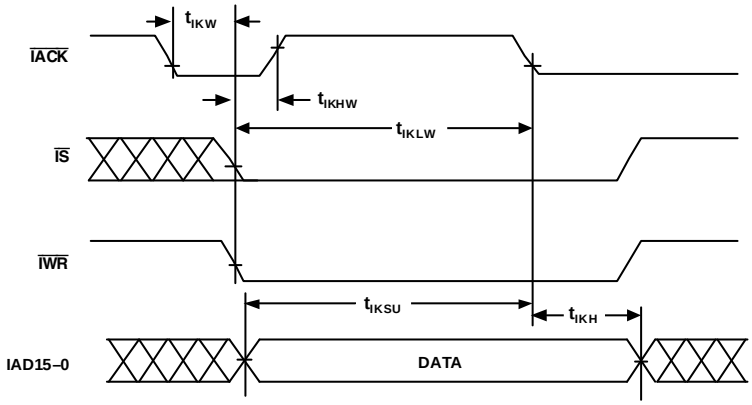
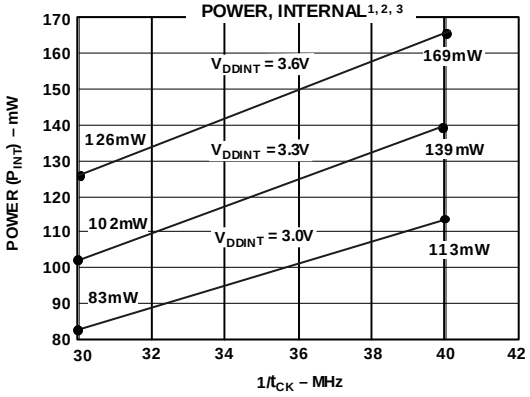
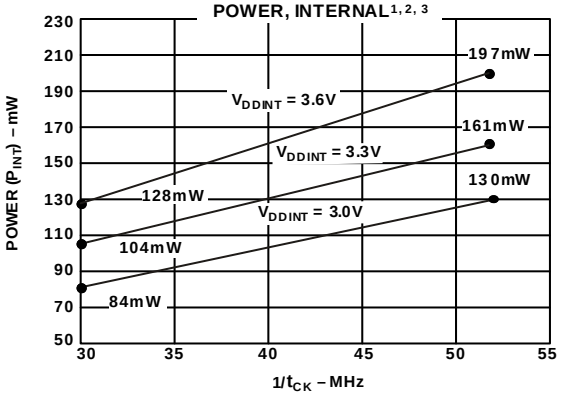
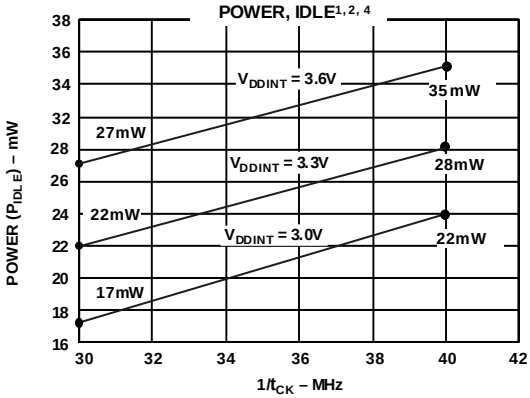
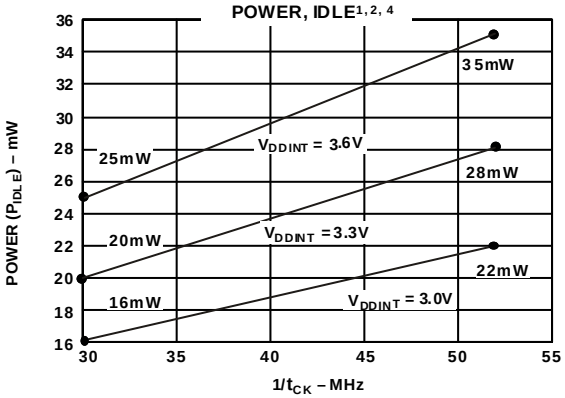


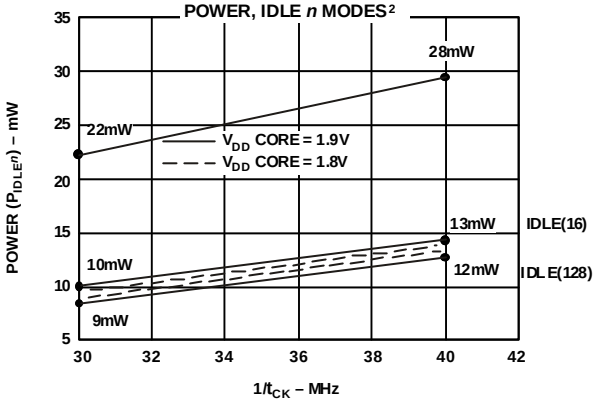
Figure 24. IDMA Write, Long Write Cycle

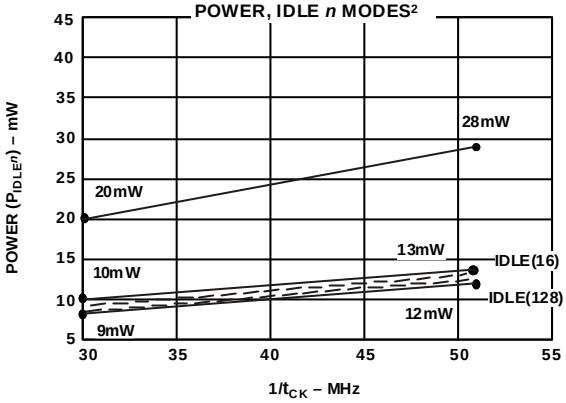










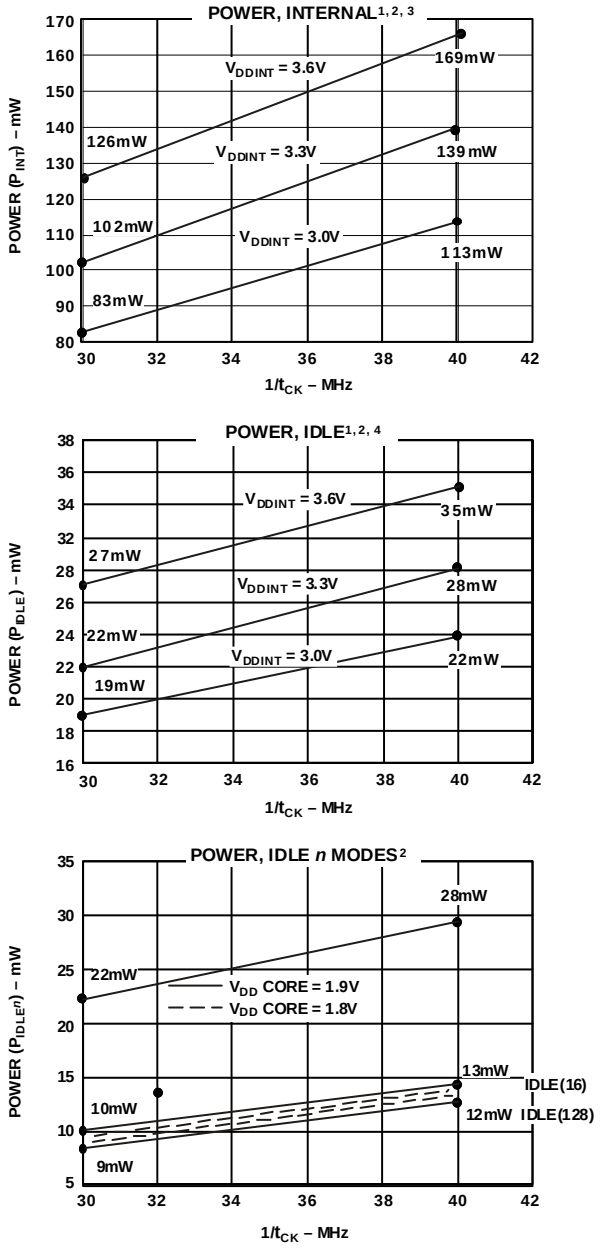


NOTES
VALID FOR ALL TEMPERATURE GRADES.
1. POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
2. TYPICAL POWER DISSIPATION AT 3.3V V_{DD} AND 25°C, EXCEPT WHERE SPECIFIED.
3. IDD MEASUREMENT TAKEN WITH ALL INSTRUCTIONS EXECUTING FROM INTERNAL MEMORY. 50% Of the INSTRUCTIONS ARE MULTIFUNCTION (TYPES 1, 4, 5, 12, 13, 14), 30% ARE TYPE 2 AND TYPE 6, AND 20% ARE IDLE INSTRUCTIONS.
4. IDLE REFERS TO STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.

Figure 28. Power vs. Frequency (ADSP-2184L)

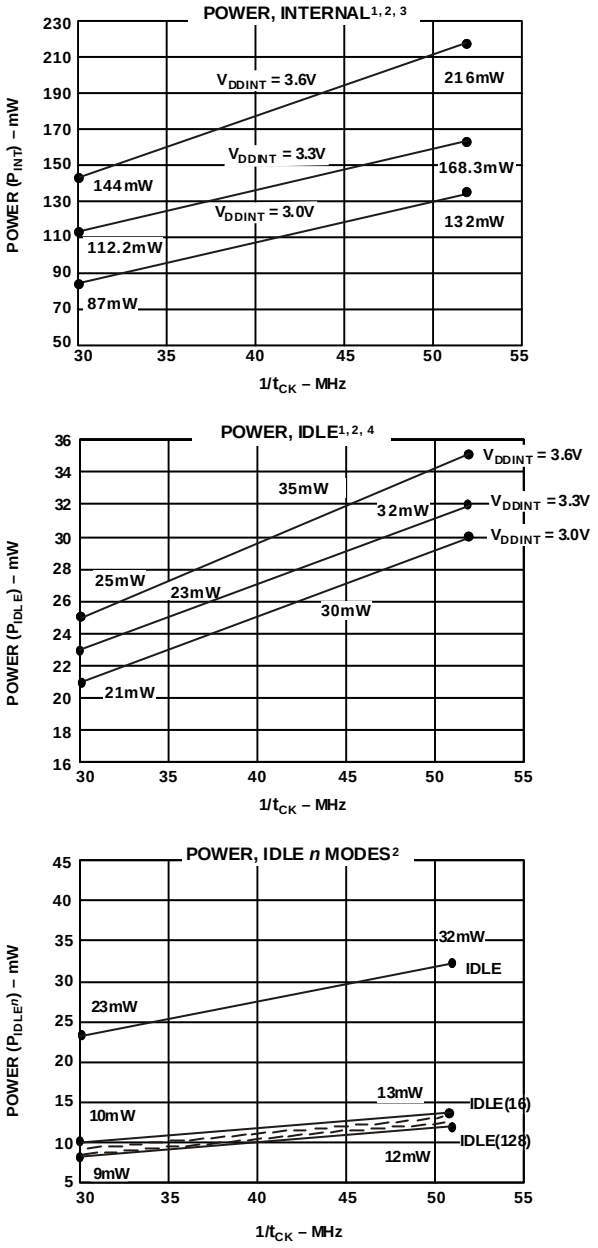
NOTES
VALID FOR ALL TEMPERATURE GRADES.
1. POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
2. TYPICAL POWER DISSIPATION AT 3.3V V_{DD} AND 25°C, EXCEPT WHERE SPECIFIED.
3. IDD MEASUREMENT TAKEN WITH ALL INSTRUCTIONS EXECUTING FROM INTERNAL MEMORY. 50% Of the INSTRUCTIONS ARE MULTIFUNCTION (TYPES 1, 4, 5, 12, 13, 14), 30% ARE TYPE 2 AND TYPE 6, AND 20% ARE IDLE INSTRUCTIONS.
4. IDLE REFERS TO STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.

Figure 29. Power vs. Frequency (ADSP-2185L)



NOTES
VALID FOR ALL TEMPERATURE GRADES.
1. POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
2. TYPICAL POWER DISSIPATION AT 3.3V V_{DD} AND 25°C, EXCEPT WHERE SPECIFIED.
3. IDD MEASUREMENT TAKEN WITH ALL INSTRUCTIONS EXECUTING FROM INTERNAL MEMORY. 50% Of the INSTRUCTIONS ARE MULTIFUNCTION (TYPES 1, 4, 5, 12, 13, 14), 30% ARE TYPE 2 AND TYPE 6, AND 20% ARE IDLE INSTRUCTIONS.
4. IDLE REFERS TO STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.

Figure 30. Power vs. Frequency (ADSP-2186L)



NOTES
VALID FOR ALL TEMPERATURE GRADES.
1. POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
2. TYPICAL POWER DISSIPATION AT 3.3V V_{DD} AND 25°C, EXCEPT WHERE SPECIFIED.
3. IDD MEASUREMENT TAKEN WITH ALL INSTRUCTIONS EXECUTING FROM INTERNAL MEMORY. 50% Of the INSTRUCTIONS ARE MULTIFUNCTION (TYPES 1, 4, 5, 12, 13, 14), 30% ARE TYPE 2 AND TYPE 6, AND 20% ARE IDLE INSTRUCTIONS.
4. IDLE REFERS TO STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.

Figure 31. Power vs. Frequency (ADSP-2187L)

LQFP PACKAGE PINOUT

The LQFP package pinout is shown in Table 29. Pin names in bold text in the table replace the plain-text-named functions when Mode C equals 1. A plus sign (+) separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$. The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default, upon reset.

Table 29. LQFP Pin Assignments

Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name
1	A4/**IAD3**	26	$\overline{\text{IRQE}}$ + PF4	51	$\overline{\text{EBR}}$	76	D16
2	A5/**IAD4**	27	$\overline{\text{IRQL0}}$ + PF5	52	$\overline{\text{BR}}$	77	D17
3	GND	28	GND	53	$\overline{\text{EBG}}$	78	D18
4	A6/**IAD5**	29	$\overline{\text{IRQL1}}$ + PF6	54	$\overline{\text{BG}}$	79	D19
5	A7/**IAD6**	30	$\overline{\text{IRQ2}}$ + PF7	55	D0/**IAD13**	80	GND
6	A8/**IAD7**	31	DT0	56	D1/**IAD14**	81	D20
7	A9/**IAD8**	32	TFS0	57	D2/**IAD15**	82	D21
8	A10/**IAD9**	33	RFS0	58	D3/$\overline{\textbf{IACK}}$	83	D22
9	A11/**IAD10**	34	DR0	59	V_{DDINT}	84	D23
10	A12/**IAD11**	35	SCLK0	60	GND	85	FL2
11	A13/**IAD12**	36	V_{DDEXT}	61	D4/$\overline{\textbf{IS}}$	86	FL1
12	GND	37	DT1/FO	62	D5/**IAL**	87	FL0
13	CLKIN	38	TFS1/$\overline{\text{IRQ1}}$	63	D6/$\overline{\textbf{IRD}}$	88	PF3 [Mode D[1]]
14	XTAL	39	RFS1/$\overline{\text{IRQ0}}$	64	D7/$\overline{\textbf{IWR}}$	89	PF2 [Mode C]
15	V_{DDEXT}	40	DR1/FI	65	D8	90	V_{DDEXT}
16	CLKOUT	41	GND	66	GND	91	$\overline{\text{PWD}}$
17	GND	42	SCLK1	67	V_{DDEXT}	92	GND
18	V_{DDINT}	43	$\overline{\text{ERESET}}$	68	D9	93	PF1 [Mode B]
19	$\overline{\text{WR}}$	44	$\overline{\text{RESET}}$	69	D10	94	PF0 [Mode A]
20	$\overline{\text{RD}}$	45	$\overline{\text{EMS}}$	70	D11	95	$\overline{\text{BGH}}$
21	$\overline{\text{BMS}}$	46	EE	71	GND	96	PWDACK
22	$\overline{\text{DMS}}$	47	ECLK	72	D12	97	A0
23	$\overline{\text{PMS}}$	48	ELOUT	73	D13	98	A1/**IAD0**
24	$\overline{\text{IOMS}}$	49	ELIN	74	D14	99	A2/**IAD1**
25	$\overline{\text{CMS}}$	50	$\overline{\text{EINT}}$	75	D15	100	A3/**IAD2**

[1] Mode D function available on ADSP-2187L only.

BGA PACKAGE PINOUT

The BGA package pinout is shown in Table 30. Pin names in bold text in the table replace the plain text named functions when Mode C equals 1. A plus sign (+) separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$. The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default upon reset.

Table 30. BGA Pin Assignments

Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name
A01	A2/**IAD1**	D01	NC	G01	XTAL	K01	NC
A02	A1/**IAD0**	D02	$\overline{\text{WR}}$	G02	NC	K02	NC
A03	GND	D03	NC	G03	GND	K03	NC
A04	A0	D04	$\overline{\text{BGH}}$	G04	A10/**IAD9**	K04	$\overline{\text{BMS}}$
A05	NC	D05	A9/**IAD8**	G05	NC	K05	$\overline{\text{DMS}}$
A06	GND	D06	PF1 [MODE B]	G06	NC	K06	RFS0
A07	NC	D07	PF2 [MODE C]	G07	NC	K07	TFS1/$\overline{\text{IRQ1}}$
A08	NC	D08	NC	G08	D6/**$\overline{\text{IRD}}$**	K08	SCLK1
A09	NC	D09	D13	G09	D5/**IAL**	K09	$\overline{\text{ERESET}}$
A10	D22	D10	D12	G10	NC	K10	$\overline{\text{EBR}}$
A11	GND	D11	NC	G11	NC	K11	$\overline{\text{BR}}$
A12	GND	D12	GND	G12	D4/**$\overline{\text{IS}}$**	K12	$\overline{\text{EBG}}$
B01	A4/**IAD3**	E01	V_{DDEXT}	H01	CLKIN	L01	$\overline{\text{IRQE}}$ + PF4
B02	A3/**IAD2**	E02	V_{DDEXT}	H02	GND	L02	NC
B03	GND	E03	A8/**IAD7**	H03	GND	L03	$\overline{\text{IRQL1}}$ + PF6
B04	NC	E04	FL0	H04	GND	L04	$\overline{\text{IOMS}}$
B05	NC	E05	PF0 [MODE A]	H05	V_{DDINT}	L05	GND
B06	GND	E06	FL2	H06	DT0	L06	$\overline{\text{PMS}}$
B07	V_{DDEXT}	E07	PF3 [MODE D[1]]	H07	TFS0	L07	DR0
B08	D23	E08	GND	H08	D2/**IAD15**	L08	GND
B09	D20	E09	GND	H09	D3/**$\overline{\text{IACK}}$**	L09	$\overline{\text{RESET}}$
B10	D18	E10	V_{DDEXT}	H10	GND	L10	ELIN
B11	D17	E11	GND	H11	NC	L11	ELOUT
B12	D16	E12	D10	H12	GND	L12	$\overline{\text{EINT}}$
C01	PWDACK	F01	A13/**IAD12**	J01	CLKOUT	M01	$\overline{\text{IRQL0}}$ + PF5
C02	A6/**IAD5**	F02	NC	J02	V_{DDINT}	M02	$\overline{\text{IRQL2}}$ + PF7
C03	$\overline{\text{RD}}$	F03	A12/**IAD11**	J03	NC	M03	NC
C04	A5/**IAD4**	F04	A11/**IAD10**	J04	V_{DDEXT}	M04	$\overline{\text{CMS}}$
C05	A7/**IAD6**	F05	FL1	J05	V_{DDEXT}	M05	GND
C06	$\overline{\text{PWD}}$	F06	NC	J06	SCLK0	M06	DT1/FO
C07	V_{DDEXT}	F07	NC	J07	D0/**IAD13**	M07	DR1/FI
C08	D21	F08	D7/**$\overline{\text{IWR}}$**	J08	RFS1/$\overline{\text{IRQ0}}$	M08	GND
C09	D19	F09	D11	J09	$\overline{\text{BG}}$	M09	NC
C10	D15	F10	D8	J10	D1/**IAD14**	M10	$\overline{\text{EMS}}$
C11	NC	F11	NC	J11	V_{DDINT}	M11	EE
C12	D14	F12	D9	J12	V_{DDINT}	M12	ECLK

[1] Mode D function available on ADSP-2187L only.