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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	52MHz
Non-Volatile Memory	External
On-Chip RAM	160kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2187lbstz-210

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REVISION HISTORY

1/08—Rev. C

This revision of the ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L processor data sheet combines the ADSP-2184L, ADSP-2185L, ADSP-2186L, and ADSP-2187L. This version also contains new RoHS compliant packages.

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting ADSP-218xL series members to fetch two operands in a single cycle, one from program memory and one from data memory. ADSP-218xL series members can fetch an operand from program memory and the next instruction in the same cycle.

In lieu of the address and data bus for external memory connection, ADSP-218xL series members can be configured for 16-bit Internal DMA port (IDMA port) connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSP's on-chip program and data RAM.

An interface to low cost, byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$, and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-218xL to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

ADSP-218xL series members can respond to eleven interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORT), the BDMA port, and the power-down circuitry. There is also a master $\overline{RESET}$ signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation. Each serial port can generate an internal programmable serial clock or accept an external serial clock.

ADSP-218xL series members provide up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, eight flags are programmable as inputs or outputs, and three flags are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) decrements every n processor cycle, where n is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

ADSP-218xL series members incorporate two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Following is a brief list of the capabilities of the ADSP-218xL SPORTs. For additional information on Serial Ports, refer to the *ADSP-218x DSP Hardware Reference*.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulse widths and timings.
- SPORTs support serial data word lengths from 3 bits to 16 bits and provide optional A-law and μ-law companding, according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24-word or 32-word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts ($\overline{IRQ0}$ and $\overline{IRQ1}$) and the FI and FO signals. The internally generated serial clock may still be used in this configuration.

MODES OF OPERATION

The ADSP-218xL series modes of operation appear in Table 2. Only the ADSP-2187L provides Mode D operation

Setting Memory Mode

Memory Mode selection for the ADSP-218xL series is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP's PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are active and passive.

Passive Configuration

Passive Configuration involves the use of a pull-up or pull-down resistor connected to the Mode C pin. To minimize power consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down resistance, on the order of 10 kΩ, can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor's output driver. For minimum power consumption

Table 2. Modes of Operation

Mode D[1]	Mode C	Mode B	Mode A	Booting Method
X	0	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Full Memory Mode.[2]
X	0	1	0	No automatic boot operations occur. Program execution starts at external memory location 0. Chip is configured in Full Memory Mode. BDMA can still be used, but the processor does not automatically use or wait for these operations.
0	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode. $\overline{\text{IACK}}$ has active pull-down. (Requires additional hardware.)
0	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until the host writes to internal program memory location 0. Chip is configured in Host Mode. $\overline{\text{IACK}}$ has active pull-down.[2]
1	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode; $\overline{\text{IACK}}$ requires external pull-down. (Requires additional hardware.)
1	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until the host writes to internal program memory location 0. Chip is configured in Host Mode. $\overline{\text{IACK}}$ requires external pull-down.[2]

[1] Mode D applies to the ADSP-2187L processor only.
[2] Considered as standard operating settings. Using these configurations allows for easier design and better memory management.

during power-down, reconfigure PF2 to be an input, as the pull-up or pull-down resistance will hold the pin in a known state, and will not switch.

Active Configuration

Active Configuration involves the use of a three-statable external driver connected to the Mode C pin. A driver's output enable should be connected to the DSP's $\overline{\text{RESET}}$ signal such that it only drives the PF2 pin when $\overline{\text{RESET}}$ is active (low). When $\overline{\text{RESET}}$ is deasserted, the driver should be three-state, thus allowing full use of the PF2 pin as either an input or output. To minimize power consumption during power-down, configure the programmable flag as an output when connected to a three-stated buffer. This ensures that the pin will be held at a constant level, and will not oscillate should the three-state driver's level hover around the logic switching point.

IDMA ACK Configuration (ADSP-2187L Only)

Mode D = 0 and in Host Mode: $\overline{\text{IACK}}$ is an active, driven signal and cannot be "wire-OR'ed." Mode D = 1 and in Host Mode: $\overline{\text{IACK}}$ is an open drain and requires an external pull-down, but multiple $\overline{\text{IACK}}$ pins can be "wire-OR'ed" together.

INTERRUPTS

The interrupt controller allows the processor to respond to the eleven possible interrupts and reset with minimum overhead. ADSP-218xL series members provide four dedicated external interrupt input pins: $\overline{\text{IRQ2}}$, $\overline{\text{IRQL0}}$, $\overline{\text{IRQL1}}$, and $\overline{\text{IRQE}}$ (shared with the PF7–4 pins). In addition, SPORT1 may be reconfigured for $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, FI, and FO, for a total of six external interrupts. The ADSP-218xL also supports internal interrupts from the timer, the byte DMA port, the two serial ports, software, and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power-down and reset). The $\overline{\text{IRQ2}}$, $\overline{\text{IRQ0}}$, and $\overline{\text{IRQ1}}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ are level-sensitive and $\overline{\text{IRQE}}$ is edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table 3.

Table 3. Interrupt Priority and Interrupt Vector Addresses

Source Of Interrupt	Interrupt Vector Address (Hex)
$\overline{\text{RESET}}$ (or Power-Up with PUCR = 1)	0x0000 (highest priority)
Power-Down (Nonmaskable)	0x002C
$\overline{\text{IRQ2}}$	0x0004
$\overline{\text{IRQL1}}$	0x0008
$\overline{\text{IRQL0}}$	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
$\overline{\text{IRQE}}$	0x0018
BDMA Interrupt	0x001C
SPORT1 Transmit or $\overline{\text{IRQ1}}$	0x0020
SPORT1 Receive or $\overline{\text{IRQ0}}$	0x0024
Timer	0x0028 (lowest priority)

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register.

Individual interrupt requests are logically AND'ed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

ADSP-218xL series members mask all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ external interrupts to be either edge- or level-sensitive. The $\overline{\text{IRQE}}$ pin is an external edge-sensitive interrupt and can be forced and cleared. The $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ pins are external level sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are 12 levels deep to allow interrupt, loop, and subroutine nesting. The following instructions allow global enable or disable servicing of the interrupts (including power-down), regardless of the state of IMASK:

```
ENA INTS;
DIS INTS;
```

Disabling the interrupts does not affect serial port autobuffering or DMA. When the processor is reset, interrupt servicing is enabled.

LOW POWER OPERATION

ADSP-218xL series members have three low-power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

ADSP-218xL series members have a low-power feature that lets the processor enter a very low-power dormant state through hardware or software control. Following is a brief list of power-down features. Refer to the *ADSP-218x DSP Hardware Reference*, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 400 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 400 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits approximately 4096 CLKIN cycles for the crystal oscillator to start or stabilize), and letting the oscillator run to allow 400 CLKIN cycle start-up.
- Power-down is initiated by either the power-down pin ($\overline{\text{PWD}}$) or the software power-down force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate power-down.
- Power-down acknowledge pin (PWDACK) indicates when the processor has entered power-down.

Idle

When the ADSP-218xL is in the Idle Mode, the processor waits indefinitely in a low-power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle Mode IDMA, BDMA, and autobuffer cycle steals still occur.

Slow Idle

The IDLE instruction is enhanced on ADSP-218xL series members to let the processor's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction.

The format of the instruction is:

```
IDLE (n);
```

where n = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT, and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the IDLE (n) instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by n, the clock divisor. When an enabled interrupt is received, ADSP-218xL series members remain in the idle state for up to a maximum of n processor cycles (n = 16, 32, 64, or 128) before resuming normal operation.

When the IDLE (n) instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a

Table 4. PMOVLAY Bits

Processor	PMOVLAY	Memory	A13	A12–0
ADSP-2184L	No internal overlay region	Not Applicable	Not applicable	Not applicable
ADSP-2185L	0	Internal overlay	Not applicable	Not applicable
ADSP-2186L	No internal overlay region	Not applicable	Not applicable	Not applicable
ADSP-2187L	0, 4, 5	Internal overlay	Not applicable	Not applicable
All Processors	1	External overlay 1	0	13 LSBs of address between 0x2000 and 0x3FFF
All Processors	2	External overlay 2	1	13 LSBs of address between 0x2000 and 0x3FFF

Table 5. DMOVLAY Bits

Processor	DMOVLAY	Memory	A13	A12–0
ADSP-2184L	No internal overlay region	Not applicable	Not applicable	Not applicable
ADSP-2185L	0	Internal overlay	Not applicable	Not applicable
ADSP-2186L	No internal overlay region	Not applicable	Not applicable	Not applicable
ADSP-2187L	0, 4, 5	Internal overlay	Not applicable	Not applicable
All Processors	1	External overlay 1	0	13 LSBs of address between 0x0000 and 0x1FFF
All Processors	2	External overlay 2	1	13 LSBs of address between 0x0000 and 0x1FFF

I/O Space (Full Memory Mode)

ADSP-218xL series members support an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit wide data. The lower eleven bits of the external address bus are used; the upper three bits are undefined.

Two instructions were added to the core ADSP-2100 family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated 3-bit wait state registers, IOWAIT0–3 as shown in Figure 8, which specify up to seven wait states to be automatically generated for each of four regions. The wait states act on address ranges, as shown in Table 6.

Note: In Full Memory Mode, all 2048 locations of I/O space are directly addressable. In Host Memory Mode, only address pin A0 is available; therefore, additional logic is required externally to achieve complete addressability of the 2048 I/O space locations.

Table 6. Wait States

Address Range	Wait State Register
0x000–0x1FF	IOWAIT0
0x200–0x3FF	IOWAIT1
0x400–0x5FF	IOWAIT2
0x600–0x7FF	IOWAIT3

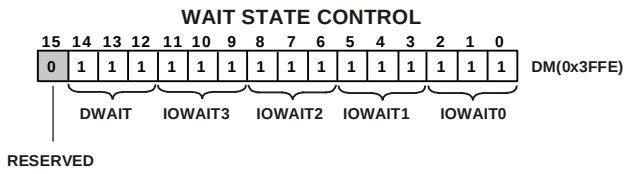


Figure 8. Wait State Control Register

Composite Memory Select

ADSP-218xL series members have a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality. Each bit in the CMSSEL register, when set, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory, and use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All enable bits default to 1 at reset, except the $\overline{\text{BMS}}$ bit.

See Figure 9 and Figure 10 for illustration of the programmable flag and composite control register and the system control register.

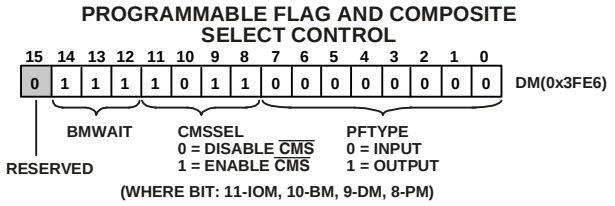


Figure 9. Programmable Flag and Composite Control Register

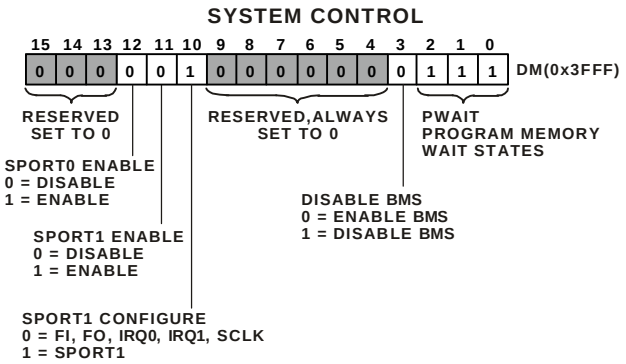


Figure 10. System Control Register

Byte Memory Select

The ADSP-218xL's $\overline{\text{BMS}}$ disable feature combined with the $\overline{\text{CMS}}$ pin allows use of multiple memories in the byte memory space. For example, an EPROM could be attached to the $\overline{\text{BMS}}$ select, and a flash memory could be connected to $\overline{\text{CMS}}$. Because at reset $\overline{\text{BMS}}$ is enabled, the EPROM would be used for booting. After booting, software could disable $\overline{\text{BMS}}$ and set the $\overline{\text{CMS}}$ signal to respond to $\overline{\text{BMS}}$, enabling the flash memory.

Byte Memory

The byte memory space is a bidirectional, 8-bit-wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The byte memory space consists of 256 pages, each of which is 16K × 8 bits.

The byte memory space on the ADSP-218xL series supports read and write operations as well as four different data formats. The byte memory uses data bits 15–8 for data. The byte memory uses data bits 23–16 and address bits 13–0 to create a 22-bit address. This allows up to a 4 megabit × 8 (32 megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BMWAIT register.

Byte Memory DMA (BDMA, Full Memory Mode)

The byte memory DMA controller (Figure 11) allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit is able to access the byte memory space while the processor is operating normally and steals only one DSP cycle per 8-, 16-, or 24-bit word transferred.

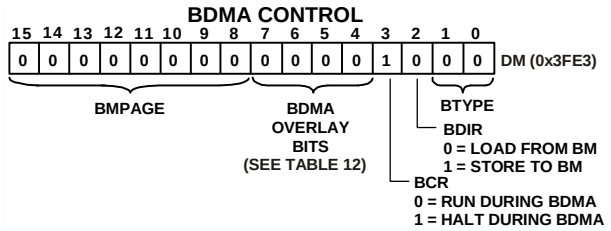


Figure 11. BDMA Control Register

The BDMA circuit supports four different data formats that are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table 7 shows the data formats supported by the BDMA circuit.

Table 7. Data Formats

BTYPE	Internal Memory Space	Word Size	Alignment
00	Program memory	24	Full word
01	Data memory	16	Full word
10	Data memory	8	MSBs
11	Data memory	8	LSBs

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte memory space. The 8-bit BMPAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally, the 14-bit BWCOUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BWCOUNT register.

The BWCOUNT register is updated after each transfer so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BMPAGE and BEAD registers must not be accessed by the DSP during BDMA operations. The source or destination of a BDMA transfer is always on-chip program or data memory.

When the BWCOUNT register is written with a nonzero value the BDMA circuit starts executing byte memory accesses with wait states set by BMWAIT. These accesses continue until the count reaches zero. When enough accesses have occurred to

INSTRUCTION SET DESCRIPTION

The ADSP-218xL series assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize on-chip memory and conform to the ADSP-218xL's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction, with up to two fetches or one write to processor memory space, during a single instruction cycle.

DEVELOPMENT SYSTEM

Analog Devices' wide range of software and hardware development tools supports the ADSP-218xL series. The DSP tools include an integrated development environment, an evaluation kit, and a serial port emulator.

VisualDSP++®† is an integrated development environment, allowing for fast and easy development, debugging, and deployment. The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy-to-use assembler that is based on an algebraic syntax; an archiver (librarian/library builder); a linker; a PROM-splitter utility; a cycle-accurate, instruction-level simulator; a C compiler; and a C run-time library that includes DSP and mathematical functions.

Debugging both C and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C and assembly code (interleaved source and object information)
- Insert break points
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- Fill and dump memory
- Source level debugging

The VisualDSP++ IDE lets programmers define and manage DSP software development. The dialog boxes and property pages let programmers configure and manage all of the ADSP-218xL development tools, including the syntax highlighting in the VisualDSP++ editor. This capability controls how the development tools process inputs and generate outputs.

The ADSP-2189M EZ-KIT Lite®‡ provides developers with a cost-effective method for initial evaluation of the powerful ADSP-218xL DSP family architecture. The ADSP-2189M EZ-KIT Lite includes a standalone ADSP-2189M DSP board supported by an evaluation suite of VisualDSP++. With this EZ-KIT Lite, users can learn about DSP hardware and software development and evaluate potential applications of the ADSP-218xL series. The ADSP-2189M EZ-KIT Lite provides an evaluation suite of the VisualDSP++ development environment with the C compiler, assembler, and linker. The size of the DSP executable that can be built using the EZ-KIT Lite tools is limited to 8K words.

The EZ-KIT Lite includes the following features:

- 75 MHz ADSP-2189M
- Full 16-Bit Stereo Audio I/O with AD73322 Codec
- RS-232 Interface
- EZ-ICE® Connector for Emulator Control
- DSP Demonstration Programs
- Evaluation Suite of VisualDSP++

The ADSP-218x EZ-ICE§ Emulator provides an easier and more cost-effective method for engineers to develop and optimize DSP systems, shortening product development cycles for faster time-to-market. ADSP-218xL series members integrate on-chip emulation support with a 14-pin ICE-Port™ interface. This interface provides a simpler target board connection that requires fewer mechanical clearance considerations than other ADSP-2100 Family EZ-ICEs. ADSP-218xL series members need not be removed from the target system when using the EZ-ICE, nor are any adapters needed. Due to the small footprint of the EZ-ICE connector, emulation can be supported in final board designs.The EZ-ICE performs a full range of functions, including:

- In-target operation
- Up to 20 breakpoints
- Single-step or full-speed operation
- Registers and memory values can be examined and altered
- PC upload and download functions
- Instruction-level emulation of program booting and execution

† VisualDSP++ is a registered trademark of Analog Devices, Inc.

‡ EZ-KIT Lite is a registered trademark of Analog Devices, Inc.

§ EZ-ICE is a registered trademark of Analog Devices, Inc.

because there are no internal pull-ups to guarantee their state during prolonged three-state conditions resulting from typical EZ-ICE debugging sessions. These resistors may be removed when the EZ-ICE is not being used.

Target System Interface Signals

When the EZ-ICE board is installed, the performance on some system signals changes. Design the system to be compatible with the following system interface signal changes introduced by the EZ-ICE board:

- EZ-ICE emulation introduces an 8 ns propagation delay between the target circuitry and the DSP on the $\overline{\text{RESET}}$ signal.
- EZ-ICE emulation introduces an 8 ns propagation delay between the target circuitry and the DSP on the $\overline{\text{BR}}$ signal.
- EZ-ICE emulation ignores $\overline{\text{RESET}}$ and $\overline{\text{BR}}$, when single-stepping.
- EZ-ICE emulation ignores $\overline{\text{RESET}}$ and $\overline{\text{BR}}$ when in Emulator Space (DSP halted).
- EZ-ICE emulation ignores the state of target $\overline{\text{BR}}$ in certain modes. As a result, the target system may take control of the DSP's external memory bus only if bus grant ($\overline{\text{BG}}$) is asserted by the EZ-ICE board's DSP.

ADDITIONAL INFORMATION

This data sheet provides a general overview of ADSP-218xL series functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-218x DSP Hardware Reference* and the *ADSP-218x DSP Instruction Set Reference*.

Table 12. Unused Pin Terminations (Continued)

Pin Name[1]	I/O 3-State (Z)[2]	Reset State	High-Z[3] Caused By	Unused Configuration
SCLK1	I/O	I		Input = High or Low, Output = Float
RFS1/$\overline{\text{IRQ0}}$	I/O	I		High or Low
DR1/FI	I	I		High or Low
TFS1/$\overline{\text{IRQ1}}$	I/O	I		High or Low
DT1/FO	O	O		Float
EE	I	I		Float
$\overline{\text{EBR}}$	I	I		Float
$\overline{\text{EBG}}$	O	O		Float
$\overline{\text{ERESET}}$	I	I		Float
$\overline{\text{EMS}}$	O	O		Float
$\overline{\text{EINT}}$	I	I		Float
ECLK	I	I		Float
ELIN	I	I		Float
ELOUT	O	O		Float

[1] CLKIN, $\overline{\text{RESET}}$, and PF3 – 0/Mode D – A are not included in this table because these pins must be used.
[2] All bidirectional pins have three-stated outputs. When the pin is configured as an output, the output is High-Z (high impedance) when inactive.
[3] High-Z = high impedance.
[4] If the CLKOUT pin is not used, turn it OFF, using CLKODIS in SPORT0 autobuffer control register.
[5] If the Interrupt/Programmable Flag pins are not used, there are two options: Option 1: When these pins are configured as INPUTS at reset and function as interrupts and input flag pins, pull the pins High (inactive). Option 2: Program the unused pins as OUTPUTS, set them to 1 prior to enabling interrupts, and let pins float.

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	K Grade (Commercial)		B Grade (Industrial)		Unit
	Min	Max	Min	Max	
V_{DD}	3.0	3.6	3.0	3.6	V
T_{AMB}	0	+70	–40	+85	°C

[1] Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	K and B Grades			Unit
			Min	Typ	Max	
V_{IH}	Hi-Level Input Voltage[2, 3]	@ V_{DD} = Max	2.0			V
		@ V_{DD} = Max	2.2			V
V_{IL}	Lo-Level Input Voltage[2, 3]	@ V_{DD} = Min			0.8	V
V_{OH}	Hi-Level Output Voltage[2, 4, 5]	@ V_{DD} = Min, I_{OH} = –0.5 mA	1.35			V
		@ V_{DD} = Min, I_{OH} = –100 µA[6]	V_{DD} – 0.3			V
V_{OL}	Lo-Level Output Voltage[2, 4, 5]	@ V_{DD} = Min, I_{OL} = 2.0 mA			0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DD} = Max, V_{IN} = V_{DD} Max			10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DD} = Max, V_{IN} = 0 V			10	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DD} = Max, V_{IN} = V_{DD} Max[8]			10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DD} = Max, V_{IN} = 0 V[8]			10	µA
C_I	Input Pin Capacitance[3, 6]	@ V_{IN} = 3.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			8	pF
C_O	Output Pin Capacitance[6, 7, 9]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			8	pF

[1] Specifications subject to change without notice.
[2] Bidirectional pins: D23–0, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A13–1, PF7–0.
[3] Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.
[4] Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–FL0, $\overline{\text{BGH}}$.
[5] Although specified for TTL outputs, all ADSP-218xL outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.
[6] Guaranteed but not tested.
[7] Three-statable pins: A13–A1, D23–D0, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF7–PF0.
[8] 0 V on $\overline{\text{BR}}$.
[9] Output pin capacitance is the capacitive load for any three-stated output pin.

Clock Signals and Reset

Table 14. Clock Signals and Reset

Parameter		ADSP-2184L, ADSP-2186L Min	ADSP-2184L, ADSP-2186L Max	ADSP-2185L, ADSP-2187L Min	ADSP-2185L, ADSP-2187L Max	Unit
Timing Requirements:						
t_{CKI}	CLKIN Period	50	150	38	100	ns
t_{CKIL}	CLKIN Width Low	20		15		ns
t_{CKIH}	CLKIN Width High	20		15		ns
Switching Characteristics:						
t_{CKL}	CLKOUT Width Low	$0.5t_{CK} - 7$		$0.5t_{CK} - 7$		ns
t_{CKH}	CLKOUT Width High	$0.5t_{CK} - 7$		$0.5t_{CK} - 7$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	0	20	ns
Control Signals Timing Requirements:						
t_{RSP}	$\overline{\text{RESET}}$ Width Low[1]	$5t_{CK}$		$5t_{CK}$		ns
t_{MS}	Mode Setup Before $\overline{\text{RESET}}$ High	2		2		ns
t_{MH}	Mode Hold After $\overline{\text{RESET}}$ High	5		5		ns

[1] Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles, assuming stable CLKIN (not including crystal oscillator start-up time).

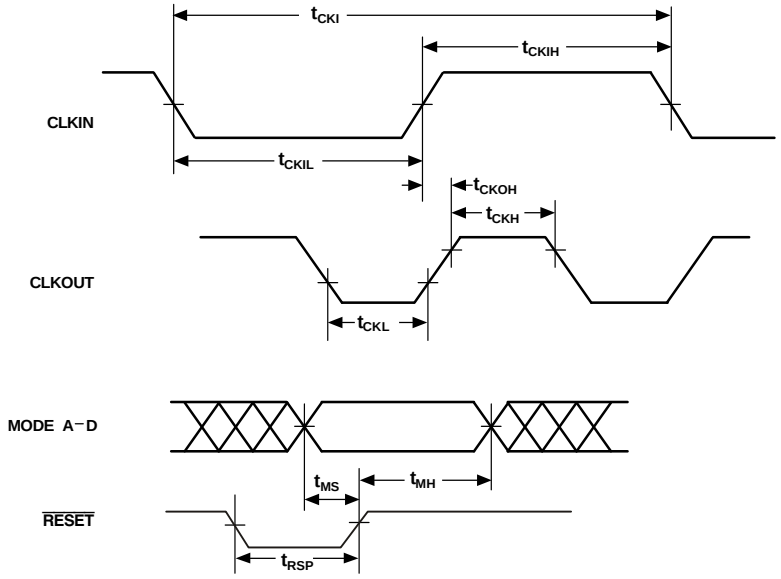


Figure 16. Clock Signals and Reset

Memory Write

Table 18. Memory Write

Parameter		Min	Max	Unit
Switching Characteristics:				
t_{DW}	Data Setup Before $\overline{WR}$ High[1]	$0.5t_{CK}$– 7 + w		ns
t_{DH}	Data Hold After $\overline{WR}$ High	$0.25t_{CK}$ – 2		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK}$ – 5 + w		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A13–0, $\overline{xMS}$ Setup Before $\overline{WR}$ Low[2]	$0.25t_{CK}$ – 6		ns
t_{DDR}	Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK}$ – 7		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK}$ – 5	$0.25t_{CK}$ + 7	ns
t_{AW}	A13–0, $\overline{xMS}$ Setup Before $\overline{WR}$ Deasserted	$0.75t_{CK}$ – 9 + w		ns
t_{WRA}	A13–0, $\overline{xMS}$ Hold After $\overline{WR}$ Deasserted	$0.25t_{CK}$ – 3		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK}$ – 5		ns

[1] w = wait states × t_{CK}.
[2] $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

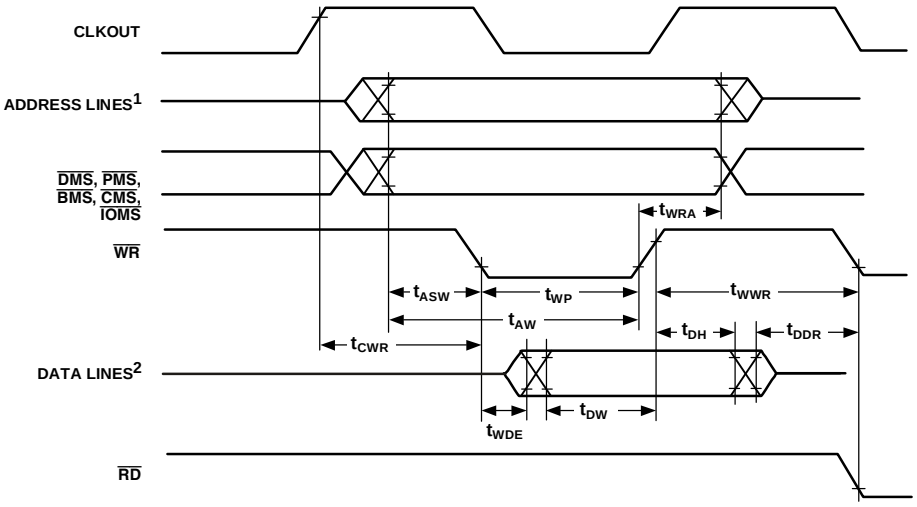


Figure 20. Memory Write

IDMA Write, Short Write Cycle

Table 21. IDMA Write, Short Write Cycle

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low Before Start of Write[1]	0		ns
t_{IWP}	Duration of Write[1, 2]	15		ns
t_{IDSU}	IAD15–0 Data Setup Before End of Write[2, 3, 4]	5		ns
t_{IDH}	IAD15–0 Data Hold After End of Write[2, 3, 4]	2		ns
Switching Characteristic:				
t_{IKHW}	Start of Write to $\overline{IACK}$ High[5]		17	ns

[1] Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2] End of Write = $\overline{IS}$ High or $\overline{IWR}$ High.
[3] If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[4] If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.
[5] For the ADSP-2185L, and the ADSP-2187L, this specification is 4 ns min., and 15 ns max.

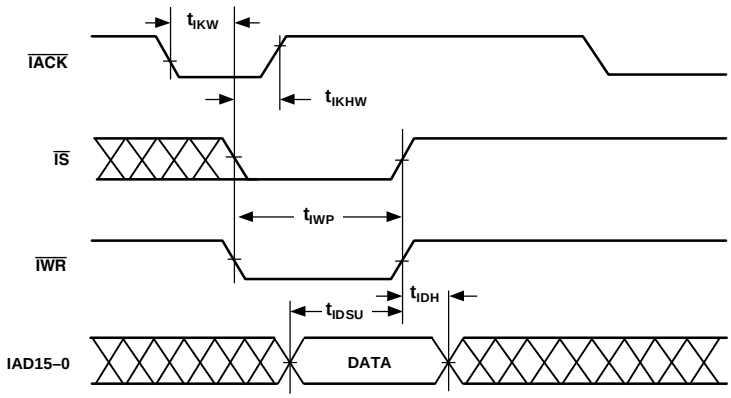


Figure 23. IDMA Write, Short Write Cycle

IDMA Write, Long Write Cycle

Table 22. IDMA Write, Long Write Cycle

Parameter		Min	Max	Unit
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low Before Start of Write[1]	0		ns
t_{IKSU}	IAD15–0 Data Setup Before End of Write[2, 3, 4]	$0.5t_{CK} + 10$		ns
t_{IKH}	IAD15–0 Data Hold After End of Write[2, 3, 4]	2		ns
Switching Characteristics:				
t_{IKLW}	Start of Write to $\overline{IACK}$ Low[4]	$1.5t_{CK}$		ns
t_{IKHW}	Start of Write to $\overline{IACK}$ High[5]		17	ns

[1] Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2] If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[3] If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.
[4] This is the earliest time for $\overline{IACK}$ Low from Start of Write. For IDMA Write cycle relationships, please refer to the *ADSP-2100 Family User's Manual*.
[5] For the ADSP-2185L, and the ADSP-2187L, this specification is 4 ns min., and 15 ns max.

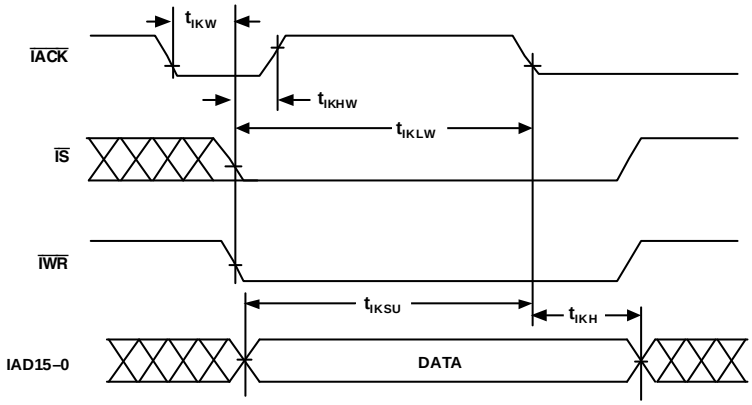


Figure 24. IDMA Write, Long Write Cycle

IDMA Read, Short Read Cycle

Table 24. IDMA Read, Short Read Cycle

Parameter[1, 2]		Min	Max	Unit
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low Before Start of Read[3]	0		ns
t_{IRP1}	Duration of Read (DM/PM1)[4, 5]	15		ns
t_{IRP2}	Duration of Read (PM2)[6, 7]	15		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High After Start of Read[3]		15	ns
t_{IKDH}	IAD15–0 Data Hold After End of Read[8]	0		ns
t_{IKDD}	IAD15–0 Data Disabled After End of Read[8]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled After Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid After Start of Read		15	ns

[1] Short Read Only must be disabled in the IDMA overlay memory mapped register. This mode is disabled by clearing (=0) Bit 14 of the IDMA overlay register, and is disabled by default upon reset.
[2] Consider using the Short Read Only mode, instead, because Short Read mode is not applicable at high clock frequencies.
[3] Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[4] DM Read or first half of PM Read.
[5] For the ADSP-2186L, this specification also has a max value of $2t_{CK} - 5$.
[6] Second half of PM Read.
[7] For the ADSP-2186L, this specification also has a max value of $t_{CK} - 5$ max.
[8] End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

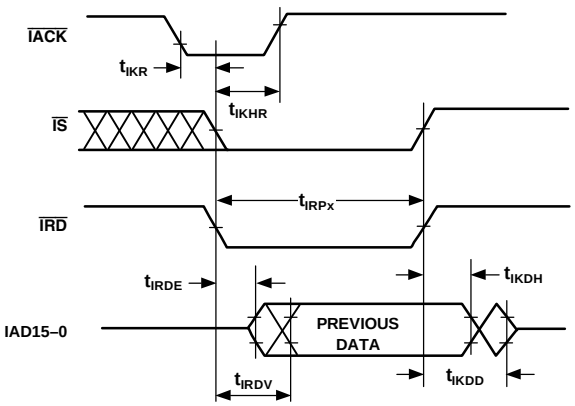


Figure 26. IDMA Read, Short Read Cycle

IDMA Read, Short Read Cycle in Short Read Only Mode

Table 25. IDMA Read, Short Read Cycle in Short Read Only Mode[1]

Parameter[2]		Min	Max	Unit
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low Before Start of Read[3]	0		ns
t_{IRP}	Duration of Read[4]	10		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High After Start of Read[3]		10	ns
t_{IKDH}	IAD15–0 Previous Data Hold After End of Read[4]	0		ns
t_{IKDD}	IAD15–0 Previous Data Disabled After End of Read[4]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled After Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid After Start of Read		10	ns

[1] Applies to the ADSP-2187L only.
[2] Short Read Only is enabled by setting Bit 14 of the IDMA overlay Register to 1 (0x3FE7). Short Read Only can be enabled by the processor core writing to the register or by an external host writing to the register. Disabled by default.
[3] Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low. Previous data remains until end of read.
[4] End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

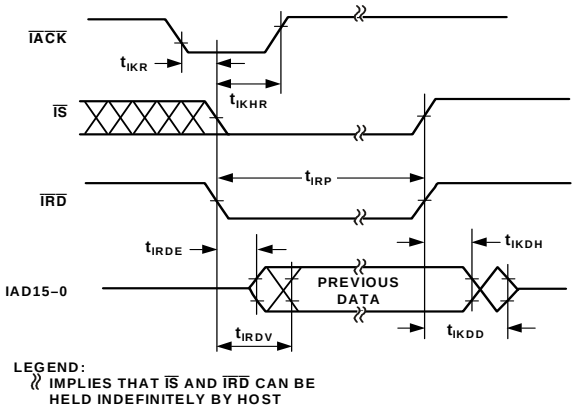


Figure 27. IDMA Read, Short Read Cycle in Short Read Only Mode

POWER DISSIPATION

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

where:

C is load capacitance.

f is the output switching frequency.

Example: In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- Application operates at V_{DD} = 3.3 V and t_{CK} = 30 ns.

$$Total\ Power\ Dissipation = P_{INT} + (C \times V_{DD}^2 \times f)$$

where:

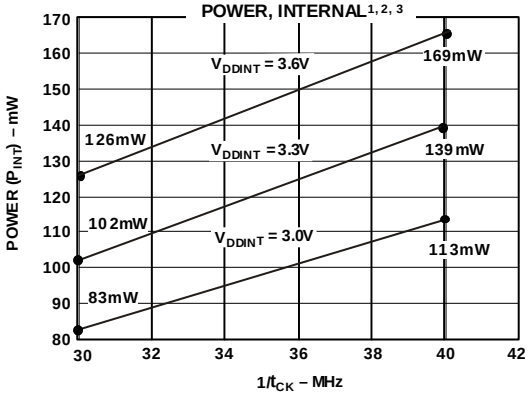
P_{INT} is the internal power dissipation from Figure 28 through Figure 31 on Page 39.

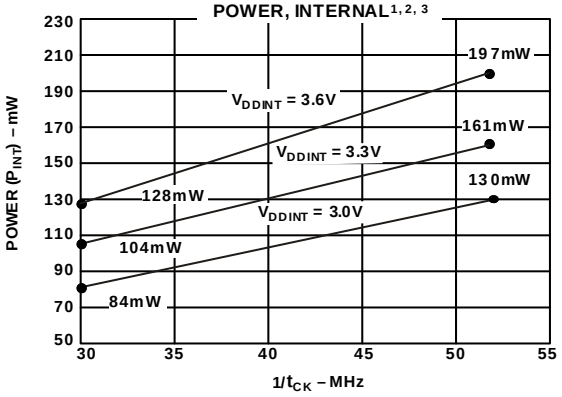
$(C \times V_{DD}^2 \times f)$ is calculated for each output, as in the example in Table 27.

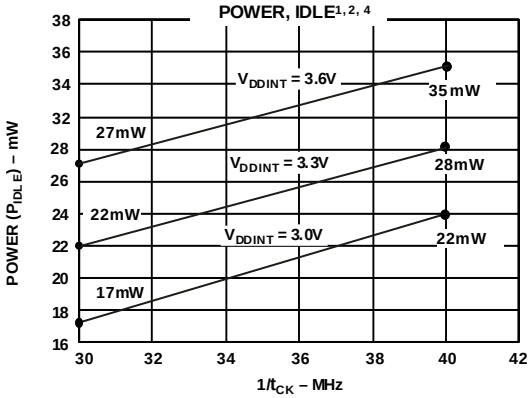
Table 27. Example Power Dissipation Calculation[1]

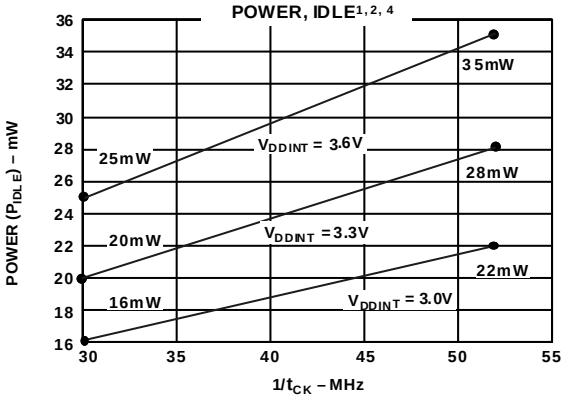
Parameters	No. of Pins	× C (pF)	× V_{DD}^2 (V)	× f (MHz)	PD (mW)
Address, $\overline{DMS}$	8	10	3.3^2	33.3	29.0
Data Output, $\overline{WR}$	9	10	3.3^2	16.67	16.3
$\overline{RD}$	1	10	3.3^2	16.67	1.8
CLKOUT	1	10	3.3^2	33.3	3.6
					= 50.7

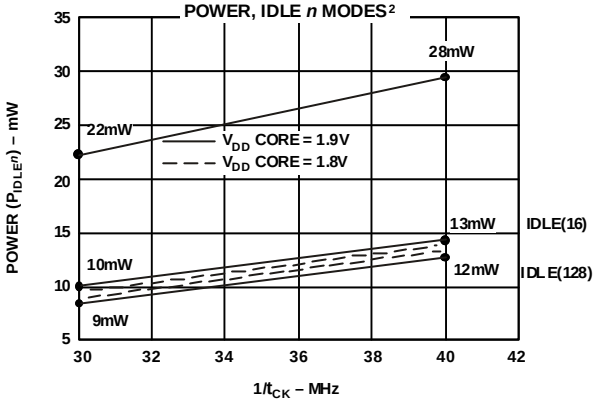
[1] Total power dissipation for this example is P_{INT} + 50.7 mW.

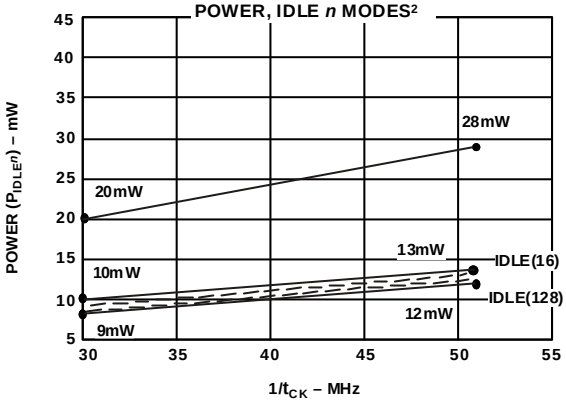












NOTES
VALID FOR ALL TEMPERATURE GRADES.
1. POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
2. TYPICAL POWER DISSIPATION AT 3.3V V_{DD} AND 25°C, EXCEPT WHERE SPECIFIED.
3. IDD MEASUREMENT TAKEN WITH ALL INSTRUCTIONS EXECUTING FROM INTERNAL MEMORY. 50% Of the INSTRUCTIONS ARE MULTIFUNCTION (TYPES 1, 4, 5, 12, 13, 14), 30% ARE TYPE 2 AND TYPE 6, AND 20% ARE IDLE INSTRUCTIONS.
4. IDLE REFERS TO STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.

Figure 28. Power vs. Frequency (ADSP-2184L)

NOTES
VALID FOR ALL TEMPERATURE GRADES.
1. POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
2. TYPICAL POWER DISSIPATION AT 3.3V V_{DD} AND 25°C, EXCEPT WHERE SPECIFIED.
3. IDD MEASUREMENT TAKEN WITH ALL INSTRUCTIONS EXECUTING FROM INTERNAL MEMORY. 50% Of the INSTRUCTIONS ARE MULTIFUNCTION (TYPES 1, 4, 5, 12, 13, 14), 30% ARE TYPE 2 AND TYPE 6, AND 20% ARE IDLE INSTRUCTIONS.
4. IDLE REFERS TO STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.

Figure 29. Power vs. Frequency (ADSP-2185L)

CAPACITIVE LOADING – ADSP-2184L, ADSP-2186L

Figure 40 and Figure 41 show the capacitive loading characteristics of the ADSP-2184L and ADSP-2186L.

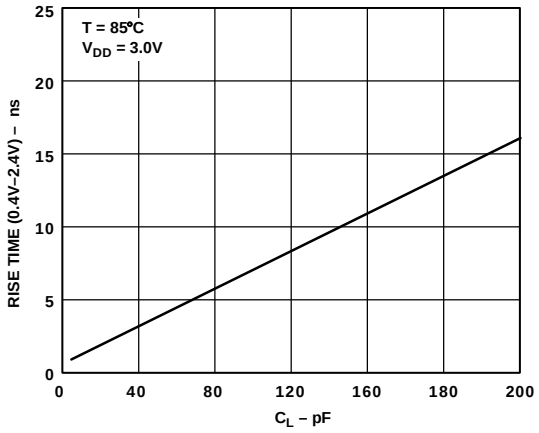


Figure 40. Typical Output Rise Time vs. Load Capacitance (at Maximum Ambient Operating Temperature)

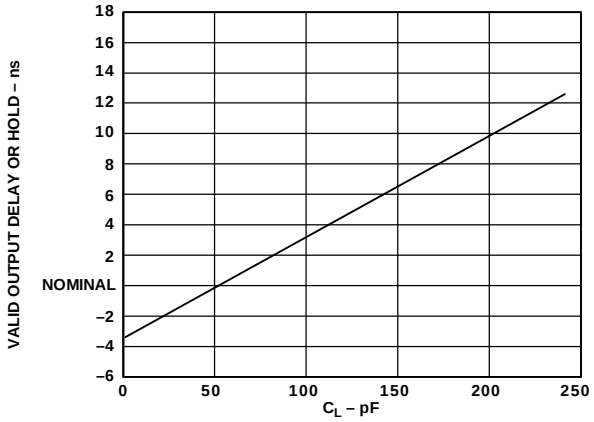


Figure 41. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

CAPACITIVE LOADING – ADSP-2185L, ADSP-2187L

Figure 42 and Figure 43 show the capacitive loading characteristics of the ADSP-2185L and ADSP-2187L.

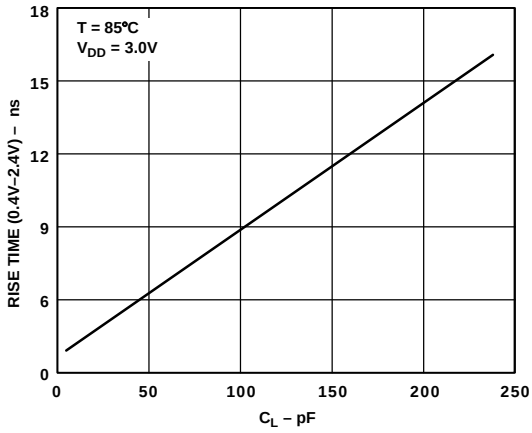


Figure 42. Typical Output Rise Time vs. Load Capacitance (at Maximum Ambient Operating Temperature)

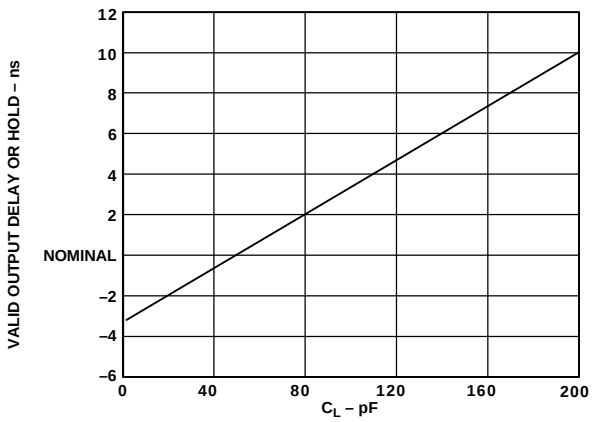


Figure 43. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

BGA PACKAGE PINOUT

The BGA package pinout is shown in Table 30. Pin names in bold text in the table replace the plain text named functions when Mode C equals 1. A plus sign (+) separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$. The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default upon reset.

Table 30. BGA Pin Assignments

Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name
A01	A2/**IAD1**	D01	NC	G01	XTAL	K01	NC
A02	A1/**IAD0**	D02	$\overline{\text{WR}}$	G02	NC	K02	NC
A03	GND	D03	NC	G03	GND	K03	NC
A04	A0	D04	$\overline{\text{BGH}}$	G04	A10/**IAD9**	K04	$\overline{\text{BMS}}$
A05	NC	D05	A9/**IAD8**	G05	NC	K05	$\overline{\text{DMS}}$
A06	GND	D06	PF1 [MODE B]	G06	NC	K06	RFS0
A07	NC	D07	PF2 [MODE C]	G07	NC	K07	TFS1/$\overline{\text{IRQ1}}$
A08	NC	D08	NC	G08	D6/**$\overline{\text{IRD}}$**	K08	SCLK1
A09	NC	D09	D13	G09	D5/**IAL**	K09	$\overline{\text{ERESET}}$
A10	D22	D10	D12	G10	NC	K10	$\overline{\text{EBR}}$
A11	GND	D11	NC	G11	NC	K11	$\overline{\text{BR}}$
A12	GND	D12	GND	G12	D4/**$\overline{\text{IS}}$**	K12	$\overline{\text{EBG}}$
B01	A4/**IAD3**	E01	V_{DDEXT}	H01	CLKIN	L01	$\overline{\text{IRQE}}$ + PF4
B02	A3/**IAD2**	E02	V_{DDEXT}	H02	GND	L02	NC
B03	GND	E03	A8/**IAD7**	H03	GND	L03	$\overline{\text{IRQL1}}$ + PF6
B04	NC	E04	FL0	H04	GND	L04	$\overline{\text{IOMS}}$
B05	NC	E05	PF0 [MODE A]	H05	V_{DDINT}	L05	GND
B06	GND	E06	FL2	H06	DT0	L06	$\overline{\text{PMS}}$
B07	V_{DDEXT}	E07	PF3 [MODE D[1]]	H07	TFS0	L07	DR0
B08	D23	E08	GND	H08	D2/**IAD15**	L08	GND
B09	D20	E09	GND	H09	D3/**$\overline{\text{IACK}}$**	L09	$\overline{\text{RESET}}$
B10	D18	E10	V_{DDEXT}	H10	GND	L10	ELIN
B11	D17	E11	GND	H11	NC	L11	ELOUT
B12	D16	E12	D10	H12	GND	L12	$\overline{\text{EINT}}$
C01	PWDACK	F01	A13/**IAD12**	J01	CLKOUT	M01	$\overline{\text{IRQL0}}$ + PF5
C02	A6/**IAD5**	F02	NC	J02	V_{DDINT}	M02	$\overline{\text{IRQL2}}$ + PF7
C03	$\overline{\text{RD}}$	F03	A12/**IAD11**	J03	NC	M03	NC
C04	A5/**IAD4**	F04	A11/**IAD10**	J04	V_{DDEXT}	M04	$\overline{\text{CMS}}$
C05	A7/**IAD6**	F05	FL1	J05	V_{DDEXT}	M05	GND
C06	$\overline{\text{PWD}}$	F06	NC	J06	SCLK0	M06	DT1/FO
C07	V_{DDEXT}	F07	NC	J07	D0/**IAD13**	M07	DR1/FI
C08	D21	F08	D7/**$\overline{\text{IWR}}$**	J08	RFS1/$\overline{\text{IRQ0}}$	M08	GND
C09	D19	F09	D11	J09	$\overline{\text{BG}}$	M09	NC
C10	D15	F10	D8	J10	D1/**IAD14**	M10	$\overline{\text{EMS}}$
C11	NC	F11	NC	J11	V_{DDINT}	M11	EE
C12	D14	F12	D9	J12	V_{DDINT}	M12	ECLK

[1] Mode D function available on ADSP-2187L only.