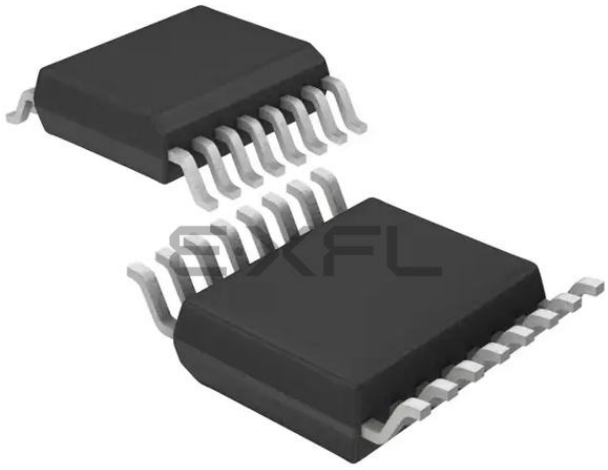

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Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	12
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
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Chapter 14
Serial Communications Interface (S08SCIV4)

Chapter 15
Serial Peripheral Interface (S08SPIV3)

Chapter 3
Modes of Operation

3.1 Introduction

The operating modes of the MC9S08SG32 Series are described in this chapter. Entry into each mode, exit from each mode, and functionality while in each of the modes are described.

3.2 Features

- Active background mode for code development
- Wait mode — CPU shuts down to conserve power; system clocks are running and full regulation is maintained
- Stop modes — System clocks are stopped and voltage regulator is in standby
  - Stop3 — All internal circuits are powered for fast recovery
  - Stop2 — Partial power down of internal circuits, RAM content is retained

3.3 Run Mode

This is the normal operating mode for the MC9S08SG32 Series. This mode is selected upon the MCU exiting reset if the BKGD/MS pin is high. In this mode, the CPU executes code from internal memory with execution beginning at the address fetched from memory at 0xFFFE–0xFFFF after reset.

3.4 Active Background Mode

The active background mode functions are managed through the background debug controller (BDC) in the HCS08 core. The BDC, together with the on-chip debug module (DBG), provide the means for analyzing MCU operation during software development.

Active background mode is entered in any of the following ways:

- When the BKGD/MS pin is low during POR or immediately after issuing a background debug force reset (see Section 5.7.2, “System Background Debug Force Reset Register (SBDFR)”)
- When a BACKGROUND command is received through the BKGD/MS pin
- When a BGND instruction is executed
- When encountering a BDC breakpoint
- When encountering a DBG breakpoint

After entering active background mode, the CPU is held in a suspended state waiting for serial background commands rather than executing instructions from the user application program.

The first byte of a series of sequential bytes being programmed in burst mode will take the same amount of time to program as a byte programmed in standard mode. Subsequent bytes will program in the burst program time provided that the conditions above are met. In the case the next sequential address is the beginning of a new row, the program time for that byte will be the standard time instead of the burst time. This is because the high voltage to the array must be disabled and then enabled again. If a new burst command has not been queued before the current command completes, then the charge pump will be disabled and high voltage removed from the array.

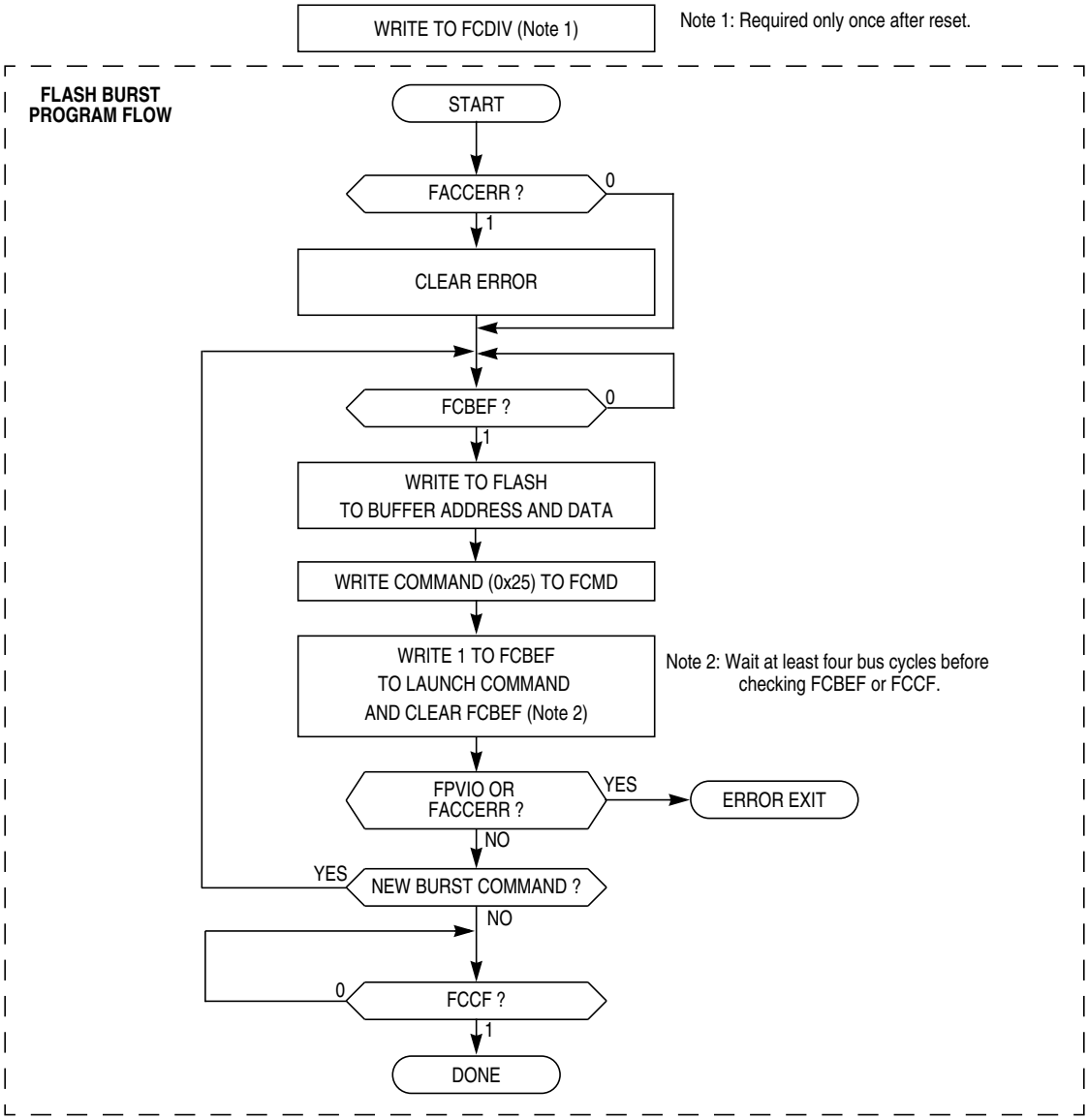


Figure 4-3. FLASH Burst Program Flowchart

The status flag corresponding to the interrupt source must be acknowledged (cleared) before returning from the ISR. Typically, the flag is cleared at the beginning of the ISR so that if another interrupt is generated by this same source, it will be registered so it can be serviced after completion of the current ISR.

5.5.2 Interrupt Vectors, Sources, and Local Masks

Table 5-2 provides a summary of all interrupt sources. Higher-priority sources are located toward the bottom of the table. The high-order byte of the address for the interrupt service routine is located at the first address in the vector address column, and the low-order byte of the address for the interrupt service routine is located at the next higher address.

When an interrupt condition occurs, an associated flag bit becomes set. If the associated local interrupt enable is 1, an interrupt request is sent to the CPU. Within the CPU, if the global interrupt mask (I bit in the CCR) is 0, the CPU will finish the current instruction; stack the PCL, PCH, X, A, and CCR CPU registers; set the I bit; and then fetch the interrupt vector for the highest priority pending interrupt. Processing then continues in the interrupt service routine.

Chapter 7
Central Processor Unit (S08CPUV3)

7.1 Introduction

This section provides summary information about the registers, addressing modes, and instruction set of the CPU of the HCS08 Family. For a more detailed discussion, refer to the *HCS08 Family Reference Manual, volume 1*, Freescale Semiconductor document order number HCS08RMV1/D.

The HCS08 CPU is fully source- and object-code-compatible with the M68HC08 CPU. Several instructions and enhanced addressing modes were added to improve C compiler efficiency and to support a new background debug system which replaces the monitor mode of earlier M68HC08 microcontrollers (MCU).

7.1.1 Features

Features of the HCS08 CPU include:

- Object code fully upward-compatible with M68HC05 and M68HC08 Families
- All registers and memory are mapped to a single 64-Kbyte address space
- 16-bit stack pointer (any size stack anywhere in 64-Kbyte address space)
- 16-bit index register (H:X) with powerful indexed addressing modes
- 8-bit accumulator (A)
- Many instructions treat X as a second general-purpose 8-bit register
- Seven addressing modes:
  - Inherent — Operands in internal registers
  - Relative — 8-bit signed offset to branch destination
  - Immediate — Operand in next object code byte(s)
  - Direct — Operand in memory at 0x0000–0x00FF
  - Extended — Operand anywhere in 64-Kbyte address space
  - Indexed relative to H:X — Five submodes including auto increment
  - Indexed relative to SP — Improves C efficiency dramatically
- Memory-to-memory data move instructions with four address mode combinations
- Overflow, half-carry, negative, zero, and carry condition codes support conditional branching on the results of signed, unsigned, and binary-coded decimal (BCD) operations
- Efficient bit manipulation instructions
- Fast 8-bit by 8-bit multiply and 16-bit by 8-bit divide instructions
- STOP and WAIT instructions to invoke low-power operating modes

7.3 Addressing Modes

Addressing modes define the way the CPU accesses operands and data. In the HCS08, all memory, status and control registers, and input/output (I/O) ports share a single 64-Kbyte linear address space so a 16-bit binary address can uniquely identify any memory location. This arrangement means that the same instructions that access variables in RAM can also be used to access I/O and control registers or nonvolatile program space.

Some instructions use more than one addressing mode. For instance, move instructions use one addressing mode to specify the source operand and a second addressing mode to specify the destination address. Instructions such as BRCLR, BRSET, CBEQ, and DBNZ use one addressing mode to specify the location of an operand for a test and then use relative addressing mode to specify the branch destination address when the tested condition is true. For BRCLR, BRSET, CBEQ, and DBNZ, the addressing mode listed in the instruction set tables is the addressing mode needed to access the operand to be tested, and relative addressing mode is implied for the branch destination.

7.3.1 Inherent Addressing Mode (INH)

In this addressing mode, operands needed to complete the instruction (if any) are located within CPU registers so the CPU does not need to access memory to get any operands.

7.3.2 Relative Addressing Mode (REL)

Relative addressing mode is used to specify the destination location for branch instructions. A signed 8-bit offset value is located in the memory location immediately following the opcode. During execution, if the branch condition is true, the signed offset is sign-extended to a 16-bit value and is added to the current contents of the program counter, which causes program execution to continue at the branch destination address.

7.3.3 Immediate Addressing Mode (IMM)

In immediate addressing mode, the operand needed to complete the instruction is included in the object code immediately following the instruction opcode in memory. In the case of a 16-bit immediate operand, the high-order byte is located in the next memory location after the opcode, and the low-order byte is located in the next memory location after that.

7.3.4 Direct Addressing Mode (DIR)

In direct addressing mode, the instruction includes the low-order eight bits of an address in the direct page (0x0000–0x00FF). During execution a 16-bit address is formed by concatenating an implied 0x00 for the high-order half of the address and the direct address from the instruction to get the 16-bit address where the desired operand is located. This is faster and more memory efficient than specifying a complete 16-bit address for the operand.

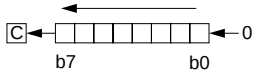
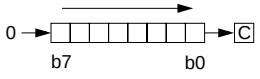
Table 7-2. Instruction Set Summary (Sheet 5 of 9)

Source Form	Operation	Address Mode	Object Code	Cycles	Cyc-by-Cyc Details	Affecton CCR	
						V 1 1 H	I N Z C
INC *oprx8*,X INC ,X INC *oprx8*,SP	Increment M ← (M) + $01 M ← (M) + $01 M ← (M) + $01	IX1 IX SP1	6C ff 7C 9E 6C ff	5 4 6	rfwpp rfwp prfwpp	↕ 1 1 –	– ↕ ↕ –
JMP *oprx16*,X JMP *oprx8*,X JMP ,X	Jump PC ← Jump Address	IX2 IX1 IX	DC ee ff EC ff FC	4 3 3	pppp ppp ppp	– 1 1 –	– – – –
JSR *oprx16*,X JSR *oprx8*,X JSR ,X	Jump to Subroutine PC ← (PC) + *n* (*n* = 1, 2, or 3) Push (PCL); SP ← (SP) – $0001 Push (PCH); SP ← (SP) – $0001 PC ← Unconditional Address	IX2 IX1 IX	DD ee ff ED ff FD	6 5 5	pssppp ssppp ssppp	– 1 1 –	– – – –

LDA *#oprx16*,X
LDA *oprx8*,X
LDA ,X
LDA *oprx16*,SP
LDA *oprx8*,SP
	Load Accumulator from Memory
	A ← (M)
		IX2
		IX1
		IX
		SP2
		SP1
			D6 ee ff
			E6 ff
			F6
			9E D6 ee ff
			9E E6 ff
				4
				3
				3
				5
				4
					prpp
					rpp
					rfp
					pprpp
					prpp
						0 1 1 –	– ↕ ↕ –

LDHX *#oprx16*,X
LDHX *oprx8*,X
LDHX ,X
LDHX *oprx16*,X
LDHX *oprx8*,X
LDHX *oprx8*,SP
	Load Index Register (H:X)
	H:X ← (M:M + $0001)
		IX
		IX2
		IX1
		SP1
			9E AE
			9E BE ee ff
			9E CE ff
			9E FE ff
				5
				6
				5
				5
					prrfp
					pprrpp
					prrpp
					prrpp
						0 1 1 –	– ↕ ↕ –

LDX *#oprx16*,X
LDX *oprx8*,X
LDX ,X
LDX *oprx16*,SP
LDX *oprx8*,SP
	Load X (Index Register Low) from Memory
	X ← (M)
		IX2
		IX1
		IX
		SP2
		SP1
			DE ee ff
			EE ff
			FE
			9E DE ee ff
			9E EE ff
				4
				3
				3
				5
				4
					prpp
					rpp
					rfp
					pprpp
					prpp
						0 1 1 –	– ↕ ↕ –

LSL *oprx8*,X LSL ,X LSL *oprx8*,SP	Logical Shift Left  (Same as ASL)	IX1 IX SP1	68 ff 78 9E 68 ff	5 4 6	rfwpp rfwp prfwpp	↕ 1 1 –	– ↕ ↕ ↕
LSR *oprx8*,X LSR ,X LSR *oprx8*,SP	Logical Shift Right  	IX1 IX SP1	64 ff 74 9E 64 ff	5 4 6	rfwpp rfwp prfwpp	↕ 1 1 –	– 0 ↕ ↕

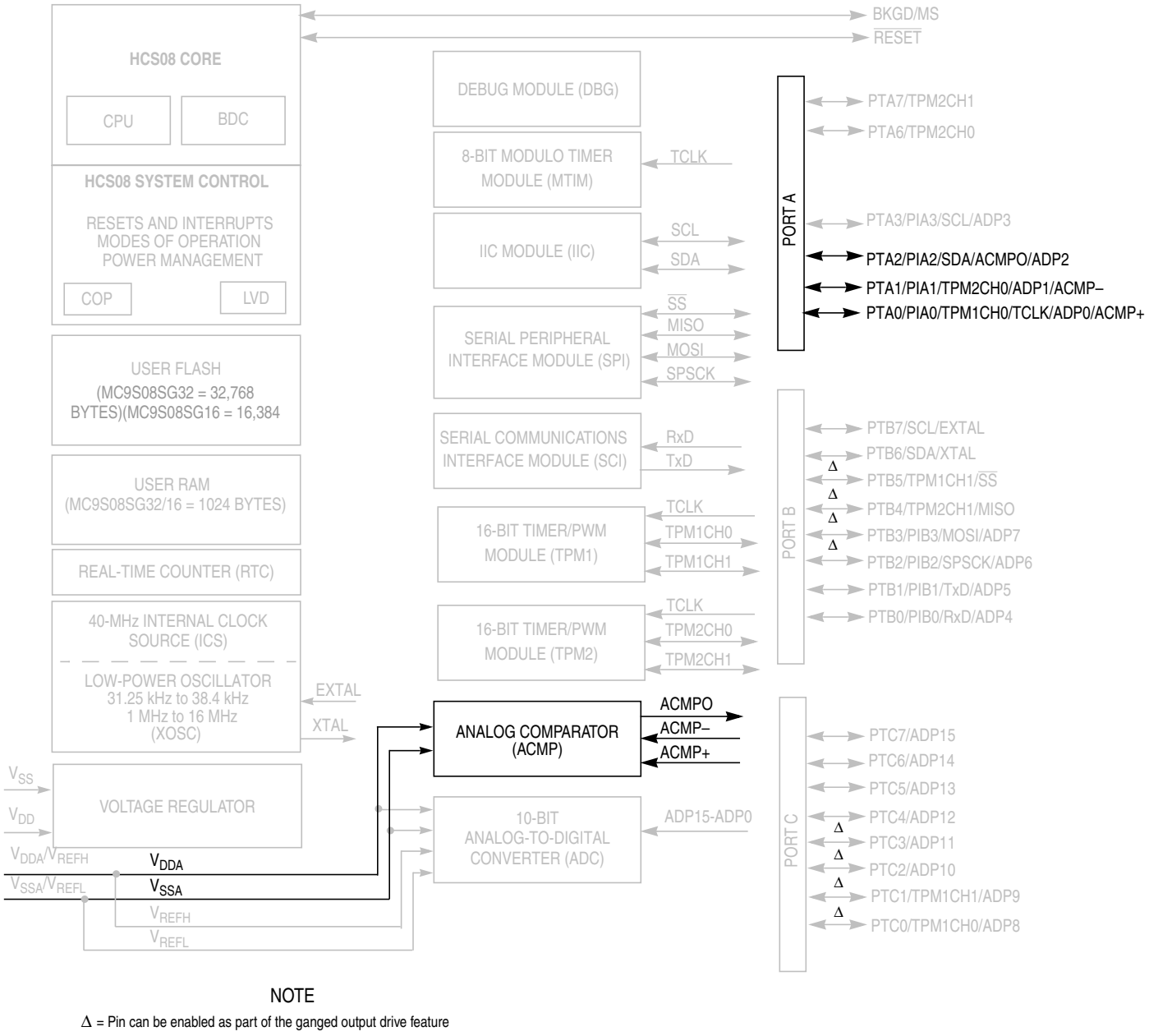


Figure 8-1. MC9S08SG32 Series Block Diagram Highlighting ACMP Block and Pins

Chapter 9
Analog-to-Digital Converter (S08ADC10V1)

9.1 Introduction

The 10-bit analog-to-digital converter (ADC) is a successive approximation ADC designed for operation within an integrated microcontroller system-on-chip.

NOTE

- MC9S08SG32 Series devices operate at a higher voltage range (2.7 V to 5.5 V) and do not include stop1 mode. Please ignore references to stop1.
- MC9S08SG32 Series devices have up to 16 analog inputs. Consequently, the APCTL3 register is not available on these devices.

The ADC channel assignments, alternate clock function, and hardware trigger function are configured as described below for the MC9S08SG32 Series family of devices.

9.1.1 Channel Assignments

The ADC channel assignments for the MC9S08SG32 Series devices are shown in Table 9-1. Reserved channels convert to an unknown value.This chapter shows bits for all S08ADCV1 channels. MC9S08SG32 Series MCUs do not use all of these channels. All bits corresponding to channels that are not available on a device are reserved.

Table 9-1. ADC Channel Assignment

ADCH	Channel	Input
00000	AD0	PTA0/AD0
00001	AD1	PTA1/ADP1
00010	AD2	PTA2/ADP2
00011	AD3	PTA3/ADP3
00100	AD4	PTB0/ADP4
00101	AD5	PTB1/ADP5
00110	AD6	PTB2/ADP6
00111	AD7	PTB3/ADP7
01000	AD8	PTC0/ADP8
01001	AD9	PTC1/ADP9
01010	AD10	PTC2/ADP10
01011	AD11	PTC3/ADP11
01100	AD12	PTC4/ADP12
01101	AD13	PTC5/ADP13
01110	AD14	PTC6/ADP14

ADCH	Channel	Input
10000	AD16	V_{SS}
10001	AD17	V_{SS}
10010	AD18	V_{SS}
10011	AD19	V_{SS}
10100	AD20	V_{SS}
10101	AD21	V_{SS}
10110	AD22	Reserved
10111	AD23	Reserved
11000	AD24	Reserved
11001	AD25	Reserved
11010	AD26	Temperature Sensor[1]
11011	AD27	Internal Bandgap[2]
11100	-	Reserved
11101	V_{REFH}	V_{DD}
11110	V_{REFL}	V_{SS}

the intermediate conversion data is lost. In 8-bit mode, there is no interlocking with ADCRH. If the MODE bits are changed, any data in ADCRL becomes invalid.

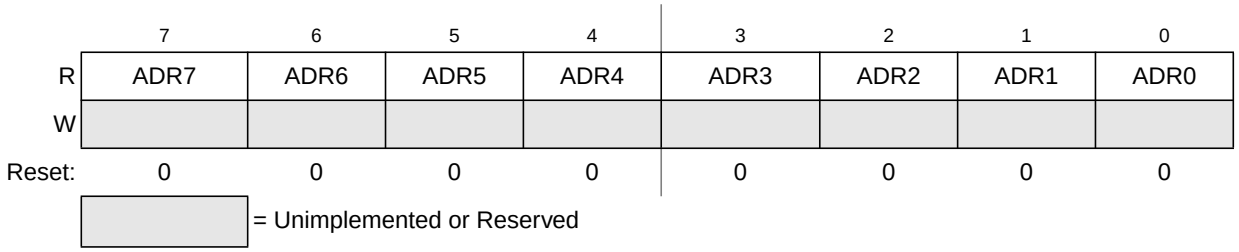


Figure 9-6. Data Result Low Register (ADCRL)

9.3.5 Compare Value High Register (ADCCVH)

In 10-bit mode, the ADCCVH register holds the upper two bits of the 10-bit compare value (ADCV[9:8]). When the compare function is enabled, these bits are compared to the upper two bits of the result following a conversion in 10-bit mode.

In 8-bit operation, ADCCVH is not used during compare.

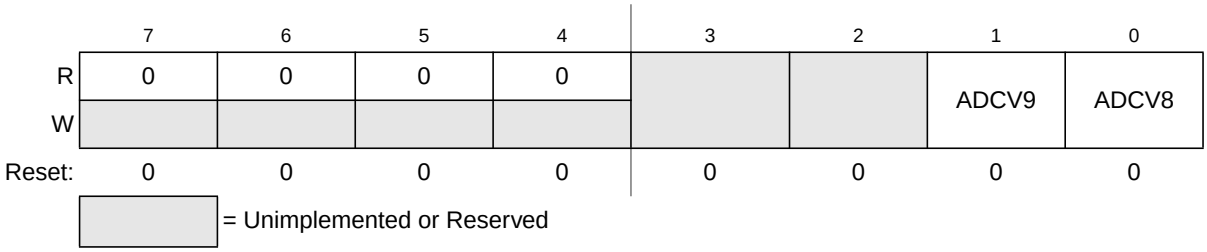


Figure 9-7. Compare Value High Register (ADCCVH)

9.3.6 Compare Value Low Register (ADCCVL)

The ADCCVL register holds the lower eight bits of the 10-bit compare value or all eight bits of the 8-bit compare value. When the compare function is enabled, bits ADCV[7:0] are compared to the lower eight bits of the result following a conversion in 10-bit or 8-bit mode.

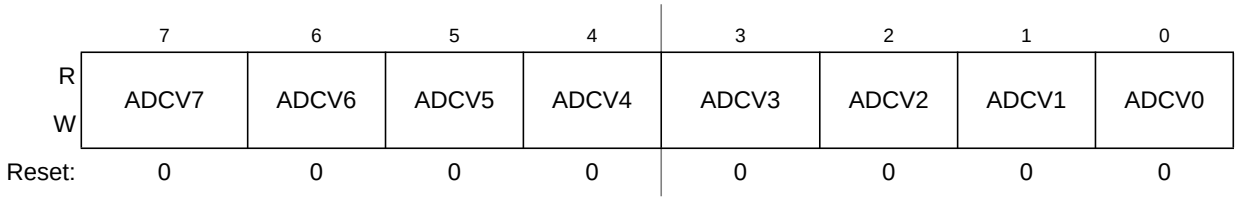


Figure 9-8. Compare Value Low Register (ADCCVL)

9.3.7 Configuration Register (ADCCFG)

ADCCFG selects the mode of operation, clock source, clock divide, and configures for low power and long sample time.

10.3.4 IIC Status Register (IICS)

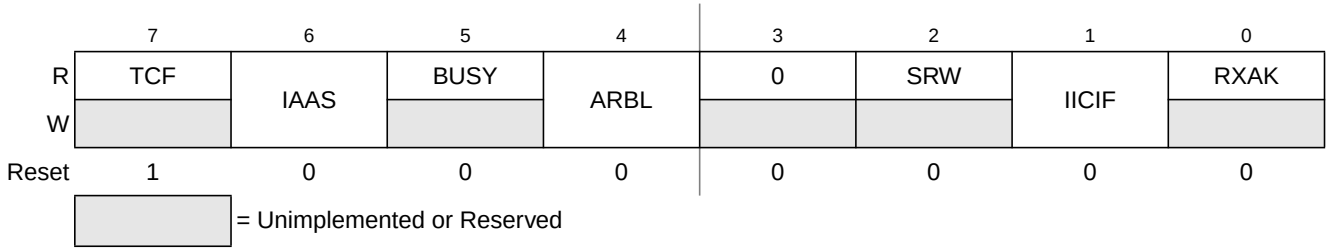


Figure 10-6. IIC Status Register (IICS)

Table 10-7. IICS Field Descriptions

Field	Description
7 TCF	**Transfer Complete Flag.** This bit is set on the completion of a byte transfer. This bit is only valid during or immediately following a transfer to the IIC module or from the IIC module.The TCF bit is cleared by reading the IICD register in receive mode or writing to the IICD in transmit mode. 0 Transfer in progress 1 Transfer complete
6 IAAS	**Addressed as a Slave.** The IAAS bit is set when the calling address matches the programmed slave address or when the GCAEN bit is set and a general call is received. Writing the IICC register clears this bit. 0 Not addressed 1 Addressed as a slave
5 BUSY	**Bus Busy.** The BUSY bit indicates the status of the bus regardless of slave or master mode. The BUSY bit is set when a start signal is detected and cleared when a stop signal is detected. 0 Bus is idle 1 Bus is busy
4 ARBL	**Arbitration Lost.** This bit is set by hardware when the arbitration procedure is lost. The ARBL bit must be cleared by software by writing a 1 to it. 0 Standard bus operation 1 Loss of arbitration
2 SRW	**Slave Read/Write.** When addressed as a slave, the SRW bit indicates the value of the R/W command bit of the calling address sent to the master. 0 Slave receive, master writing to slave 1 Slave transmit, master reading from slave
1 IICIF	**IIC Interrupt Flag.** The IICIF bit is set when an interrupt is pending. This bit must be cleared by software, by writing a 1 to it in the interrupt routine. One of the following events can set the IICIF bit: • One byte transfer completes • Match of slave address to calling address • Arbitration lost 0 No interrupt pending 1 Interrupt pending
0 RXAK	**Receive Acknowledge**. When the RXAK bit is low, it indicates an acknowledge signal has been received after the completion of one byte of data transmission on the bus. If the RXAK bit is high it means that no acknowledge signal is detected. 0 Acknowledge received 1 No acknowledge received

- CLKS bits are written to 00
- IREFS bit is written to 1
- RDIV bits are written to divide trimmed reference clock to be within the range of 31.25 kHz to 39.0625 kHz.

In FLL engaged internal mode, the ICSOUT clock is derived from the FLL clock, which is controlled by the internal reference clock. The FLL loop will lock the frequency to 1024 times the reference frequency, as selected by the RDIV bits. The ICSLCLK is available for BDC communications, and the internal reference clock is enabled.

11.4.1.2 FLL Engaged External (FEE)

The FLL engaged external (FEE) mode is entered when all the following conditions occur:

- CLKS bits are written to 00
- IREFS bit is written to 0
- RDIV bits are written to divide reference clock to be within the range of 31.25 kHz to 39.0625 kHz

In FLL engaged external mode, the ICSOUT clock is derived from the FLL clock which is controlled by the external reference clock.The FLL loop will lock the frequency to 1024 times the reference frequency, as selected by the RDIV bits. The ICSLCLK is available for BDC communications, and the external reference clock is enabled.

11.4.1.3 FLL Bypassed Internal (FBI)

The FLL bypassed internal (FBI) mode is entered when all the following conditions occur:

- CLKS bits are written to 01
- IREFS bit is written to 1.
- BDM mode is active or LP bit is written to 0

In FLL bypassed internal mode, the ICSOUT clock is derived from the internal reference clock. The FLL clock is controlled by the internal reference clock, and the FLL loop will lock the FLL frequency to 1024 times the reference frequency, as selected by the RDIV bits. The ICSLCLK will be available for BDC communications, and the internal reference clock is enabled.

11.4.1.4 FLL Bypassed Internal Low Power (FBILP)

The FLL bypassed internal low power (FBILP) mode is entered when all the following conditions occur:

- CLKS bits are written to 01
- IREFS bit is written to 1.
- BDM mode is not active and LP bit is written to 1

In FLL bypassed internal low power mode, the ICSOUT clock is derived from the internal reference clock and the FLL is disabled. The ICSLCLK will be not be available for BDC communications, and the internal reference clock is enabled.

13.3.2 RTC Counter Register (RTCCNT)

RTCCNT is the read-only value of the current RTC count of the 8-bit counter.

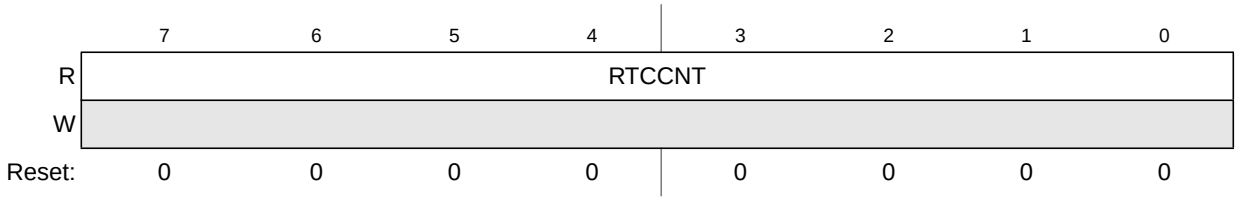


Figure 13-4. RTC Counter Register (RTCCNT)

Table 13-4. RTCCNT Field Descriptions

Field	Description
7:0 RTCCNT	RTC Count. These eight read-only bits contain the current value of the 8-bit counter. Writes have no effect to this register. Reset, writing to RTCMOD, or writing different values to RTCLKS and RTCPS clear the count to 0x00.

13.3.3 RTC Modulo Register (RTCMOD)

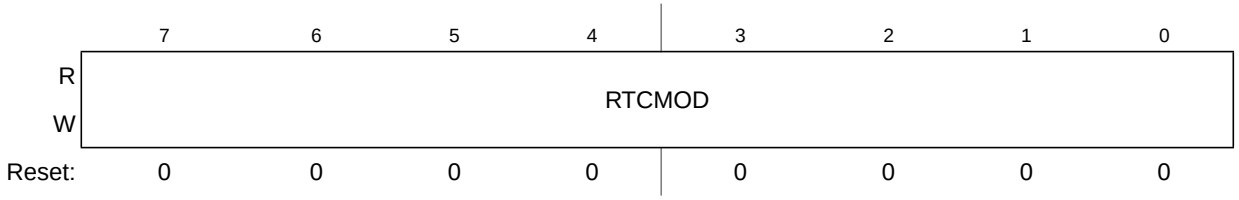


Figure 13-5. RTC Modulo Register (RTCMOD)

Table 13-5. RTCMOD Field Descriptions

Field	Description
7:0 RTCMOD	RTC Modulo. These eight read/write bits contain the modulo value used to reset the count to 0x00 upon a compare match and set the RTIF status bit. A value of 0x00 sets the RTIF bit on each rising edge of the prescaler output. Writing to RTCMOD resets the prescaler and the RTCCNT counters to 0x00. Reset sets the modulo to 0x00.

13.4 Functional Description

The RTC is composed of a main 8-bit up-counter with an 8-bit modulo register, a clock source selector, and a prescaler block with binary-based and decimal-based selectable values. The module also contains software selectable interrupt logic.

After any MCU reset, the counter is stopped and reset to 0x00, the modulus register is set to 0x00, and the prescaler is off. The 1-kHz internal oscillator clock is selected as the default clock source. To start the prescaler, write any value other than zero to the prescaler select bits (RTCPS).

Three clock sources are software selectable: the low power oscillator clock (LPO), the external clock (ERCLK), and the internal clock (IRCLK). The RTC clock select bits (RTCLKS) select the desired clock source. If a different value is written to RTCLKS, the prescaler and RTCCNT counters are reset to 0x00.

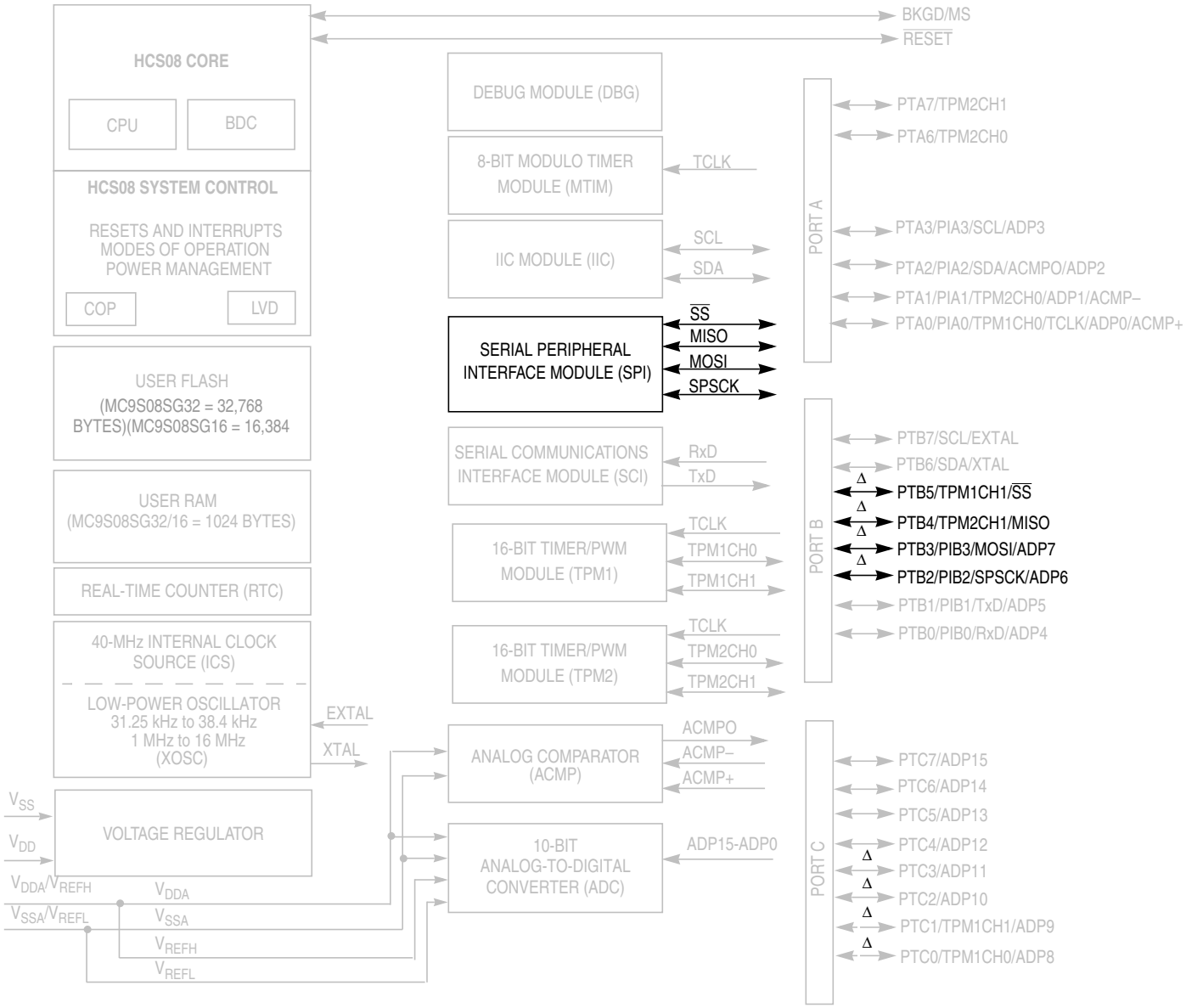
Chapter 15
Serial Peripheral Interface (S08SPIV3)

15.1 Introduction

The serial peripheral interface (SPI) module provides for full-duplex, synchronous, serial communication between the MCU and peripheral devices. These peripheral devices can include other microcontrollers, analog-to-digital converters, shift registers, sensors, memories, and so forth.

The SPI runs at a baud rate up to that of the bus clock divided by two in master mode and bus clock divided by four in slave mode. The SPI operation can be interrupt driven or software can poll the status flags.

All devices in the MC9S08SG32 Series MCUs contain one SPI module, as shown in the following block diagram. Figure 15-1 shows the MC9S08SG32 Series block diagram with the SPI modules highlighted.



NOTE

- PTC7-PTC0 and PTA7-PTA6 are not available on 16-pin Packages
- PTC7-PTC4 and PTA7-PTA6 are not available on 20-pin Packages
- For the 16-pin and 20-pin packages: V_{DDA}/V_{REFH} and V_{SSA}/V_{REFL} are double bonded to V_{DD} and V_{SS} respectively.

Δ = Pin can be enabled as part of the ganged output drive feature

Figure 15-1. MC9S08SG32 Series Block Diagram Highlighting SPI Block and Pin

Table A-6. DC Characteristics (continued)

#	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit	Temp Rated	
									Standard	AEC Grade 0
9	P	Input leakage current (per pin)	$\|I_{In}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	—	1	µA	♦	—
				temperature > 125 C	—	—	2	µA	—	♦
10	P	Hi-Z (off-state) leakage current (per pin) input/output port pins	$\|I_{OZ}\|$	$V_{In} = V_{DD}$ or V_{SS}; temperature	—	—	1	µA	♦	—
		$\overline{\text{RESET}}$		$V_{In} = V_{DD}$ or V_{SS}	—	—	2	µA	♦	—
		Input/Output Port pins		$V_{In} = V_{DD}$ or V_{SS}; temperature > 125 C	—	0.2	2	µA	—	♦
11	P	Pullup or Pulldown[2] resistors; when enabled I/O pins	R_{PU},R_{PD}	—	17	37	52	kΩ	♦	♦
	C	$\overline{\text{RESET}}$[3]	R_{PU}	—	17	37	52	kΩ	♦	♦
12	D	DC injection current [4, 5, 6, 7]	I_{IC}						♦	♦
		Single pin limit		$V_{IN} > V_{DD}$	0	—	2	mA	♦	♦
				$V_{IN} < V_{SS}$,	0	—	–0.2	mA	♦	♦
		Total MCU limit, includes sum of all stressed pins		$V_{IN} > V_{DD}$	0	—	25	mA	♦	♦
				$V_{IN} < V_{SS}$,	0	—	–5	mA	♦	♦
13	D	Input Capacitance, all pins	C_{In}	—	—	—	8	pF	♦	♦
14	D	RAM retention voltage	V_{RAM}	—	—	0.6	1.0	V	♦	♦
15	D	POR re-arm voltage[8]	V_{POR}	—	0.9	1.4	2.0	V	♦	♦
16	D	POR re-arm time[9]	t_{POR}	—	10	—	—	µs	♦	♦
17	P	Low-voltage detection threshold — high range V_{DD} falling	V_{LVD1}	—	3.9	4.0	4.1	V	♦	—
		V_{DD} rising		—	3.88 3.98	4.0 4.1	4.12 4.22	V	—	♦

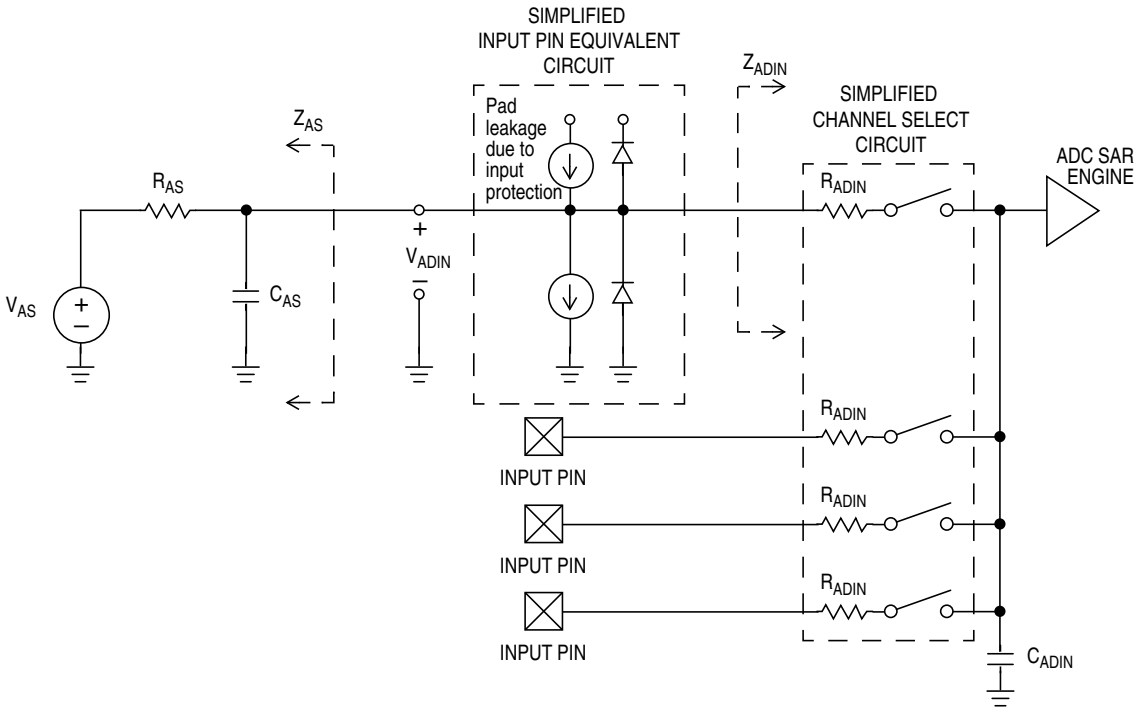


Figure A-9. ADC Input Impedance Equivalency Diagram

The following pages are mechanical specifications for MC9S08SG32 Series package options. See Table B-2 for the document number for each package type.

Table B-2. Package Information

Pin Count	Type	Designator	Document No.
28	TSSOP	TL	98ARS23923W
20	TSSOP	TJ	98ASH70169A
16	TSSOP	TG	98ASH70247A

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