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Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08sg16e1wtlr

Freescale Semiconductor, Inc.
Data Sheet Addendum

Addendum to Rev. 8.1 of the MC9S08SG32 Covers: MC9S08SG32 and MC9S08SG16

This addendum identifies changes to Rev. 8.1 of the MC9S08SG32 data sheet (covering MC9S08SG32 and MC9S08SG16). The changes described in this addendum have not been implemented in the specified pages.

1 Update to the "Nonvolatile Register Summary" table for NVFTRIM and NVOPT

Location:	Table 4-4. Nonvolatile Register Summary, Page 47

For the NVFTRIM and NVOPT registers in Table 4-4, "Nonvolatile Register Summary," all reserved bits should be marked as "—" (not "0").

2 Update to the "Instruction Set Summary" table for BRA and BRN

Location:	Table 7-2. Instruction Set Summary (Sheet 3 of 9), Page 106

In Table 7-2, "Instruction Set Summary," remove "(if I = 1)" from the BRA instruction and remove "(if I = 0)" from the BRN instruction. The BRA and BRN instructions do not depend on the I bit.

Chapter 14
Serial Communications Interface (S08SCIV4)

Chapter 15
Serial Peripheral Interface (S08SPIV3)

Table 3-1 shows all of the control bits that affect stop mode selection and the mode selected under various conditions. The selected mode is entered following the execution of a STOP instruction.

Table 3-1. Stop Mode Selection

STOPE	ENBDM [1]	LVDE	LVDSE	PPDC	Stop Mode
0	x	x		x	Stop modes disabled; illegal opcode reset if STOP instruction executed
1	1	x		x	Stop3 with BDM enabled [2]
1	0	Both bits must be 1		x	Stop3 with voltage regulator active
1	0	Either bit a 0		0	Stop3
1	0	Either bit a 0		1	Stop2

[1] ENBDM is located in the BDCSCR, which is only accessible through BDC commands, see Section 17.4.1.1, "BDC Status and Control Register (BDCSCR)".

[2] When in Stop3 mode with BDM enabled, The S_{IDD} will be near R_{IDD} levels because internal clocks are enabled.

3.6.1 Stop3 Mode

Stop3 mode is entered by executing a STOP instruction under the conditions as shown in Table 3-1. The states of all of the internal registers and logic, RAM contents, and I/O pin states are maintained.

Stop3 can be exited by asserting $\overline{RESET}$, or by an interrupt from one of the following sources: the real-time counter (RTC), LVD system, ACMP, ADC, SCI or any pin interrupts.

If stop3 is exited by means of the $\overline{RESET}$ pin, then the MCU is reset and operation will resume after taking the reset vector. Exit by means of one of the internal interrupt sources results in the MCU taking the appropriate interrupt vector.

3.6.1.1 LVD Enabled in Stop3 Mode

The LVD system is capable of generating either an interrupt or a reset when the supply voltage drops below the LVD voltage. For configuring the LVD system for interrupt or reset, refer to Section 5.6, "Low-Voltage Detect (LVD) System". If the LVD is enabled in stop (LVDE and LVDSE bits in SPMSC1 both set) at the time the CPU executes a STOP instruction, then the voltage regulator remains active during stop mode.

For the ADC to operate in stop mode, the LVD must be enabled when entering stop3.

For the ACMP to operate in stop mode with compare to internal bandgap option, the LVD must be enabled when entering stop3.

3.6.1.2 Active BDM Enabled in Stop3 Mode

Entry into the active background mode from run mode is enabled if ENBDM in BDCSCR is set. This register is described in Chapter 17, "Development Support." If ENBDM is set when the CPU executes a STOP instruction, the system clocks to the background debug logic remain active when the MCU enters stop mode. Because of this, background debug communication remains possible. In addition, the voltage regulator does not enter its low-power standby state but maintains full internal regulation.

other than the most experienced programmers because it can lead to subtle program errors that are difficult to debug.

The interrupt service routine ends with a return-from-interrupt (RTI) instruction which restores the CCR, A, X, and PC registers to their pre-interrupt values by reading the previously saved information from the stack.

NOTE

For compatibility with M68HC08 devices, the H register is not automatically saved and restored. It is good programming practice to push H onto the stack at the start of the interrupt service routine (ISR) and restore it immediately before the RTI that is used to return from the ISR.

If more than one interrupt is pending when the I bit is cleared, the highest priority source is serviced first (see Table 5-2).

5.5.1 Interrupt Stack Frame

Figure 5-1 shows the contents and organization of a stack frame. Before the interrupt, the stack pointer (SP) points at the next available byte location on the stack. The current values of CPU registers are stored on the stack starting with the low-order byte of the program counter (PCL) and ending with the CCR. After stacking, the SP points at the next available location on the stack which is the address that is one less than the address where the CCR was saved. The PC value that is stacked is the address of the instruction in the main program that would have executed next if the interrupt had not occurred.
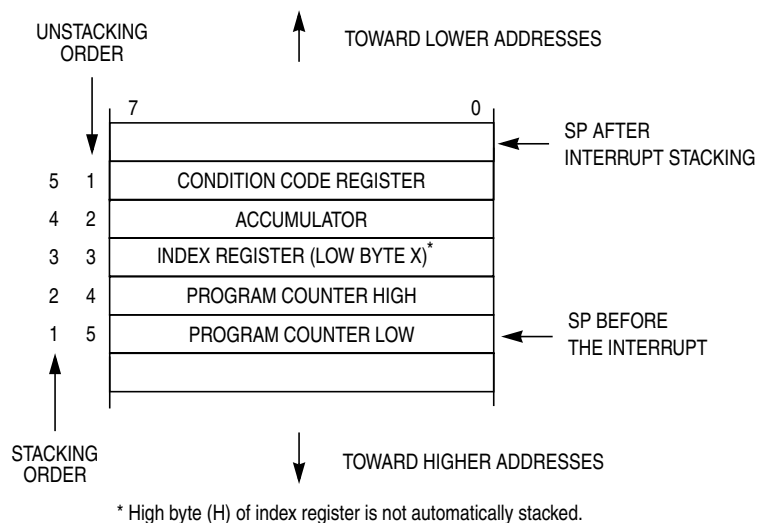

Figure 5-1. Interrupt Stack Frame

When an RTI instruction is executed, these values are recovered from the stack in reverse order. As part of the RTI sequence, the CPU fills the instruction pipeline by reading three bytes of program information, starting from the PC address recovered from the stack.

5.7.4 System Options Register 2 (SOPT2)

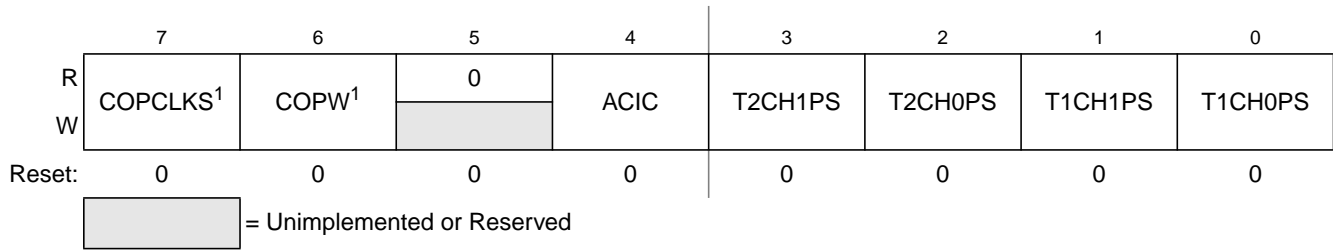This high page register contains bits to configure MCU specific features on the MC9S08SG32 Series devices.

	7	6	5	4	3	2	1	0
R	COPCLKS[1]	COPW[1]	0	ACIC	T2CH1PS	T2CH0PS	T1CH1PS	T1CH0PS
W								
Reset:	0	0	0	0	0	0	0	0

☐ = Unimplemented or Reserved

Figure 5-5. System Options Register 2 (SOPT2)

[1] This bit can be written only one time after reset. Additional writes are ignored.

Table 5-6. SOPT2 Register Field Descriptions

Field	Description
7 COPCLKS	**COP Watchdog Clock Select** — This write-once bit selects the clock source of the COP watchdog. 0 Internal 1-kHz clock is source to COP. 1 Bus clock is source to COP.
6 COPW	**COP Window** — This write-once bit selects the COP operation mode. When set, the 0x55-0xAA write sequence to the SRS register must occur in the last 25% of the selected period. Any write to the SRS register during the first 75% of the selected period will reset the MCU. 0 Normal COP operation 1 Window COP operation (only if COPCLKS = 1)
4 ACIC	**Analog Comparator to Input Capture Enable** — This bit connects the output of ACMP to TPM1 input channel 0. 0 ACMP output not connected to TPM1 input channel 0. 1 ACMP output connected to TPM1 input channel 0.
3 T2CH1PS	**TPM2CH1 Pin Select** — This selects the location of the TPM2CH1 pin of the TPM2 module. 0 TPM2CH1 on PTB4. 1 TPM2CH1 on PTA7.
2 T2CH0PS	**TPM2CH0 Pin Select** — This bit selects the location of the TPM2CH0 pin of the TPM2 module. 0 TPM2CH0 on PTA1. 1 TPM2CH0 on PTA6.
1 T1CH1PS	**TPM1CH1 Pin Select** — This bit selects the location of the TPM1CH1 pin of the TPM1 module. 0 TPM1CH1 on PTB5. 1 TPM1CH1 on PTC1.
0 T1CH0PS	**TPM1CH0 Pin Select** — This bit selects the location of the TPM1CH0 pin of the TPM1 module. 0 TPM1CH0 on PTA0. 1 TPM1CH0 on PTC0.

Table 7-2. Instruction Set Summary (Sheet 8 of 9)

Source Form	Operation	Address Mode	Object Code	Cycles	Cyc-by-Cyc Details	Affecton CCR			
						V 1 1 H		I N Z C	

SUB #opr8i
SUB opr8a
SUB opr16a
SUB oprx16,X
SUB oprx8,X
SUB ,X
SUB oprx16,SP
SUB oprx8,SP
	Subtract
	A ← (A) − (M)
		IMM
		DIR
		EXT
		IX2
		IX1
		IX
		SP2
		SP1
			A0 ii
			B0 dd
			C0 hh ll
			D0 ee ff
			E0 ff
			F0
			9E D0 ee ff
			9E E0 ff
				2
				3
				4
				4
				3
				3
				5
				4
					pp
					rpp
					prpp
					prpp
					rpp
					rfp
					pprpp
					prpp
						↕ 1 1 –		– ↕ ↕ ↕	

SWI	Software Interrupt PC ← (PC) + $0001 Push (PCL); SP ← (SP) − $0001 Push (PCH); SP ← (SP) − $0001 Push (X); SP ← (SP) − $0001 Push (A); SP ← (SP) − $0001 Push (CCR); SP ← (SP) − $0001 I ← 1; PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	INH	83	11	sssssvvfppp	– 1 1 –		1 – – –	
TAP	Transfer Accumulator to CCR CCR ← (A)	INH	84	1	p	↕ 1 1 ↕		↕ ↕ ↕ ↕	
TAX	Transfer Accumulator to X (Index Register Low) X ← (A)	INH	97	1	p	– 1 1 –		– – – –	
TPA	Transfer CCR to Accumulator A ← (CCR)	INH	85	1	p	– 1 1 –		– – – –	
TST opr8a TSTA TSTX TST oprx8,X TST ,X TST oprx8,SP	Test for Negative or Zero (M) − $00 (A) − $00 (X) − $00 (M) − $00 (M) − $00 (M) − $00	DIR INH INH IX1 IX SP1	3D dd 4D 5D 6D ff 7D 9E 6D ff	4 1 1 4 3 5	rfpp p p rfpp rfp prfpp	0 1 1 –		– ↕ ↕ –	
TSX	Transfer SP to Index Reg. H:X ← (SP) + $0001	INH	95	2	fp	– 1 1 –		– – – –	
TXA	Transfer X (Index Reg. Low) to Accumulator A ← (X)	INH	9F	1	p	– 1 1 –		– – – –	

9.4.5 Automatic Compare Function

The compare function is enabled by the ACFE bit. The compare function can be configured to check for an upper or lower limit. After the input is sampled and converted, the compare value (ADCCVH and ADCCVL) is subtracted from the conversion result. When comparing to an upper limit (ACFGT = 1), if the conversion result is greater-than or equal-to the compare value, COCO is set. When comparing to a lower limit (ACFGT = 0), if the result is less than the compare value, COCO is set. An ADC interrupt is generated upon the setting of COCO if the ADC interrupt is enabled (AIEN = 1).

The subtract operation of two positive values (the conversion result less the compare value) results in a signed value that is 1-bit wider than the bit-width of the two terms. The final value transferred to the ADCRH and ADCRL registers is the result of the subtraction operation, excluding the sign bit. The value of the sign bit can be derived based on ACFGT control setting. When ACFGT=1, the sign bit of any value stored in ADCRH and ADCRL is always 0, indicating a positive result for the subtract operation. When ACFGT = 1, the sign bit of any result is always 1, indicating a negative result for the subtract operation.

Upon completion of a conversion while the compare function is enabled, if the compare condition is not true, COCO is not set and no data is transferred to the result registers.

NOTE

The compare function can monitor the voltage on a channel while the MCU is in wait or stop3 mode. The ADC interrupt wakes the MCU when the compare condition is met.

An example of compare operation eases understanding of the compare feature. If the ADC is configured for 10-bit operation, ACFGT=0, and ADCCVH:ADCCVL= 0x200, then a conversion result of 0x080 causes the compare condition to be met and the COCO bit is set. A value of 0x280 is stored in ADCRH:ADCRL. This is signed data without the sign bit and must be combined with a derived sign bit to have meaning. The value stored in ADCRH:ADCRL is calculated as follows.

The value to interpret from the data is (Result – Compare Value) = (0x080 – 0x200) = –0x180. A standard method for handling subtraction is to convert the second term to its 2's complement, and then add the two terms. First calculate the 2's complement of 0x200 by complementing each bit and adding 1. Note that prior to complementing, a sign bit of 0 is added so that the 10-bit compare value becomes a 11-bit signed value that is always positive.

```
    %101 1111 1111          <= 1's complement of 0x200 compare value
  +          %1
    ---------------
    %110 0000 0000          <= 2's complement of 0x200 compare value
```

Then the conversion result of 0x080 is added to 2's complement of 0x200:

```
    %000 1000 0000
  + %110 0000 0000
    ---------------
    %110 1000 0000          <= Subtraction result is –0x180 in signed 11-bit data
```

11.1.2   Features

Key features of the ICS module follow. For device specific information, refer to the ICS Characteristics in the Electricals section of the documentation.

- Frequency-locked loop (FLL) is trimmable for accuracy using the internal 32 kHz reference over the specified temperature and voltage ranges
  - 0.1% resolution using 9-bit TRIM:FTRIM
  - 1.5% deviation for –40 °C to 125 °C standard-temperature rated devices
  - 3% deviation for AEC Grade 0 high-temperature rated devices (-40 to 150 °C)
- Internal or external reference clocks up to 5 MHz can be used to control the FLL
  - 3-bit select for reference divider is provided
- Internal reference clock has 9 trim bits available
- Internal or external reference clocks can be selected as the clock source for the MCU
- Whichever clock is selected as the source can be divided down
  - 2-bit select for clock divider is provided
    - Allowable dividers are: 1, 2, 4, 8
    - BDC clock is provided as a constant divide by 2 of the DCO output
- Control signals for a low power oscillator as the external reference clock are provided
  - HGO, RANGE, EREFS, ERCLKEN, EREFSTEN
- FLL Engaged Internal mode is automatically selected out of reset

11.1.3   Block Diagram

Figure 11-2 is the ICS block diagram.

11.1.4.4 FLL Bypassed Internal Low Power (FBILP)

In FLL bypassed internal low power mode, the FLL is disabled and bypassed, and the ICS supplies a clock derived from the internal reference clock. The BDC clock is not available.

11.1.4.5 FLL Bypassed External (FBE)

In FLL bypassed external mode, the FLL is enabled and controlled by an external reference clock, but is bypassed. The ICS supplies a clock derived from the external reference clock. The external reference clock can be an external crystal/resonator supplied by an OSC controlled by the ICS, or it can be another external clock source. The BDC clock is supplied from the FLL.

11.1.4.6 FLL Bypassed External Low Power (FBELP)

In FLL bypassed external low power mode, the FLL is disabled and bypassed, and the ICS supplies a clock derived from the external reference clock. The external reference clock can be an external crystal/resonator supplied by an OSC controlled by the ICS, or it can be another external clock source. The BDC clock is not available.

11.1.4.7 Stop (STOP)

In stop mode the FLL is disabled and the internal or external reference clocks can be selected to be enabled or disabled. The BDC clock is not available and the ICS does not provide an MCU clock source.

11.2 External Signal Description

There are no ICS signals that connect off chip.

11.3 Register Definition

Figure 11-1 is a summary of ICS registers.

Table 11-1. ICS Register Summary

Name		7	6	5	4	3	2	1	0
ICSC1	R	CLKS		RDIV			IREFS	IRCLKEN	IREFSTEN
	W	CLKS		RDIV			IREFS	IRCLKEN	IREFSTEN
ICSC2	R	BDIV		RANGE	HGO	LP	EREFS	ERCLKEN	EREFSTEN
	W	BDIV		RANGE	HGO	LP	EREFS	ERCLKEN	EREFSTEN
ICSTRM	R	TRIM							
	W	TRIM							
ICSSC	R	0	0	0	IREFST	CLKST		OSCINIT	FTRIM
	W								FTRIM

11.3.2 ICS Control Register 2 (ICSC2)

	7	6	5	4	3	2	1	0
R	BDIV		RANGE	HGO	LP	EREFS	ERCLKEN	EREFSTEN
W								
Reset:	0	1	0	0	0	0	0	0
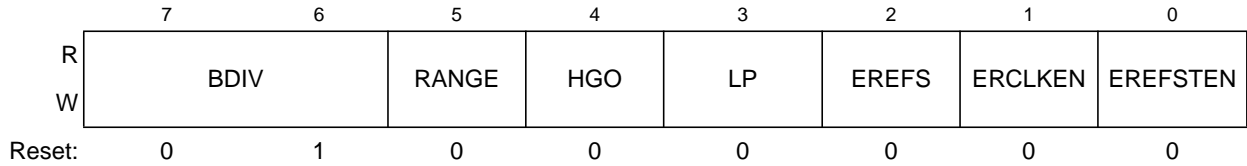
Figure 11-4. ICS Control Register 2 (ICSC2)

Table 11-3. ICS Control Register 2 Field Descriptions

| Field	Description
7:6 BDIV	**Bus Frequency Divider** — Selects the amount to divide down the clock source selected by the CLKS bits. This controls the bus frequency. 00 Encoding 0 — Divides selected clock by 1 01 Encoding 1 — Divides selected clock by 2 (reset default) 10 Encoding 2 — Divides selected clock by 4 11 Encoding 3 — Divides selected clock by 8
5 RANGE	**Frequency Range Select** — Selects the frequency range for the external oscillator. 1 High frequency range selected for the external oscillator 0 Low frequency range selected for the external oscillator
4 HGO	**High Gain Oscillator Select** — The HGO bit controls the external oscillator mode of operation. 1 Configure external oscillator for high gain operation 0 Configure external oscillator for low power operation
3 LP	**Low Power Select** — The LP bit controls whether the FLL is disabled in FLL bypassed modes. 1 FLL is disabled in bypass modes unless BDM is active 0 FLL is not disabled in bypass mode
2 EREFS	**External Reference Select** — The EREFS bit selects the source for the external reference clock. 1 Oscillator requested 0 External Clock Source requested
1 ERCLKEN	**External Reference Enable** — The ERCLKEN bit enables the external reference clock for use as ICSERCLK. 1 ICSERCLK active 0 ICSERCLK inactive
0 EREFSTEN	**External Reference Stop Enable** — The EREFSTEN bit controls whether or not the external reference clock remains enabled when the ICS enters stop mode. 1 External reference clock stays enabled in stop if ERCLKEN is set or if ICS is in FEE, FBE, or FBELP mode before entering stop 0 External reference clock is disabled in stop
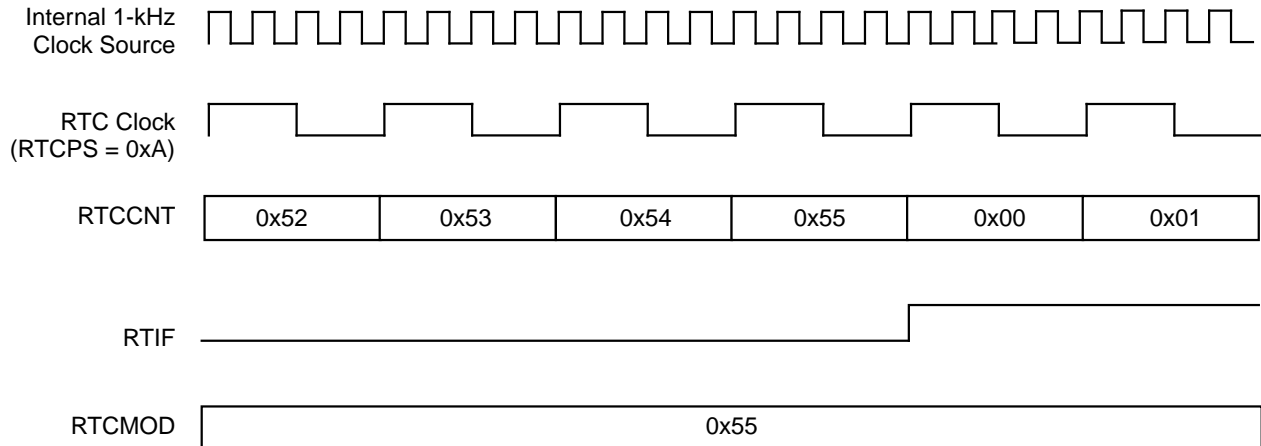
Figure 13-6. RTC Counter Overflow Example

In the example of Figure 13-6, the selected clock source is the 1-kHz internal oscillator clock source. The prescaler (RTCPS) is set to 0xA or divide-by-4. The modulo value in the RTCMOD register is set to 0x55. When the counter, RTCCNT, reaches the modulo value of 0x55, the counter overflows to 0x00 and continues counting. The real-time interrupt flag, RTIF, sets when the counter value changes from 0x55 to 0x00. A real-time interrupt is generated when RTIF is set, if RTIE is set.

13.5 Initialization/Application Information

This section provides example code to give some basic direction to a user on how to initialize and configure the RTC module. The example software is implemented in C language.

The example below shows how to implement time of day with the RTC using the 1-kHz clock source to achieve the lowest possible power consumption. Because the 1-kHz clock source is not as accurate as a crystal, software can be added for any adjustments. For accuracy without adjustments at the expense of additional power consumption, the external clock (ERCLK) or the internal clock (IRCLK) can be selected with appropriate prescaler and modulo values.

```
/* Initialize the elapsed time counters */
Seconds = 0;
Minutes = 0;
Hours = 0;
Days=0;

/* Configure RTC to interrupt every 1 second from 1-kHz clock source */
RTCMOD.byte = 0x00;
RTCSC.byte = 0x1F;


/**********************************************************************
Function Name : RTC_ISR
Notes : Interrupt service routine for RTC module.
**********************************************************************/
#pragma TRAP_PROC
void RTC_ISR(void)
{
        /* Clear the interrupt flag */
```

Table 16-8. TPM Clock Source Selection

CLKSB:CLKSA	TPM Clock Source to Prescaler Input
00	No clock selected (TPM counter disabled)
01	Bus rate clock
10	Fixed system clock
11	External source

The bus rate clock is the main system bus clock for the MCU. This clock source requires no synchronization because it is the clock that is used for all internal MCU activities including operation of the CPU and buses.

In MCUs that have no PLL and FLL or the PLL and FLL are not engaged, the fixed system clock source is the same as the bus-rate-clock source, and it does not go through a synchronizer. When a PLL or FLL is present and engaged, a synchronizer is required between the crystal divided-by two clock source and the timer counter so counter transitions will be properly aligned to bus-clock transitions. A synchronizer will be used at chip level to synchronize the crystal-related source clock to the bus clock.

The external clock source may be connected to any TPM channel pin. This clock source always has to pass through a synchronizer to assure that counter transitions are properly aligned to bus clock transitions. The bus-rate clock drives the synchronizer; therefore, to meet Nyquist criteria even with jitter, the frequency of the external clock source must not be faster than the bus rate divided-by four. With ideal clocks the external clock can be as fast as bus clock divided by four.

When the external clock source shares the TPM channel pin, this pin should not be used for other channel timing functions. For example, it would be ambiguous to configure channel 0 for input capture when the TPM channel 0 pin was also being used as the timer external clock source. (It is the user's responsibility to avoid such settings.) The TPM channel could still be used in output compare mode for software timing functions (pin controls set not to affect the TPM channel pin).

16.4.1.2   Counter Overflow and Modulo Reset

An interrupt flag and enable are associated with the 16-bit main counter. The flag (TOF) is a software-accessible indication that the timer counter has overflowed. The enable signal selects between software polling (TOIE=0) where no hardware interrupt is generated, or interrupt-driven operation (TOIE=1) where a static hardware interrupt is generated whenever the TOF flag is equal to one.

The conditions causing TOF to become set depend on whether the TPM is configured for center-aligned PWM (CPWMS=1). In the simplest mode, there is no modulus limit and the TPM is not in CPWMS=1 mode. In this case, the 16-bit timer counter counts from 0x0000 through 0xFFFF and overflows to 0x0000 on the next counting clock. TOF becomes set at the transition from 0xFFFF to 0x0000. When a modulus limit is set, TOF becomes set at the transition from the value set in the modulus register to 0x0000. When the TPM is in center-aligned PWM mode (CPWMS=1), the TOF flag gets set as the counter changes direction at the end of the count value set in the modulus register (that is, at the transition from the value set in the modulus register to the next lower count value). This corresponds to the end of a PWM period (the 0x0000 count value corresponds to the center of a period).

Table 17-2. BDCSCR Register Field Descriptions (continued)

Field	Description
2 WS	**Wait or Stop Status** — When the target CPU is in wait or stop mode, most BDC commands cannot function. However, the BACKGROUND command can be used to force the target CPU out of wait or stop and into active background mode where all BDC commands work. Whenever the host forces the target MCU into active background mode, the host should issue a READ_STATUS command to check that BDMACT = 1 before attempting other BDC commands. 0 Target CPU is running user application code or in active background mode (was not in wait or stop mode when background became active) 1 Target CPU is in wait or stop mode, or a BACKGROUND command was used to change from wait or stop to active background mode
1 WSF	**Wait or Stop Failure Status** — This status bit is set if a memory access command failed due to the target CPU executing a wait or stop instruction at or about the same time. The usual recovery strategy is to issue a BACKGROUND command to get out of wait or stop mode into active background mode, repeat the command that failed, then return to the user program. (Typically, the host would restore CPU registers and stack values and re-execute the wait or stop instruction.) 0 Memory access did not conflict with a wait or stop instruction 1 Memory access command failed because the CPU entered wait or stop mode
0 DVF	**Data Valid Failure Status** — This status bit is not used in the MC9S08SG32 Series because it does not have any slow access memory. 0 Memory access did not conflict with a slow memory access 1 Memory access command failed because CPU was not finished with a slow memory access

17.4.1.2   BDC Breakpoint Match Register (BDCBKPT)

This 16-bit register holds the address for the hardware breakpoint in the BDC. The BKPTEN and FTS control bits in BDCSCR are used to enable and configure the breakpoint logic. Dedicated serial BDC commands (READ_BKPT and WRITE_BKPT) are used to read and write the BDCBKPT register but is not accessible to user programs because it is not located in the normal memory map of the MCU. Breakpoints are normally set while the target MCU is in active background mode before running the user application program. For additional information about setup and use of the hardware breakpoint logic in the BDC, refer to Section 17.2.4, "BDC Hardware Breakpoint."

17.4.2   System Background Debug Force Reset Register (SBDFR)

This register contains a single write-only control bit. A serial background mode command such as WRITE_BYTE must be used to write to SBDFR. Attempts to write this register from a user program are ignored. Reads always return 0x00.

Appendix A
Electrical Characteristics

A.1 Introduction

This section contains electrical and timing specifications for the MC9S08SG32 Series of microcontrollers available at the time of publication. The MC9S08SG32 Series includes both:

- Standard (STD)— devices that are *standard-temperature* rated. Table rows marked with a ♦ indicate electrical characteristics that apply to these devices.
- AEC Grade 0 — devices that are *high-temperature* rated. Table rows marked with a ♦ indicate electrical characteristics that apply to AEC Grade 0 devices.

A.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table A-1. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved through the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE
The classification is shown in the column labeled "C" in the parameter tables where appropriate.

A.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table A-2 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

Table A-7. Supply Current Characteristics (continued)

#	C	Parameter	Symbol	V_{DD} (V)	Typ[1]	Max[2]	Unit	Temp Rated Standard	Temp Rated AEC Grade 0
		Stop2 mode supply current							
5	C	−40°C (C,M, and V suffix)	$S2I_{DD}$	5	0.94	–	µA	♦	—
	P	25°C (All parts)			1.25	–	µA	♦	—
	P[5]	85°C (C suffix only)			13.4	30	µA	♦	—
	P[5]	105°C (V suffix only)			30	65	µA	♦	—
	P[5]	125°C (M suffix only)			65	120	µA	♦	—
	C	−40°C (C,M, and V suffix)		3	0.83	–	µA	♦	—
	P	25°C (All parts)			1.1	–	µA	♦	—
	P[5]	85°C (C suffix only)			11.5	25	µA	♦	—
	P[5]	105°C (V suffix only)			25	55	µA	♦	—
	P[5]	125°C (M suffix only)			57	100	µA	♦	—
6	C	RTC adder to stop2 or stop3[6]	$S23I_{DDRTI}$	5	300	500	nA	♦	—
				3	300	500	nA	♦	—
7	C	LVD adder to stop3 (LVDE = LVDSE = 1)	$S3I_{DDLVD}$	5	110	180	µA	♦	—
				3	90	160	µA	♦	—
8	C	Adder to stop3 for oscillator enabled[7] (EREFSTEN =1)	$S3I_{DDOSC}$	5,3	5	8	µA	♦	—

[1] Typical values are based on characterization data at 25°C. See Figure A-5 through Figure A-7 for typical curves across temperature and voltage.

[2] Max values in this column apply for the full operating temperature range of the device unless otherwise noted.

[3] All modules except ADC active, ICS configured for FBELP, and does not include any dc loads on port pins

[4] All modules except ADC active, ICS configured for FEI, and does not include any dc loads on port pins

[5] Stop Currents are tested in production for 25 Con all parts. Tests at other temperatures depend upon the part number suffix and maturity of the product. Freescale may eliminate a test insertion at a particular temperature from the production test flow once sufficient data has been collected and is approved.

[6] Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.

[7] Values given under the following conditions: low range operation (RANGE = 0) with a 32.768kHz crystal and low power mode (HGO = 0).
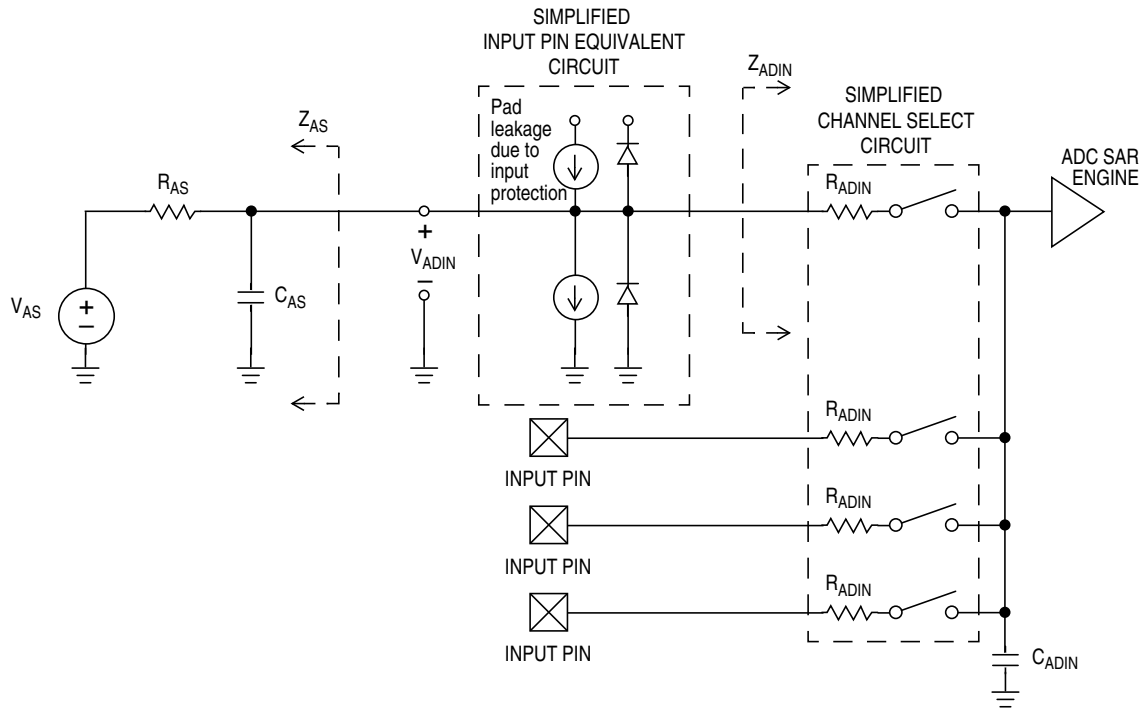
**Figure A-9. ADC Input Impedance Equivalency Diagram**

Table A-12. ADC Characteristics (continued)

#	Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Temp Rated Standard	Temp Rated AEC Grade 0	Comment
	Full-scale error	28-pin packages only									
		10-bit mode	T	E_{FS}	0	±0.5	±1	LSB^2	♦	♦	
		8-bit mode			0	±0.5	±0.5	LSB^2	♦	♦	
		20-pin packages									
		10-bit mode	T	E_{FS}	0	±1.0	±1.5	LSB^2	♦	—	
		8-bit mode			0	±0.5	±0.5	LSB^2	♦	—	
		16-pin packages									
		10-bit mode	T	E_{FS}	0	±1.0	±1.5	LSB^2	♦	♦	
		8-bit mode			0	±0.5	±0.5	LSB^2	♦	♦	
	Quantization error	10-bit mode	D	E_Q	—	—	±0.5	LSB^2	♦	♦	
		8-bit mode			—	—	±0.5	LSB^2	♦	♦	
	Input leakage error	10-bit mode	D	E_{IL}	0	±0.2	±2.5	LSB^2	♦	♦	Pad leakage[3] * R_{AS}
		8-bit mode			0	±0.1	±1	LSB^2	♦	♦	
	Temp sensor slope	-40°C to 25°C	D	m	—	3.266	—	mV/°C	♦	♦	
		25°C to 125°C			—	3.638	—	mV/°C	♦	♦	
	Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.396	—	V	♦	♦	

[1] Typical values assume V_{DD} = 5.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

[3] Based on input pad leakage current. Refer to pad electricals.
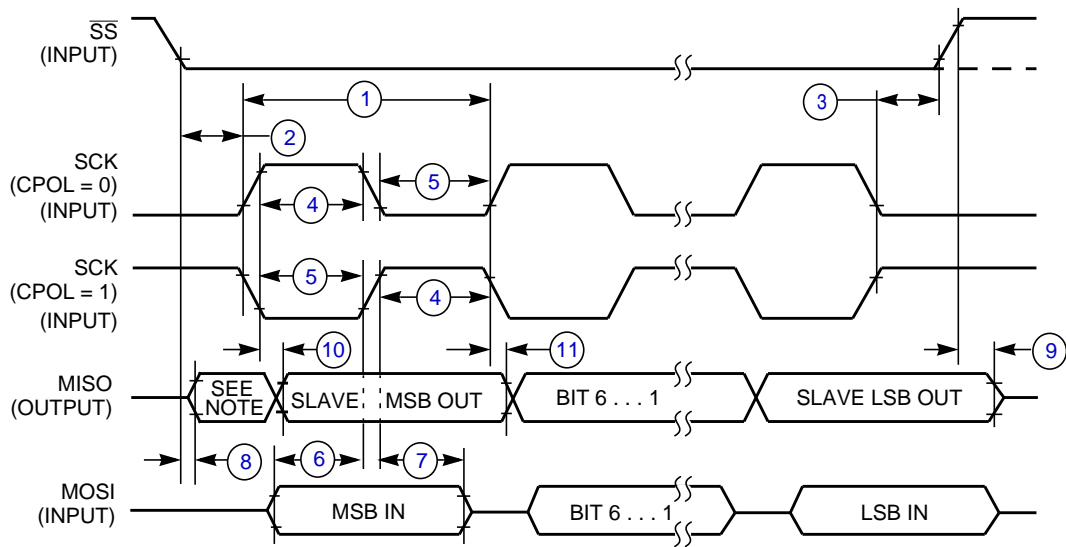
NOTE:
1. Not defined but normally LSB of character just received

Figure A-17. SPI Slave Timing (CPHA = 1)

The following pages are mechanical specifications for MC9S08SG32 Series package options. See Table B-2 for the document number for each package type.

Table B-2. Package Information

Pin Count	Type	Designator	Document No.
28	TSSOP	TL	98ARS23923W
20	TSSOP	TJ	98ASH70169A
16	TSSOP	TG	98ASH70247A