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#### Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I <sup>2</sup> C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08sg32e1ctlr">https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08sg32e1ctlr</a>

# **Addendum to Rev. 8.1 of the MC9S08SG32 Covers: MC9S08SG32 and MC9S08SG16**

This addendum identifies changes to Rev. 8.1 of the MC9S08SG32 data sheet (covering MC9S08SG32 and MC9S08SG16). The changes described in this addendum have not been implemented in the specified pages.

## **1 Update to the “Nonvolatile Register Summary” table for NVFTRIM and NVOPT**

<b>Location:</b>	<a href="#">Table 4-4. Nonvolatile Register Summary, Page 47</a>
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For the NVFTRIM and NVOPT registers in Table 4-4, “Nonvolatile Register Summary,” all reserved bits should be marked as “—” (not “0”).

## **2 Update to the “Instruction Set Summary” table for BRA and BRN**

<b>Location:</b>	<a href="#">Table 7-2. Instruction Set Summary (Sheet 3 of 9), Page 106</a>
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In Table 7-2, “Instruction Set Summary,” remove “(if I = 1)” from the BRA instruction and remove “(if I = 0)” from the BRN instruction. The BRA and BRN instructions do not depend on the I bit.

# MC9S08SG32 DataSheet Addendum

by: Microcontroller Solutions Group

This is the MC9S08SG32 DataSheet set consisting of the following files:

- MC9S08SG32 DataSheet Addendum, Rev 1
- MC9S08SG32 DataSheet, Rev 8

# MC9S08SG32 Series Features

## 8-Bit HCS08 Central Processor Unit (CPU)

- 40-MHz HCS08 CPU (central processor unit)
- 36-MHz HCS08 CPU for temperatures greater than 125 °C
- HC08 instruction set with added BGND instruction
- Support for up to 32 interrupt/reset sources

## On-Chip Memory

- FLASH read/program/erase over full operating voltage and temperature from -40 up to 150 °C
- Random-access memory (RAM)
- Security circuitry to prevent unauthorized access to RAM and FLASH contents

## Power-Saving Modes

- Two very low power stop modes
- Reduced power wait mode
- Very low power real time counter for use in run, wait, and stop

## Clock Source Options

- Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
- Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and:
  - 1.5% deviation over temperature -40 to 125 °C
  - 3% deviation for temperature > 125 °C
- ICS supports bus frequencies from 2 MHz to 20 MHz

## System Protection

- Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points
- Illegal opcode detection with reset
- Illegal address detection with reset
- FLASH block protect

## Development Support

- Single-wire background debug interface
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- On-chip, in-circuit emulation (ICE) debug module containing two comparators and 9 trigger modes. Eight-deep FIFO for storing change-of-flow

address and event-only data. Debug module supports both tag and force breakpoints

## Peripherals

- **ADC** — 16-channel, 10-bit resolution, 2.5 μs conversion time, automatic compare function, temperature sensor, internal bandgap reference channel; runs in stop3
- **ACMP** — Analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; output can be optionally routed to TPM module; runs in stop3
- **SCI** — Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake up on active edge
- **SPI** — Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
- **IIC** — Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10-bit addressing
- **MTIM** — 8-bit modulo counter with 8-bit prescaler and overflow interrupt
- **TPMx** — Two 2-channel timer pwm modules (TPM1, TPM2); Selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
- **RTC** — (Real-time counter) 8-bit modulus counter with binary or decimal based prescaler; External clock source for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components, runs in all MCU modes

## Input/Output

- 22 general purpose I/O pins (GPIOs)
- 8 interrupt pins with selectable polarity
- Ganged output option for PTB[5:2] and PTC[3:0]; allows single write to change state of multiple pins
- Hysteresis and configurable pull up device on all input pins; Configurable slew rate and drive strength on all output pins

## Package Options

- 28-TSSOP, 20-TSSOP, 16-TSSOP (20-pin package options not available on high-temperature rated devices).

Table 3-1 shows all of the control bits that affect stop mode selection and the mode selected under various conditions. The selected mode is entered following the execution of a STOP instruction.

**Table 3-1. Stop Mode Selection**

STOPE	ENBDM <sup>1</sup>	LVDE	LVDSE	PPDC	Stop Mode
0	x	x	x	x	Stop modes disabled; illegal opcode reset if STOP instruction executed
1	1	x	x	x	Stop3 with BDM enabled <sup>2</sup>
1	0	Both bits must be 1	x	x	Stop3 with voltage regulator active
1	0	Either bit a 0	0	0	Stop3
1	0	Either bit a 0	1	1	Stop2

<sup>1</sup> ENBDM is located in the BDCSCR, which is only accessible through BDC commands, see [Section 17.4.1.1, “BDC Status and Control Register \(BDCSCR\)”](#).

<sup>2</sup> When in Stop3 mode with BDM enabled, The S<sub>IDD</sub> will be near R<sub>IDD</sub> levels because internal clocks are enabled.

### 3.6.1 Stop3 Mode

Stop3 mode is entered by executing a STOP instruction under the conditions as shown in [Table 3-1](#). The states of all of the internal registers and logic, RAM contents, and I/O pin states are maintained.

Stop3 can be exited by asserting  $\overline{\text{RESET}}$ , or by an interrupt from one of the following sources: the real-time counter (RTC), LVD system, ACMP, ADC, SCI or any pin interrupts.

If stop3 is exited by means of the  $\overline{\text{RESET}}$  pin, then the MCU is reset and operation will resume after taking the reset vector. Exit by means of one of the internal interrupt sources results in the MCU taking the appropriate interrupt vector.

#### 3.6.1.1 LVD Enabled in Stop3 Mode

The LVD system is capable of generating either an interrupt or a reset when the supply voltage drops below the LVD voltage. For configuring the LVD system for interrupt or reset, refer to [Section 5.6, “Low-Voltage Detect \(LVD\) System”](#). If the LVD is enabled in stop (LVDE and LVDSE bits in SPMSC1 both set) at the time the CPU executes a STOP instruction, then the voltage regulator remains active during stop mode.

For the ADC to operate in stop mode, the LVD must be enabled when entering stop3.

For the ACMP to operate in stop mode with compare to internal bandgap option, the LVD must be enabled when entering stop3.

#### 3.6.1.2 Active BDM Enabled in Stop3 Mode

Entry into the active background mode from run mode is enabled if ENBDM in BDCSCR is set. This register is described in [Chapter 17, “Development Support.”](#) If ENBDM is set when the CPU executes a STOP instruction, the system clocks to the background debug logic remain active when the MCU enters stop mode. Because of this, background debug communication remains possible. In addition, the voltage regulator does not enter its low-power standby state but maintains full internal regulation.

# Chapter 4

## Memory

### 4.1 MC9S08SG32 Series Memory Map

As shown in [Figure 4-1](#), on-chip memory in the MC9S08SG32 Series series of MCUs consists of RAM, FLASH program memory for nonvolatile data storage, and I/O and control/status registers. The registers are divided into three groups:

- Direct-page registers (0x0000 through 0x007F)
- High-page registers (0x1800 through 0x185F)
- Nonvolatile registers (0xFFB0 through 0xFFBF)

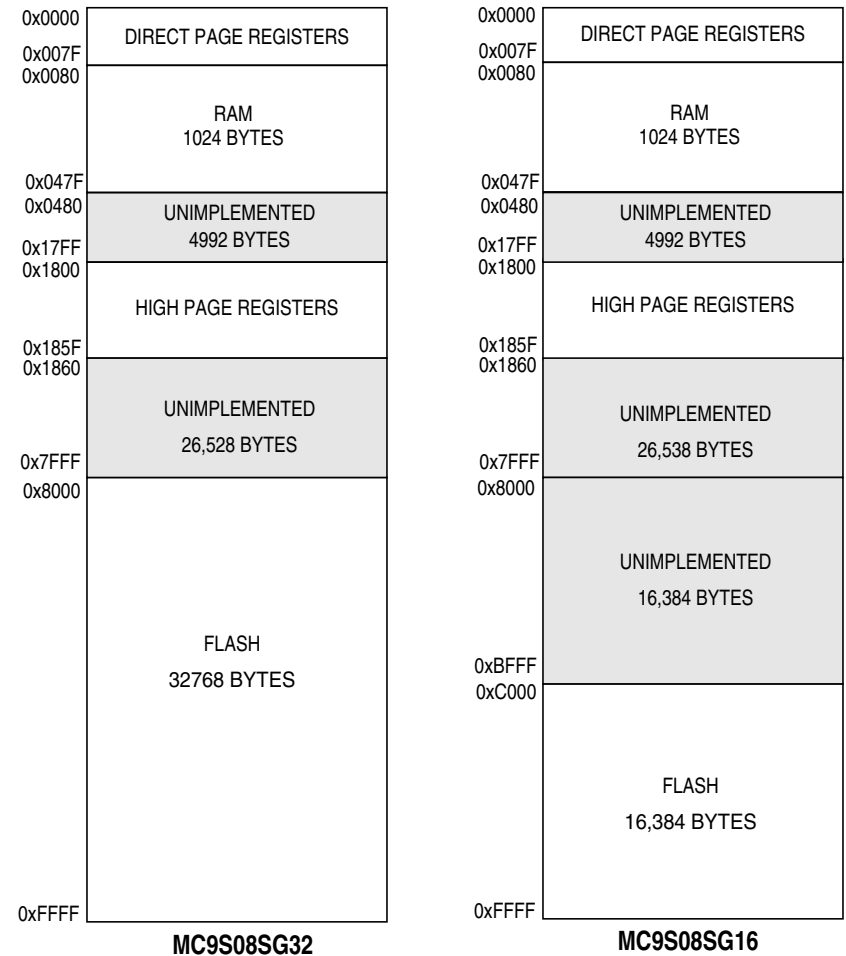


Figure 4-1. MC9S08SG32/MC9S08SG16 Memory Map

Table 4-2. Direct-Page Register Summary (Sheet 3 of 3)

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
0x0066	TPM2C0VH	Bit 15	14	13	12	11	10	9	Bit 8
0x0067	TPM2C0VL	Bit 7	6	5	4	3	2	1	Bit 0
0x0068	TPM2C1SC	CH1F	CH1IE	MS1B	MS1A	ELS1B	ELS1A	0	0
0x0069	TPM2C1VH	Bit 15	14	13	12	11	10	9	Bit 8
0x006A	TPM2C1VL	Bit 7	6	5	4	3	2	1	Bit 0
0x006B	Reserved	—	—	—	—	—	—	—	—
0x006C	RTCSC	RTIF	RTCLKS		RTIE	RTCPS			
0x006D	RTCCNT	RTCCNT							
0x006E	RTCMOD	RTCMOD							
0x006F - 0x007F	Reserved	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—

### 7.4.5 BGND Instruction

The BGND instruction is new to the HCS08 compared to the M68HC08. BGND would not be used in normal user programs because it forces the CPU to stop processing user instructions and enter the active background mode. The only way to resume execution of the user program is through reset or by a host debug system issuing a GO, TRACE1, or TAGGO serial command through the background debug interface.

Software-based breakpoints can be set by replacing an opcode at the desired breakpoint address with the BGND opcode. When the program reaches this breakpoint address, the CPU is forced to active background mode rather than continuing the user program.



## 10.4.2 10-bit Address

For 10-bit addressing, 0x11110 is used for the first 5 bits of the first address byte. Various combinations of read/write formats are possible within a transfer that includes 10-bit addressing.

### 10.4.2.1 Master-Transmitter Addresses a Slave-Receiver

The transfer direction is not changed (see Table 10-10). When a 10-bit address follows a start condition, each slave compares the first seven bits of the first byte of the slave address (11110XX) with its own address and tests whether the eighth bit ( $R/\overline{W}$  direction bit) is 0. More than one device can find a match and generate an acknowledge (A1). Then, each slave that finds a match compares the eight bits of the second byte of the slave address with its own address. Only one slave finds a match and generates an acknowledge (A2). The matching slave remains addressed by the master until it receives a stop condition (P) or a repeated start condition (Sr) followed by a different slave address.

S	Slave Address 1st 7 bits 11110 + AD10 + AD9	R/W 0	A1	Slave Address 2nd byte AD[8:1]	A2	Data	A	...	Data	A/A	P
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**Table 10-10. Master-Transmitter Addresses Slave-Receiver with a 10-bit Address**

After the master-transmitter has sent the first byte of the 10-bit address, the slave-receiver sees an IIC interrupt. Software must ensure the contents of IICD are ignored and not treated as valid data for this interrupt.

### 10.4.2.2 Master-Receiver Addresses a Slave-Transmitter

The transfer direction is changed after the second  $R/\overline{W}$  bit (see Table 10-11). Up to and including acknowledge bit A2, the procedure is the same as that described for a master-transmitter addressing a slave-receiver. After the repeated start condition (Sr), a matching slave remembers that it was addressed before. This slave then checks whether the first seven bits of the first byte of the slave address following Sr are the same as they were after the start condition (S) and tests whether the eighth ( $R/\overline{W}$ ) bit is 1. If there is a match, the slave considers that it has been addressed as a transmitter and generates acknowledge A3. The slave-transmitter remains addressed until it receives a stop condition (P) or a repeated start condition (Sr) followed by a different slave address.

After a repeated start condition (Sr), all other slave devices also compare the first seven bits of the first byte of the slave address with their own addresses and test the eighth ( $R/\overline{W}$ ) bit. However, none of them are addressed because  $R/\overline{W} = 1$  (for 10-bit devices) or the 11110XX slave address (for 7-bit devices) does not match.

S	Slave Address 1st 7 bits 11110 + AD10 + AD9	R/W 0	A1	Slave Address 2nd byte AD[8:1]	A2	Sr	Slave Address 1st 7 bits 11110 + AD10 + AD9	R/W 1	A3	Data	A	...	Data	A	P
---	--	----------	----	-----------------------------------	----	----	--	----------	----	------	---	-----	------	---	---

**Table 10-11. Master-Receiver Addresses a Slave-Transmitter with a 10-bit Address**

After the master-receiver has sent the first byte of the 10-bit address, the slave-transmitter sees an IIC interrupt. Software must ensure the contents of IICD are ignored and not treated as valid data for this interrupt.

## Chapter 11

# Internal Clock Source (S08ICSV2)

### 11.1 Introduction

The internal clock source (ICS) module provides clock source choices for the MCU. The module contains a frequency-locked loop (FLL) as a clock source that is controllable by either an internal or an external reference clock. The module can provide this FLL clock or either of the internal or external reference clocks as a source for the MCU system clock. There are also signals provided to control a low power oscillator (XOSC) module to allow the use of an external crystal/resonator as the external reference clock.

Whichever clock source is chosen, it is passed through a reduced bus divider (BDIV) which allows a lower final output clock frequency to be derived.

The bus frequency will be one-half of the ICSOUT frequency. After reset, the ICS is configured for FEI mode and BDIV is reset to 0:1 to introduce an extra divide-by-two before ICSOUT so the bus frequency is  $f_{dco}/4$ . At POR, the TRIM and FTRIM settings are reset to 0x80 and 0 respectively so the dco frequency is  $f_{dco\_ut}$ . For other resets, the trim settings keep the value that was present before the reset.

#### NOTE

Refer to [Section 1.3, “System Clock Distribution](#) for a detailed view of the distribution of clock sources throughout the MCU.

#### 11.1.1 Module Configuration

When the internal reference is enabled in stop mode (IREFSTEN = 1), the voltage regulator must also be enabled in stop mode by setting the LVDE and LVDSE bits in the SPMSC1 register.

[Figure 11-1](#) shows the MC9S08SG32 block diagram with the ICS highlighted.

- CLKS bits are written to 00
- IREFS bit is written to 1
- RDIV bits are written to divide trimmed reference clock to be within the range of 31.25 kHz to 39.0625 kHz.

In FLL engaged internal mode, the ICSOUT clock is derived from the FLL clock, which is controlled by the internal reference clock. The FLL loop will lock the frequency to 1024 times the reference frequency, as selected by the RDIV bits. The ICSLCLK is available for BDC communications, and the internal reference clock is enabled.

#### 11.4.1.2 FLL Engaged External (FEE)

The FLL engaged external (FEE) mode is entered when all the following conditions occur:

- CLKS bits are written to 00
- IREFS bit is written to 0
- RDIV bits are written to divide reference clock to be within the range of 31.25 kHz to 39.0625 kHz

In FLL engaged external mode, the ICSOUT clock is derived from the FLL clock which is controlled by the external reference clock. The FLL loop will lock the frequency to 1024 times the reference frequency, as selected by the RDIV bits. The ICSLCLK is available for BDC communications, and the external reference clock is enabled.

#### 11.4.1.3 FLL Bypassed Internal (FBI)

The FLL bypassed internal (FBI) mode is entered when all the following conditions occur:

- CLKS bits are written to 01
- IREFS bit is written to 1.
- BDM mode is active or LP bit is written to 0

In FLL bypassed internal mode, the ICSOUT clock is derived from the internal reference clock. The FLL clock is controlled by the internal reference clock, and the FLL loop will lock the FLL frequency to 1024 times the reference frequency, as selected by the RDIV bits. The ICSLCLK will be available for BDC communications, and the internal reference clock is enabled.

#### 11.4.1.4 FLL Bypassed Internal Low Power (FBILP)

The FLL bypassed internal low power (FBILP) mode is entered when all the following conditions occur:

- CLKS bits are written to 01
- IREFS bit is written to 1.
- BDM mode is not active and LP bit is written to 1

In FLL bypassed internal low power mode, the ICSOUT clock is derived from the internal reference clock and the FLL is disabled. The ICSLCLK will be not be available for BDC communications, and the internal reference clock is enabled.

## 12.1.2 Features

Timer system features include:

- 8-bit up-counter
  - Free-running or 8-bit modulo limit
  - Software controllable interrupt on overflow
  - Counter reset bit (TRST)
  - Counter stop bit (TSTP)
- Four software selectable clock sources for input to prescaler:
  - System bus clock — rising edge
  - Fixed frequency clock (XCLK) — rising edge
  - External clock source on the TCLK pin — rising edge
  - External clock source on the TCLK pin — falling edge
- Nine selectable clock prescale values:
  - Clock source divide by 1, 2, 4, 8, 16, 32, 64, 128, or 256

## 12.1.3 Modes of Operation

This section defines the MTIM's operation in stop, wait and background debug modes.

### 12.1.3.1 MTIM in Wait Mode

The MTIM continues to run in wait mode if enabled before executing the WAIT instruction. Therefore, the MTIM can be used to bring the MCU out of wait mode if the timer overflow interrupt is enabled. For lowest possible current consumption, the MTIM should be stopped by software if not needed as an interrupt source during wait mode.

### 12.1.3.2 MTIM in Stop Modes

The MTIM is disabled in all stop modes, regardless of the settings before executing the STOP instruction. Therefore, the MTIM cannot be used as a wake up source from stop modes.

Waking from stop2 mode, the MTIM will be put into its reset state. If stop3 is exited with a reset, the MTIM will be put into its reset state. If stop3 is exited with an interrupt, the MTIM continues from the state it was in when stop3 was entered. If the counter was active upon entering stop3, the count will resume from the current value.

### 12.1.3.3 MTIM in Active Background Mode

The MTIM suspends all counting until the microcontroller returns to normal user operating mode. Counting resumes from the suspended value as long as an MTIM reset did not occur (TRST written to a 1 or MTIMMOD written).

### 13.3.1 RTC Status and Control Register (RTCSC)

RTCSC contains the real-time interrupt status flag (RTIF), the clock select bits (RTCLKS), the real-time interrupt enable bit (RTIE), and the prescaler select bits (RTCPS).

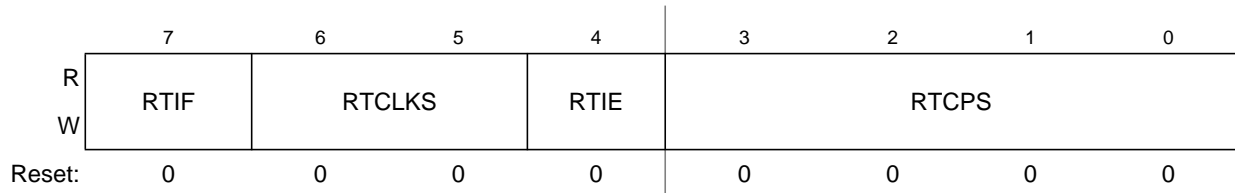


Figure 13-3. RTC Status and Control Register (RTCSC)

Table 13-2. RTCSC Field Descriptions

Field	Description
7 RTIF	Real-Time Interrupt Flag This status bit indicates the RTC counter register reached the value in the RTC modulo register. Writing a logic 0 has no effect. Writing a logic 1 clears the bit and the real-time interrupt request. Reset clears RTIF. 0 RTC counter has not reached the value in the RTC modulo register. 1 RTC counter has reached the value in the RTC modulo register.
6–5 RTCLKS	Real-Time Clock Source Select. These two read/write bits select the clock source input to the RTC prescaler. Changing the clock source clears the prescaler and RTCCNT counters. When selecting a clock source, ensure that the clock source is properly enabled (if applicable) to ensure correct operation of the RTC. Reset clears RTCLKS. 00 Real-time clock source is the 1-kHz low power oscillator (LPO) 01 Real-time clock source is the external clock (ERCLK) 1x Real-time clock source is the internal clock (IRCLK)
4 RTIE	Real-Time Interrupt Enable. This read/write bit enables real-time interrupts. If RTIE is set, then an interrupt is generated when RTIF is set. Reset clears RTIE. 0 Real-time interrupt requests are disabled. Use software polling. 1 Real-time interrupt requests are enabled.
3–0 RTCPS	Real-Time Clock Prescaler Select. These four read/write bits select binary-based or decimal-based divide-by values for the clock source. See <a href="#">Table 13-3</a> . Changing the prescaler value clears the prescaler and RTCCNT counters. Reset clears RTCPS.

Table 13-3. RTC Prescaler Divide-by values

RTCLKS[0]	RTCPS															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Off	2 <sup>3</sup>	2 <sup>5</sup>	2 <sup>6</sup>	2 <sup>7</sup>	2 <sup>8</sup>	2 <sup>9</sup>	2 <sup>10</sup>	1	2	2 <sup>2</sup>	10	2 <sup>4</sup>	10 <sup>2</sup>	5x10 <sup>2</sup>	10 <sup>3</sup>
1	Off	2 <sup>10</sup>	2 <sup>11</sup>	2 <sup>12</sup>	2 <sup>13</sup>	2 <sup>14</sup>	2 <sup>15</sup>	2 <sup>16</sup>	10 <sup>3</sup>	2x10 <sup>3</sup>	5x10 <sup>3</sup>	10 <sup>4</sup>	2x10 <sup>4</sup>	5x10 <sup>4</sup>	10 <sup>5</sup>	2x10 <sup>5</sup>



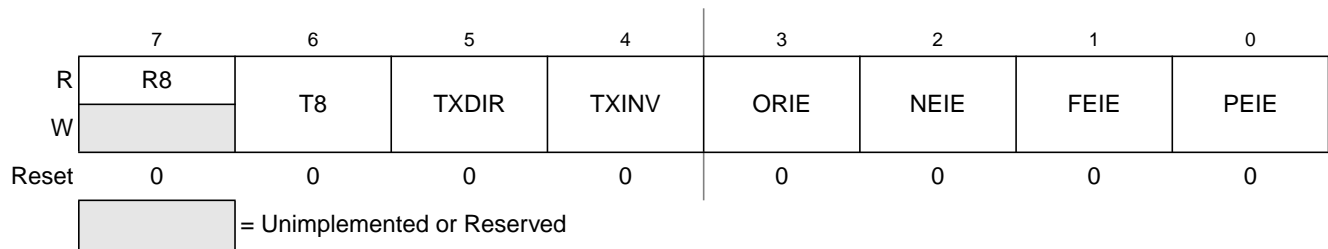
**Table 14-6. SCIS2 Field Descriptions (continued)**

Field	Description
1 LBKDE	<b>LIN Break Detection Enable</b> — LBKDE is used to select a longer break character detection length. While LBKDE is set, framing error (FE) and receive data register full (RDRF) flags are prevented from setting. 0 Break character is detected at length of 10 bit times (11 if M = 1). 1 Break character is detected at length of 11 bit times (12 if M = 1).
0 RAF	<b>Receiver Active Flag</b> — RAF is set when the SCI receiver detects the beginning of a valid start bit, and RAF is cleared automatically when the receiver detects an idle line. This status flag can be used to check whether an SCI character is being received before instructing the MCU to go to stop mode. 0 SCI receiver idle waiting for a start bit. 1 SCI receiver active (RxD input not idle).

<sup>1</sup> Setting RXINV inverts the RxD input for all cases: data bits, start and stop bits, break, and idle.

When using an internal oscillator in a LIN system, it is necessary to raise the break detection threshold by one bit time. Under the worst case timing conditions allowed in LIN, it is possible that a 0x00 data character can appear to be 10.26 bit times long at a slave which is running 14% faster than the master. This would trigger normal break detection circuitry which is designed to detect a 10 bit break symbol. When the LBKDE bit is set, framing errors are inhibited and the break detection threshold changes from 10 bits to 11 bits, preventing false detection of a 0x00 data character as a LIN break symbol.

## 14.2.6 SCI Control Register 3 (SCIC3)



**Figure 14-10. SCI Control Register 3 (SCIC3)**

**Table 14-7. SCIC3 Field Descriptions**

Field	Description
7 R8	<b>Ninth Data Bit for Receiver</b> — When the SCI is configured for 9-bit data (M = 1), R8 can be thought of as a ninth receive data bit to the left of the MSB of the buffered data in the SCID register. When reading 9-bit data, read R8 before reading SCID because reading SCID completes automatic flag clearing sequences which could allow R8 and SCID to be overwritten with new data.
6 T8	<b>Ninth Data Bit for Transmitter</b> — When the SCI is configured for 9-bit data (M = 1), T8 may be thought of as a ninth transmit data bit to the left of the MSB of the data in the SCID register. When writing 9-bit data, the entire 9-bit value is transferred to the SCI shift register after SCID is written so T8 should be written (if it needs to change from its previous value) before SCID is written. If T8 does not need to change in the new value (such as when it is used to generate mark or space parity), it need not be written each time SCID is written.
5 TXDIR	<b>TxD Pin Direction in Single-Wire Mode</b> — When the SCI is configured for single-wire half-duplex operation (LOOPS = RSRC = 1), this bit determines the direction of data at the TxD pin. 0 TxD pin is an input in single-wire mode. 1 TxD pin is an output in single-wire mode.

## 15.5.2 SPI Interrupts

There are three flag bits, two interrupt mask bits, and one interrupt vector associated with the SPI system. The SPI interrupt enable mask (SPIE) enables interrupts from the SPI receiver full flag (SPRF) and mode fault flag (MODF). The SPI transmit interrupt enable mask (SPTIE) enables interrupts from the SPI transmit buffer empty flag (SPTEF). When one of the flag bits is set, and the associated interrupt mask bit is set, a hardware interrupt request is sent to the CPU. If the interrupt mask bits are cleared, software can poll the associated flag bits instead of using interrupts. The SPI interrupt service routine (ISR) should check the flag bits to determine what event caused the interrupt. The service routine should also clear the flag bit(s) before returning from the ISR (usually near the beginning of the ISR).

## 15.5.3 Mode Fault Detection

A mode fault occurs and the mode fault flag (MODF) becomes set when a master SPI device detects an error on the  $\overline{SS}$  pin (provided the  $\overline{SS}$  pin is configured as the mode fault input signal). The  $\overline{SS}$  pin is configured to be the mode fault input signal when  $MSTR = 1$ , mode fault enable is set ( $MODFEN = 1$ ), and slave select output enable is clear ( $SSOE = 0$ ).

The mode fault detection feature can be used in a system where more than one SPI device might become a master at the same time. The error is detected when a master's  $\overline{SS}$  pin is low, indicating that some other SPI device is trying to address this master as if it were a slave. This could indicate a harmful output driver conflict, so the mode fault logic is designed to disable all SPI output drivers when such an error is detected.

When a mode fault is detected, MODF is set and MSTR is cleared to change the SPI configuration back to slave mode. The output drivers on the SPSCCK, MOSI, and MISO (if not bidirectional mode) are disabled.

MODF is cleared by reading it while it is set, then writing to the SPI control register 1 (SPIC1). User software should verify the error condition has been corrected before changing the SPI back to master mode.



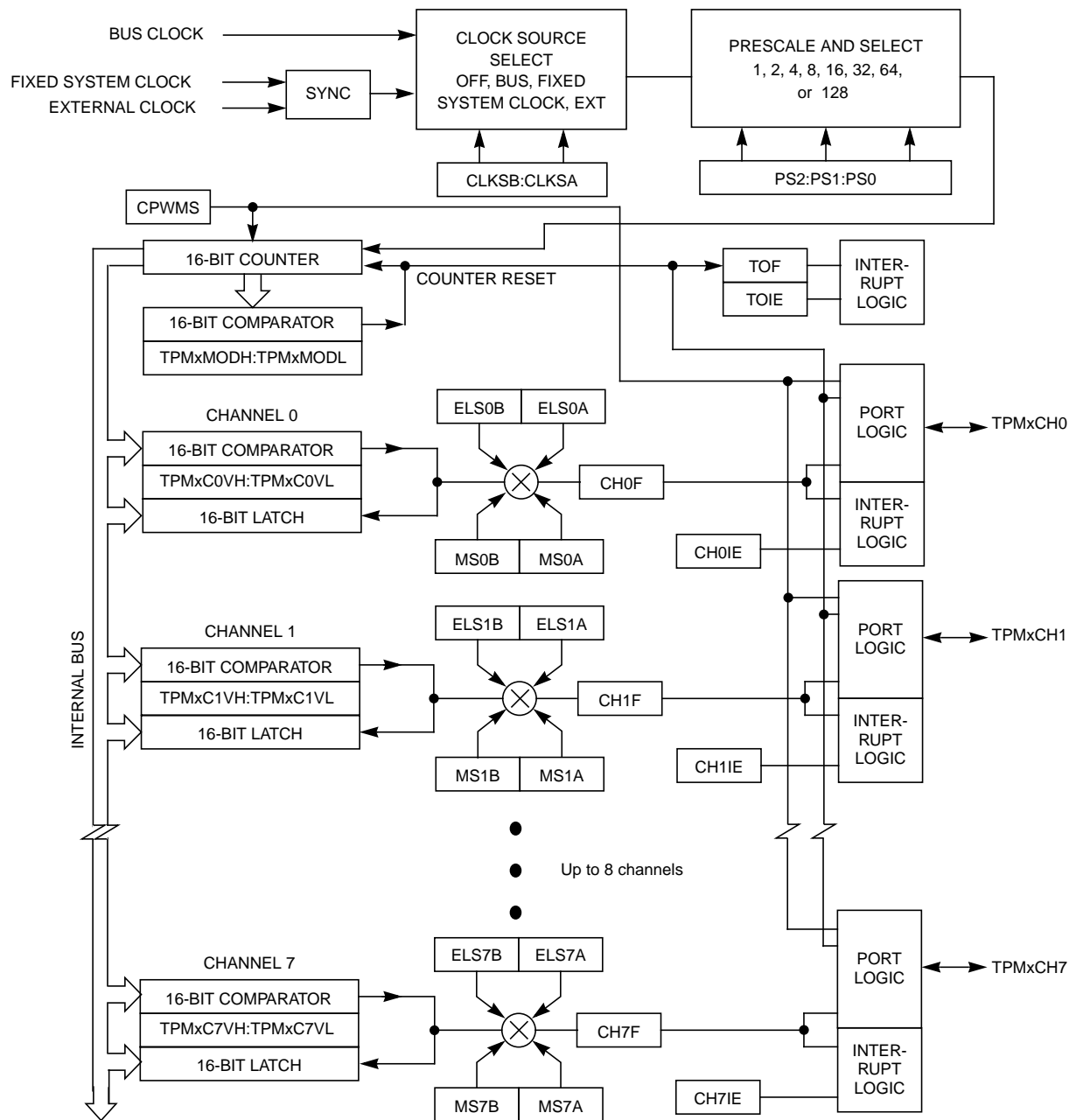


Figure 16-2. TPM Block Diagram

Figure 17-2 shows an external host transmitting a logic 1 or 0 to the BKGD pin of a target HCS08 MCU. The host is asynchronous to the target so there is a 0-to-1 cycle delay from the host-generated falling edge to where the target perceives the beginning of the bit time. Ten target BDC clock cycles later, the target senses the bit level on the BKGD pin. Typically, the host actively drives the pseudo-open-drain BKGD pin during host-to-target transmissions to speed up rising edges. Because the target does not drive the BKGD pin during the host-to-target transmission period, there is no need to treat the line as an open-drain signal during this period.

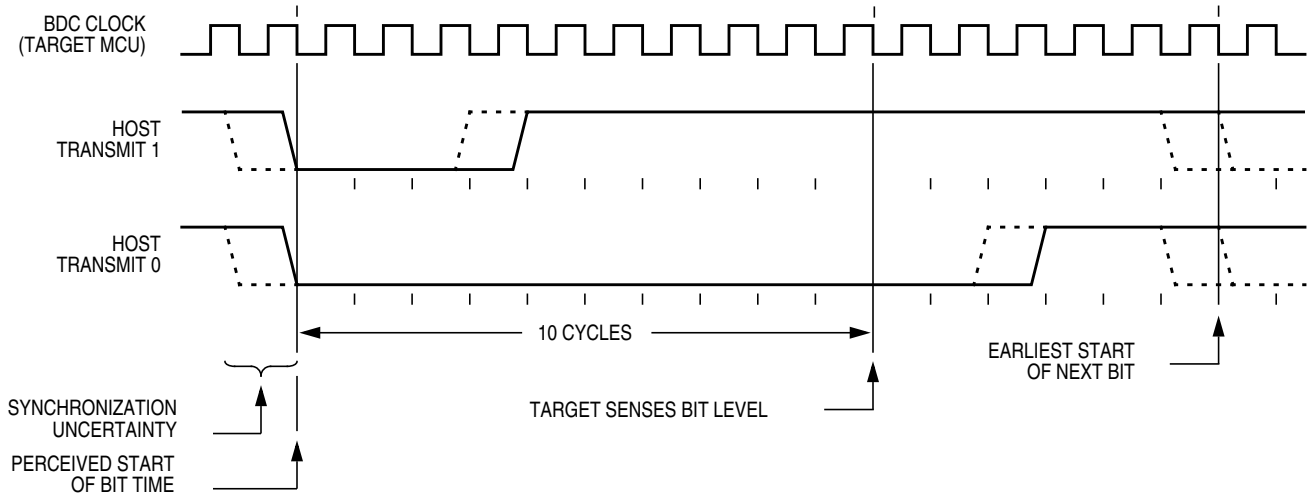


Figure 17-2. BDC Host-to-Target Serial Bit Timing

## A.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

**Table A-7. Supply Current Characteristics**

#	C	Parameter	Symbol	V <sub>DD</sub> (V)	Typ <sup>1</sup>	Max <sup>2</sup>	Unit	Temp Rated	
								Standard	AEC Grade 0
1	C	Run supply current <sup>3</sup> measured at (CPU clock = 4 MHz, f <sub>BUS</sub> = 2 MHz)	R <sub>I</sub> DD	5	1.4	3	mA	◆	◆
	C			3	1.3	2.5	mA	◆	◆
2	P	Run supply current <sup>3</sup> measured at (CPU clock = 16 MHz, f <sub>BUS</sub> = 8 MHz)	R <sub>I</sub> DD	5	4.7	7.5	mA	◆	◆
	C			3	4.6	7	mA	◆	◆
3	C	Run supply current <sup>4</sup> measured at (CPU clock = 32 MHz, f <sub>BUS</sub> = 16MHz)	R <sub>I</sub> DD	5	8.9	10	mA	◆	◆
	C			3	8.7	9.6	mA	◆	◆
4	Stop3 mode supply current								
	C	−40°C (C,V, and M suffix)  25°C (All parts)  85°C (C suffix only)  105°C (V suffix only)  125°C (M suffix only)	S3I <sub>DD</sub>	5	0.96	–	μA	◆	—
	P				1.3	–	μA	◆	—
	P <sup>5</sup>				16.9	35	μA	◆	—
	P <sup>5</sup>				37	90	μA	◆	—
	P <sup>5</sup>				84	150	μA	◆	—
	C	−40°C (C,V, and M suffix)  25°C (All parts)  85°C (C suffix only)  105°C (V suffix only)  125°C (M suffix only)		3	0.85	–	μA	◆	—
	P				1.2	–	μA	◆	—
	P <sup>5</sup>				14.8	30	μA	◆	—
	P <sup>5</sup>				32.7	80	μA	◆	—
	P <sup>5</sup>				75	130	μA	◆	—

Table A-12. ADC Characteristics

#	Characteristic	Conditions	C	Symb	Min	Typ <sup>1</sup>	Max	Unit	Temp Rated		Comment
									Standard	AEC Grade 0	
1	Supply current	ADLPC=1 ADLSMP=1 ADCO=1	T	$I_{DD} + I_{DDAD}$	—	133	—	μA	◆	◆	ADC current only
		ADLPC=1 ADLSMP=0 ADCO=1	T	$I_{DD} + I_{DDAD}$	—	218	—	μA	◆	◆	ADC current only
		ADLPC=0 ADLSMP=1 ADCO=1	T	$I_{DD} + I_{DDAD}$	—	327	—	μA	◆	◆	ADC current only
		ADLPC=0 ADLSMP=0 ADCO=1	P	$I_{DD} + I_{DDAD}$	—	0.58 2	1	mA	◆	◆	ADC current only
2	ADC asynchronous clock source	High speed (ADLPC=0)	P	$f_{ADACK}$	2	3.3	5	MHz	◆	◆	$t_{ADACK} = 1/f_{ADACK}$
		Low power (ADLPC=1)			1.25	2	3.3		◆	◆	
3	Conversion time (including sample time)	Short sample (ADLSMP=0)	D	$t_{ADC}$	—	20	—	ADCK cycles	◆	◆	See ADC Chapter for conversion time variances
		Long sample (ADLSMP=1)			—	40	—		◆	◆	
4	Sample time	Short sample (ADLSMP=0)	D	$t_{ADS}$	—	3.5	—	ADCK cycles	◆	◆	
		Long sample (ADLSMP=1)			—	23.5	—		◆	◆	

## B.1.1 Device Numbering Scheme

This device uses a smart numbering system. Refer to the following diagram to understand what each element of the device number represents.

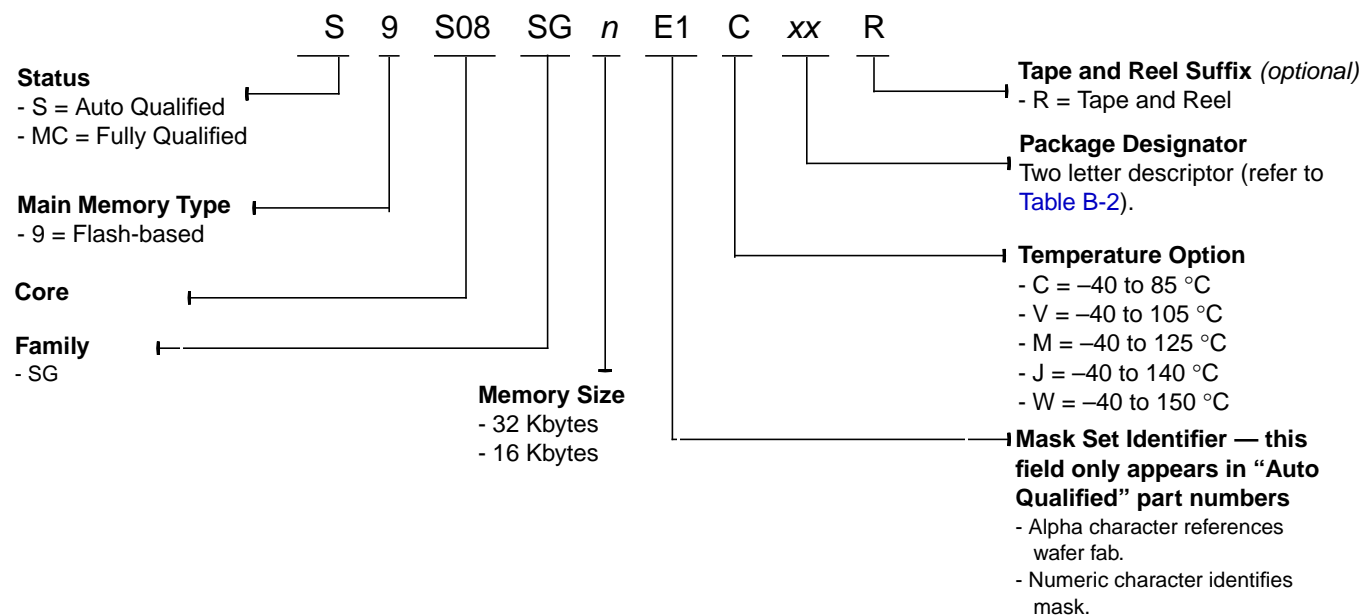


Figure B-1. MC9S08SG32 Device Numbering Scheme

## B.2 Package Information and Mechanical Drawings

Table B-2 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08SG32 Series Product Summary pages at <http://www.freescale.com>.

To view the latest drawing, either:

- Click on the appropriate link in Table B-2, or
- Open a browser to the Freescale® website (<http://www.freescale.com>), and enter the appropriate document number (from Table B-2) in the "Enter Keyword" search box at the top of the page.