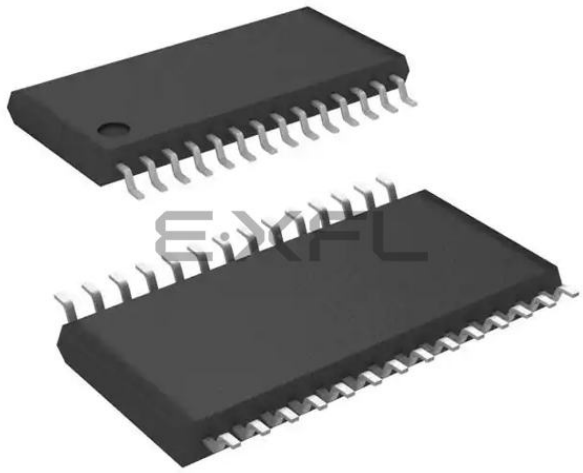

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08sg32e1wtl

Section Number	Title	Page

4.2 Reset and Interrupt Vector Assignments

Table 4-1 shows address assignments for reset and interrupt vectors. The vector names shown in this table are the labels used in the Freescale Semiconductor provided equate file for the MC9S08SG32 Series.

Table 4-1. Reset and Interrupt Vectors

Address (High/Low)	Vector	Vector Name
0xFFC0:0xFFC1	Reserved	—
0xFFC2:0xFFC3	ACMP	Vacmp
0xFFC4:0xFFC5	Reserved	—
0xFFC6:0xFFC7	Reserved	—
0xFFC8:0xFFC9	Reserved	—
0xFFCA:0xFFCB	MTIM Overflow	Vmtim
0xFFCC:0xFFCD	RTC	Vrtc
0xFFCE:0xFFCF	IIC	Viic
0xFFD0:0xFFD1	ADC Conversion	Vadc
0xFFD2:0xFFD3	Reserved	—
0xFFD4:0xFFD5	Port B Pin Interrupt	Vportb
0xFFD6:0xFFD7	Port A Pin Interrupt	Vporta
0xFFD8:0xFFD9	Reserved	—
0xFFDA:0xFFDB	SCI Transmit	Vscitx
0xFFDC:0xFFDD	SCI Receive	Vscirx
0xFFDE:0xFFDF	SCI Error	Vsc1err
0xFFE0:0xFFE1	SPI	Vspi
0xFFE2:0xFFE3	TPM2 Overflow	Vtpm2ovf
0xFFE4:0xFFE5	TPM2 Channel 1	Vtpm2ch1
0xFFE6:0xFFE7	TPM2 Channel 0	Vtpm2ch0
0xFFE8:0xFFE9	TPM1 Overflow	Vtpm1ovf
0xFFEA:0xFFEB	Reserved	—
0xFFEC:0xFFED	Reserved	—
0xFFEE:0xFFEF	Reserved	—
0xFFF0:0xFFF1	Reserved	—
0xFFF2:0xFFF3	TPM1 Channel 1	Vtpm1ch1
0xFFF4:0xFFF5	TPM1 Channel 0	Vtpm1ch0
0xFFF6:0xFFF7	Reserved	—
0xFFF8:0xFFF9	Low Voltage Detect	Vlvd
0xFFFA:0xFFFB	Reserved	—
0xFFFC:0xFFFD	SWI	Vswi
0xFFFE:0xFFFF	Reset	Vreset

other than the most experienced programmers because it can lead to subtle program errors that are difficult to debug.

The interrupt service routine ends with a return-from-interrupt (RTI) instruction which restores the CCR, A, X, and PC registers to their pre-interrupt values by reading the previously saved information from the stack.

NOTE

For compatibility with M68HC08 devices, the H register is not automatically saved and restored. It is good programming practice to push H onto the stack at the start of the interrupt service routine (ISR) and restore it immediately before the RTI that is used to return from the ISR.

If more than one interrupt is pending when the I bit is cleared, the highest priority source is serviced first (see Table 5-2).

5.5.1 Interrupt Stack Frame

Figure 5-1 shows the contents and organization of a stack frame. Before the interrupt, the stack pointer (SP) points at the next available byte location on the stack. The current values of CPU registers are stored on the stack starting with the low-order byte of the program counter (PCL) and ending with the CCR. After stacking, the SP points at the next available location on the stack which is the address that is one less than the address where the CCR was saved. The PC value that is stacked is the address of the instruction in the main program that would have executed next if the interrupt had not occurred.

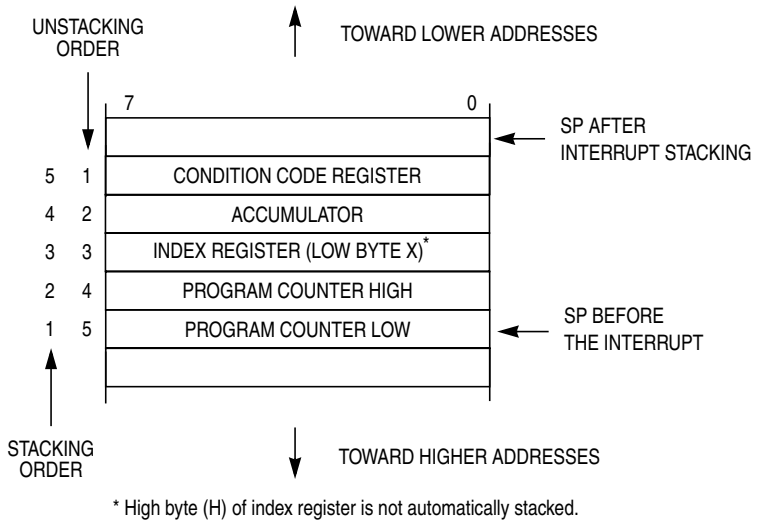


Figure 5-1. Interrupt Stack Frame

When an RTI instruction is executed, these values are recovered from the stack in reverse order. As part of the RTI sequence, the CPU fills the instruction pipeline by reading three bytes of program information, starting from the PC address recovered from the stack.

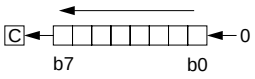
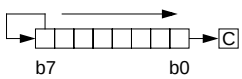
7.5 HCS08 Instruction Set Summary

Table 7-2 provides a summary of the HCS08 instruction set in all possible addressing modes. The table shows operand construction, execution time in internal bus clock cycles, and cycle-by-cycle details for each addressing mode variation of each instruction.

Table 7-2. Instruction Set Summary (Sheet 1 of 9)

Source Form	Operation	Address Mode	Object Code	Cycles	Cyc-by-Cyc Details	Affecton CCR	
						V 1 1 H	I N Z C
ADC *#opr8i* ADC *opr8a* ADC *opr16a* ADC *oprx16*,X ADC *oprx8*,X ADC ,X ADC *oprx16*,SP ADC *oprx8*,SP	Add with Carry A ← (A) + (M) + (C)	IMM DIR EXT IX2 IX1 IX SP2 SP1	A9 ii B9 dd C9 hh ll D9 ee ff E9 ff F9 9E D9 ee ff 9E E9 ff	2 3 4 4 3 3 5 4	pp rpp prpp prpp rpp rfp pprpp prpp	↕ 1 1 ↕	– ↕ ↕ ↕

ADD *#opr8i*
ADD *opr8a*
ADD *opr16a*
ADD *oprx16*,X
ADD *oprx8*,X
ADD ,X
ADD *oprx16*,SP
ADD *oprx8*,SP
	Add without Carry
	A ← (A) + (M)
		IMM
		DIR
		EXT
		IX2
		IX1
		IX
		SP2
		SP1
			AB ii
			BB dd
			CB hh ll
			DB ee ff
			EB ff
			FB
			9E DB ee ff
			9E EB ff
				2
				3
				4
				4
				3
				3
				5
				4
					pp
					rpp
					prpp
					prpp
					rpp
					rfp
					pprpp
					prpp
						↕ 1 1 ↕	– ↕ ↕ ↕

AIS *#opr8i*	Add Immediate Value (Signed) to Stack Pointer SP ← (SP) + (M)	IMM	A7 ii	2	pp	– 1 1 –	– – – –
AIX *#opr8i*	Add Immediate Value (Signed) to Index Register (H:X) H:X ← (H:X) + (M)	IMM	AF ii	2	pp	– 1 1 –	– – – –
AND *#opr8i* AND *opr8a* AND *opr16a* AND *oprx16*,X AND *oprx8*,X AND ,X AND *oprx16*,SP AND *oprx8*,SP	Logical AND A ← (A) & (M)	IMM DIR EXT IX2 IX1 IX SP2 SP1	A4 ii B4 dd C4 hh ll D4 ee ff E4 ff F4 9E D4 ee ff 9E E4 ff	2 3 4 4 3 3 5 4	pp rpp prpp prpp rpp rfp pprpp prpp	0 1 1 –	– ↕ ↕ –
ASL *opr8a* ASLA ASLX ASL *oprx8*,X ASL ,X ASL *oprx8*,SP	Arithmetic Shift Left  (Same as LSL)	DIR INH INH IX1 IX SP1	38 dd 48 58 68 ff 78 9E 68 ff	5 1 1 5 4 6	rfwpp p p rfwpp rfwp prfwpp	↕ 1 1 –	– ↕ ↕ ↕
ASR *opr8a* ASRA ASRX ASR *oprx8*,X ASR ,X ASR *oprx8*,SP	Arithmetic Shift Right  	DIR INH INH IX1 IX SP1	37 dd 47 57 67 ff 77 9E 67 ff	5 1 1 5 4 6	rfwpp p p rfwpp rfwp prfwpp	↕ 1 1 –	– ↕ ↕ ↕

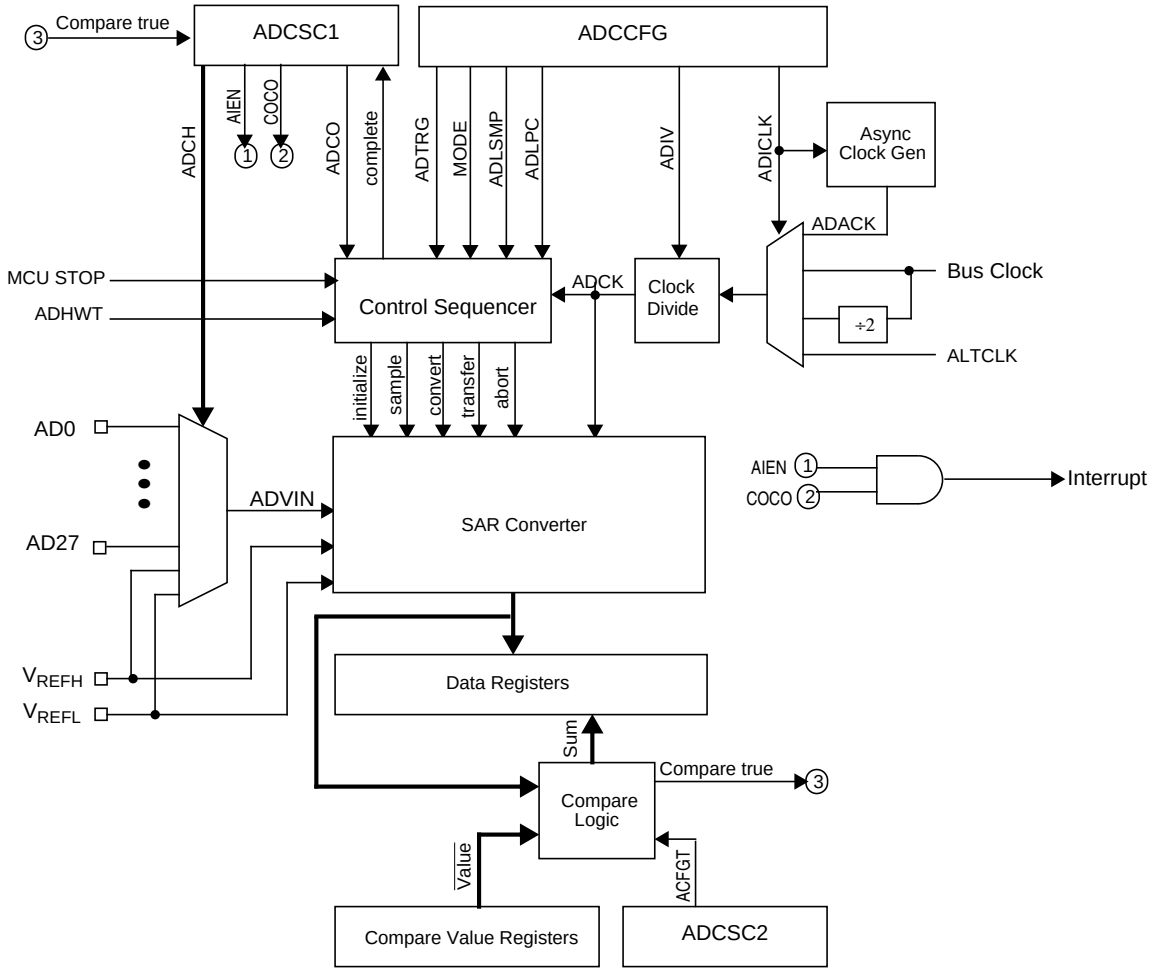


Figure 9-2. ADC Block Diagram

9.2 External Signal Description

The ADC module supports up to 28 separate analog inputs. It also requires four supply/reference/ground connections.

Table 9-2. Signal Properties

Name	Function
AD27–AD0	Analog Channel inputs
V_{REFH}	High reference voltage
V_{REFL}	Low reference voltage
V_{DDA}	Analog power supply
V_{SSA}	Analog ground

12.4.1 MTIM Operation Example

This section shows an example of the MTIM operation as the counter reaches a matching value from the modulo register.

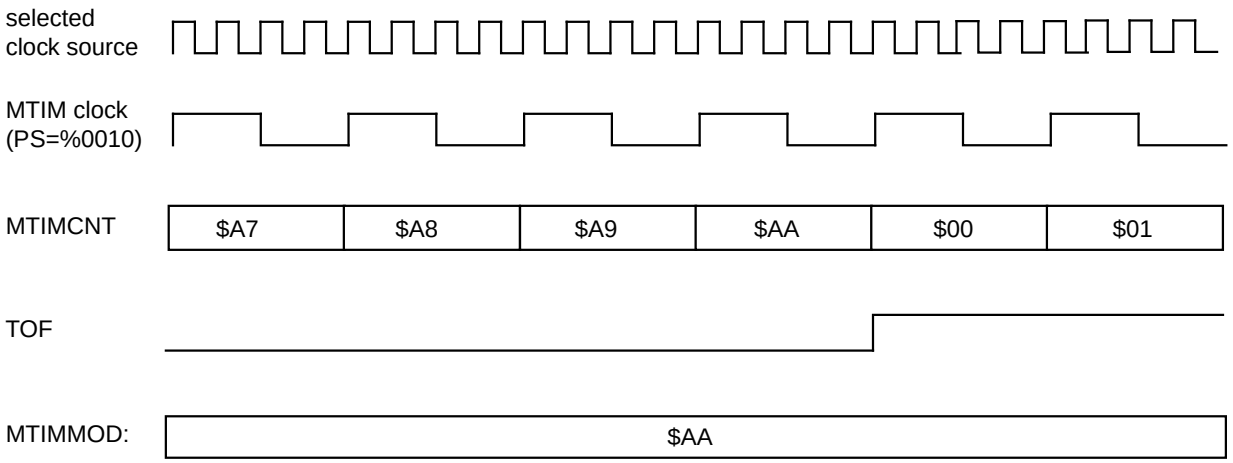


Figure 12-8. MTIM counter overflow example

In the example of Figure 12-8, the selected clock source could be any of the five possible choices. The prescaler is set to PS = %0010 or divide-by-4. The modulo value in the MTIMMOD register is set to $AA. When the counter, MTIMCNT, reaches the modulo value of $AA, the counter overflows to $00 and continues counting. The timer overflow flag, TOF, sets when the counter value changes from $AA to $00. An MTIM overflow interrupt is generated when TOF is set, if TOIE = 1.

Chapter 13
Real-Time Counter (S08RTCV1)

13.1 Introduction

The RTC module consists of one 8-bit counter, one 8-bit comparator, several binary-based and decimal-based prescaler dividers, two clock sources, and one programmable periodic interrupt. This module can be used for time-of-day, calendar or any task scheduling functions. It can also serve as a cyclic wake up from low power modes without the need of external components.

pin from a master and the MISO waveform applies to the MISO output from a slave. The $\overline{SS}$ OUT waveform applies to the slave select output from a master (provided MODFEN and SSOE = 1). The master $\overline{SS}$ output goes to active low one-half SPSCK cycle before the start of the transfer and goes back high at the end of the eighth bit time of the transfer. The $\overline{SS}$ IN waveform applies to the slave select input of a slave.

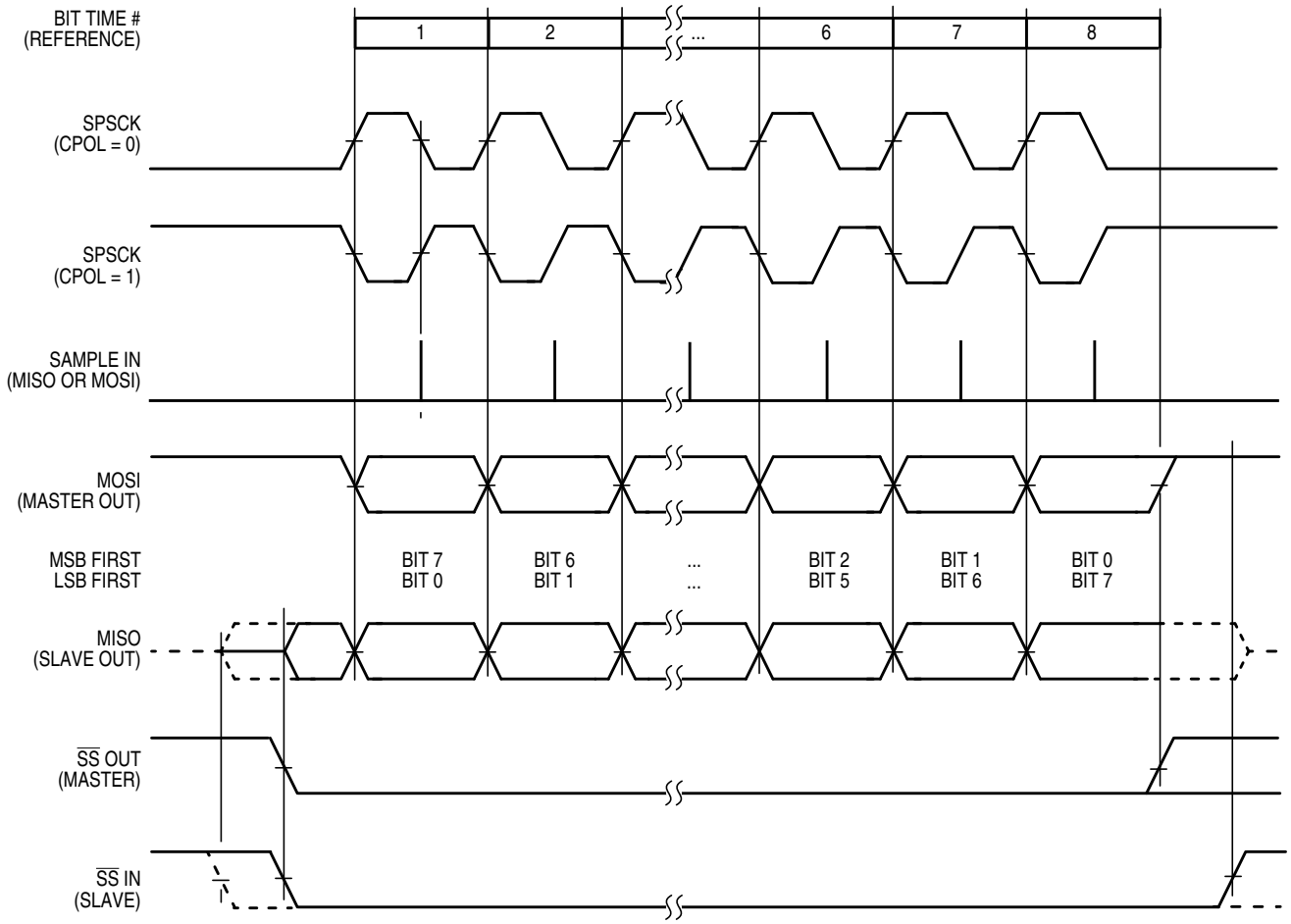


Figure 15-10. SPI Clock Formats (CPHA = 1)

When CPHA = 1, the slave begins to drive its MISO output when $\overline{SS}$ goes to active low, but the data is not defined until the first SPSCK edge. The first SPSCK edge shifts the first bit of data from the shifter onto the MOSI output of the master and the MISO output of the slave. The next SPSCK edge causes both the master and the slave to sample the data bit values on their MISO and MOSI inputs, respectively. At the third SPSCK edge, the SPI shifter shifts one bit position which shifts in the bit value that was just sampled, and shifts the second data bit value out the other end of the shifter to the MOSI and MISO outputs of the master and slave, respectively. When CHPA = 1, the slave's $\overline{SS}$ input is not required to go to its inactive high level between transfers.

Figure 15-11 shows the clock formats when CPHA = 0. At the top of the figure, the eight bit times are shown for reference with bit 1 starting as the slave is selected ($\overline{SS}$ IN goes low), and bit 8 ends at the last SPSCK edge. The MSB first and LSB first lines show the order of SPI data bits depending on the setting

- Non-intrusive commands can be executed at any time even while the user's program is running. Non-intrusive commands allow a user to read or write MCU memory locations or access status and control registers within the background debug controller.

Typically, a relatively simple interface pod is used to translate commands from a host computer into commands for the custom serial interface to the single-wire background debug system. Depending on the development tool vendor, this interface pod may use a standard RS-232 serial port, a parallel printer port, or some other type of communications such as a universal serial bus (USB) to communicate between the host PC and the pod. The pod typically connects to the target system with ground, the BKGD pin, $\overline{\text{RESET}}$, and sometimes V_{DD}. An open-drain connection to reset allows the host to force a target system reset, which is useful to regain control of a lost target system or to control startup of a target system before the on-chip nonvolatile memory has been programmed. Sometimes V_{DD} can be used to allow the pod to use power from the target system to avoid the need for a separate power supply. However, if the pod is powered separately, it can be connected to a running target system without forcing a target system reset or otherwise disturbing the running application program.

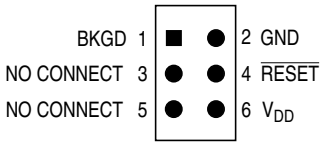


Figure 17-1. BDM Tool Connector

17.2.1 BKGD Pin Description

BKGD is the single-wire background debug interface pin. The primary function of this pin is for bidirectional serial communication of active background mode commands and data. During reset, this pin is used to select between starting in active background mode or starting the user's application program. This pin is also used to request a timed sync response pulse to allow a host development tool to determine the correct clock frequency for background debug serial communications.

BDC serial communications use a custom serial protocol first introduced on the M68HC12 Family of microcontrollers. This protocol assumes the host knows the communication clock rate that is determined by the target BDC clock rate. All communication is initiated and controlled by the host that drives a high-to-low edge to signal the beginning of each bit time. Commands and data are sent most significant bit first (MSB first). For a detailed description of the communications protocol, refer to Section 17.2.2, "Communication Details."

If a host is attempting to communicate with a target MCU that has an unknown BDC clock rate, a SYNC command may be sent to the target MCU to request a timed sync response signal from which the host can determine the correct communication speed.

BKGD is a pseudo-open-drain pin and there is an on-chip pullup so no external pullup resistor is required. Unlike typical open-drain pins, the external RC time constant on this pin, which is influenced by external capacitance, plays almost no role in signal rise time. The custom protocol provides for brief, actively driven speedup pulses to force rapid rise times on this pin without risking harmful drive level conflicts. Refer to Section 17.2.2, "Communication Details," for more detail.

The SYNC command is unlike other BDC commands because the host does not necessarily know the correct communications speed to use for BDC communications until after it has analyzed the response to the SYNC command.

To issue a SYNC command, the host:

- Drives the BKGD pin low for at least 128 cycles of the slowest possible BDC clock (The slowest clock is normally the reference oscillator/64 or the self-clocked rate/64.)
- Drives BKGD high for a brief speedup pulse to get a fast rise time (This speedup pulse is typically one cycle of the fastest clock in the system.)
- Removes all drive to the BKGD pin so it reverts to high impedance
- Monitors the BKGD pin for the sync response pulse

The target, upon detecting the SYNC request from the host (which is a much longer low time than would ever occur during normal BDC communications):

- Waits for BKGD to return to a logic high
- Delays 16 cycles to allow the host to stop driving the high speedup pulse
- Drives BKGD low for 128 BDC clock cycles
- Drives a 1-cycle high speedup pulse to force a fast rise time on BKGD
- Removes all drive to the BKGD pin so it reverts to high impedance

The host measures the low time of this 128-cycle sync response pulse and determines the correct speed for subsequent BDC communications. Typically, the host can determine the correct communication speed within a few percent of the actual target speed and the communication protocol can easily tolerate speed errors of several percent.

17.2.4 BDC Hardware Breakpoint

The BDC includes one relatively simple hardware breakpoint that compares the CPU address bus to a 16-bit match value in the BDCBKPT register. This breakpoint can generate a forced breakpoint or a tagged breakpoint. A forced breakpoint causes the CPU to enter active background mode at the first instruction boundary following any access to the breakpoint address. The tagged breakpoint causes the instruction opcode at the breakpoint address to be tagged so that the CPU will enter active background mode rather than executing that instruction if and when it reaches the end of the instruction queue. This implies that tagged breakpoints can only be placed at the address of an instruction opcode while forced breakpoints can be set at any address.

The breakpoint enable (BKPTEN) control bit in the BDC status and control register (BDCSCR) is used to enable the breakpoint logic (BKPTEN = 1). When BKPTEN = 0, its default value after reset, the breakpoint logic is disabled and no BDC breakpoints are requested regardless of the values in other BDC breakpoint registers and control bits. The force/tag select (FTS) control bit in BDCSCR is used to select forced (FTS = 1) or tagged (FTS = 0) type breakpoints.

The on-chip debug module (DBG) includes circuitry for two additional hardware breakpoints that are more flexible than the simple breakpoint in the BDC module.

A.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table A-3. Thermal Characteristics

#	C	Rating	Symbol	Value		Unit	Temp Rated	
							Standard	AEC Grade 0
1	—	Operating temperature range (packaged)						
		Temperature Code W	T_A	–40 to 150		°C	—	♦
		Temperature Code J		–40 to 140			—	♦
		Temperature Code M		–40 to 125			♦	—
		Temperature Code V		–40 to 105			♦	—
		Temperature Code C		–40 to 85			♦	—
2	D	Thermal resistance, Single-layer board						
				Airflow @200 ft/min	Natural Convection			
		28-pin TSSOP	θ_{JA}	71	91	°C/W	♦	♦
		20-pin TSSOP		94	114		♦	—
		16-pin TSSOP		108	133		♦	♦
3	D	Thermal resistance, Four-layer board						
				Airflow @200 ft/min	Natural Convection			
		28-pin TSSOP	θ_{JA}	51	58	°C/W	♦	♦
		20-pin TSSOP		68	75		♦	—
		16-pin TSSOP		78	92		♦	♦
4	D	Maximum junction temperature	T_J	135		°C	♦	—
				155			—	♦

A.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table A-7. Supply Current Characteristics

#	C	Parameter	Symbol	V_{DD} (V)	Typ[1]	Max[2]	Unit	Temp Rated	
								Standard	AEC Grade 0
1	C	Run supply current[3] measured at (CPU clock = 4 MHz, f_{Bus} = 2 MHz)	RI_{DD}	5	1.4	3	mA	♦	♦
	C			3	1.3	2.5	mA	♦	♦
2	P	Run supply current[3] measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)	RI_{DD}	5	4.7	7.5	mA	♦	♦
	C			3	4.6	7	mA	♦	♦
3	C	Run supply current[4] measured at (CPU clock = 32 MHz, f_{Bus} = 16MHz)	RI_{DD}	5	8.9	10	mA	♦	♦
	C			3	8.7	9.6	mA	♦	♦
4		Stop3 mode supply current							
	C	–40°C (C,V, and M suffix)	$S3I_{DD}$	5	0.96	–	µA	♦	—
	P	25°C (All parts)			1.3	–	µA	♦	—
	P[5]	85°C (C suffix only)			16.9	35	µA	♦	—
	P[5]	105°C (V suffix only)			37	90	µA	♦	—
	P[5]	125°C (M suffix only)			84	150	µA	♦	—
	C	–40°C (C,V, and M suffix)		3	0.85	–	µA	♦	—
	P	25°C (All parts)			1.2	–	µA	♦	—
	P[5]	85°C (C suffix only)			14.8	30	µA	♦	—
	P[5]	105°C (V suffix only)			32.7	80	µA	♦	—
	P[5]	125°C (M suffix only)			75	130	µA	♦	—

A.8 External Oscillator (XOSC) Characteristics

Table A-8. Oscillator Electrical Specifications (Temperature Range = –40 to 125°C Ambient)

#	C	Rating	Symbol	Min	Typ[1]	Max	Unit	Temp Rated	
								Standard	AEC Grade 0
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)							
		Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz	♦	♦
		High range (RANGE = 1) FEE or FBE mode [2]	f_{hi}	1	—	5	MHz	♦	♦
		High range (RANGE = 1, HGO = 1) FBELP mode	f_{hi-hgo}	1	—	16	MHz	♦	♦
		High range (RANGE = 1, HGO = 0) FBELP mode	f_{hi-lp}	1	—	8	MHz	♦	♦
2	—	Load capacitors	C_1, C_2	See crystal or resonator manufacturer's recommendation.					
3	—	Feedback resistor							
		Low range (32 kHz to 100 kHz)	R_F	—	10	—	MΩ	♦	♦
		High range (1 MHz to 16 MHz)		—	1	—	MΩ	♦	♦
4	—	Series resistor							
		Low range, low gain (RANGE = 0, HGO = 0)	R_S	—	0	—	kΩ	♦	♦
		Low range, high gain (RANGE = 0, HGO = 1)		—	100	—	kΩ	♦	♦
		High range, low gain (RANGE = 1, HGO = 0)		—	0	—	kΩ	♦	♦
		High range, high gain (RANGE = 1, HGO = 1)							
		≥ 8 MHz		—	0	0	kΩ	♦	♦
		4 MHz		—	0	10	kΩ	♦	♦
		1 MHz		—	0	20	kΩ	♦	♦
5	T	Crystal start-up time [3]							
		Low range, low gain (RANGE = 0, HGO = 0)	$t_{CSTL-LP}$	—	200	—	ms	♦	♦
		Low range, high gain (RANGE = 0, HGO = 1)	$t_{CSTL-HGO}$	—	400	—	ms	♦	♦
		High range, low gain (RANGE = 1, HGO = 0)[4]	$t_{CSTH-LP}$	—	5	—	ms	♦	♦
		High range, high gain (RANGE = 1, HGO = 1)[4]	$t_{CSTH-HGO}$	—	20	—	ms	♦	♦
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)							
		FEE or FBE mode [2]	f_{extal}	0.03125	—	5	MHz	♦	♦
		FBELP mode		0	—	40	MHz	♦	—
		FBELP mode		0	—	36	MHz	—	♦

Table A-12. ADC Characteristics (continued)

#	Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Temp Rated		Comment
									Standard	AEC Grade 0	
	Full-scale error	28-pin packages only									
		10-bit mode	T	E_{FS}	0	±0.5	±1	LSB[2]	♦	♦	
		8-bit mode			0	±0.5	±0.5	LSB[2]	♦	♦	
		20-pin packages									
		10-bit mode	T	E_{FS}	0	±1.0	±1.5	LSB[2]	♦	—	
		8-bit mode			0	±0.5	±0.5	LSB[2]	♦	—	
		16-pin packages									
		10-bit mode	T	E_{FS}	0	±1.0	±1.5	LSB[2]	♦	♦	
		8-bit mode			0	±0.5	±0.5	LSB[2]	♦	♦	
	Quantization error	10-bit mode	D	E_Q	—	—	±0.5	LSB[2]	♦	♦	
		8-bit mode			—	—	±0.5	LSB[2]	♦	♦	
	Input leakage error	10-bit mode	D	E_{IL}	0	±0.2	±2.5	LSB[2]	♦	♦	Pad leakage[3] * R_{AS}
		8-bit mode			0	±0.1	±1	LSB[2]	♦	♦	
	Temp sensor slope	-40°C to 25°C	D	m	—	3.266	—	mV/°C	♦	♦	
		25°C to 125°C			—	3.638	—	mV/°C	♦	♦	
	Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.396	—	V	♦	♦	

1 Typical values assume V_{DD} = 5.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Based on input pad leakage current. Refer to pad electricals.

A.12 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

A.12.1 Control Timing

Table A-13. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit	Temp Rated	
								Standard	AEC Grade 0
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$) -40 C to 125 C	f_{Bus}	dc	—	20	MHz	♦	—
		> 125 C		dc	—	18	MHz	—	♦
2	D	Internal low power oscillator period -40 C to 125 C	t_{LPO}	700		1500	µs	♦	—
		> 125 C		600		1500	µs	—	♦
3	D	External reset pulse width[2]	t_{extrst}	100		—	ns	♦	♦
4	D	Reset low drive[3]	t_{rstdrv}	66 x t_{cyc}		—	ns	♦	♦
5	D	Pin interrupt pulse width Asynchronous path[2] / Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 / 1.5 x t_{cyc}	—	—	ns	♦	♦
6	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5]							
		Slew rate control disabled (PTxSE = 0)	t_{Rise}, t_{Fall}	—	40	—	ns	♦	♦
		Slew rate control enabled (PTxSE = 1)		—	75	—		♦	♦
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF)[5]							
		Slew rate control disabled (PTxSE = 0)	t_{Rise}, t_{Fall}	—	11	—	ns	♦	♦
		Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	—	35	—		♦	♦

1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 When any reset is initiated, internal circuitry drives the reset pin low for about 66 cycles of t_{cyc}. After POR reset, the bus clock frequency changes to the untrimmed DCO frequency ($f_{reset} = (f_{dco\_ut})/4$) because TRIM is reset to 0x80 and FTRIM is reset to 0, and there is an extra divide-by-two because BDIV is reset to 0:1. After other resets trim stays at the pre-reset value.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 125°C.

A.12.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table A-14. TPM Input Timing

#	C	Rating	Symbol	Min	Max	Unit	Temp Rated	
							Standard	AEC Grade 0
1	—	External clock frequency ($1/t_{TCLK}$)	f_{TCLK}	dc	$f_{Bus}/4$	MHz	♦	♦
2	—	External clock period	t_{TCLK}	4	—	t_{cyc}	♦	♦
3	—	External clock high time	t_{clkh}	1.5	—	t_{cyc}	♦	♦
4	—	External clock low time	t_{clkl}	1.5	—	t_{cyc}	♦	♦
5	—	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}	♦	♦

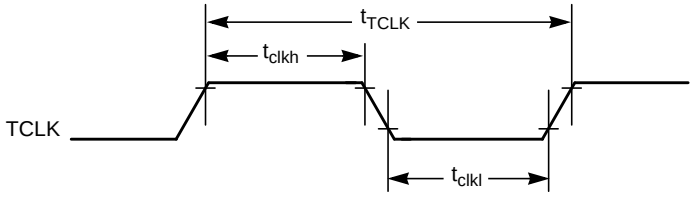


Figure A-12. Timer External Clock

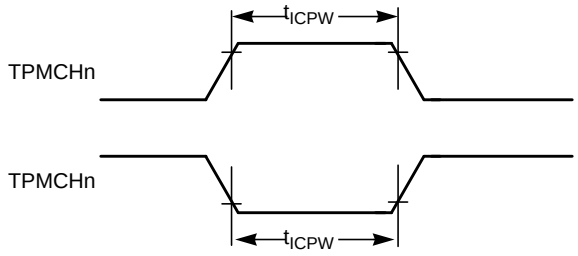


Figure A-13. Timer Input Capture Pulse

A.12.3 SPI

Table A-15 and Figure A-14 through Figure A-17 describe the timing requirements for the SPI system.

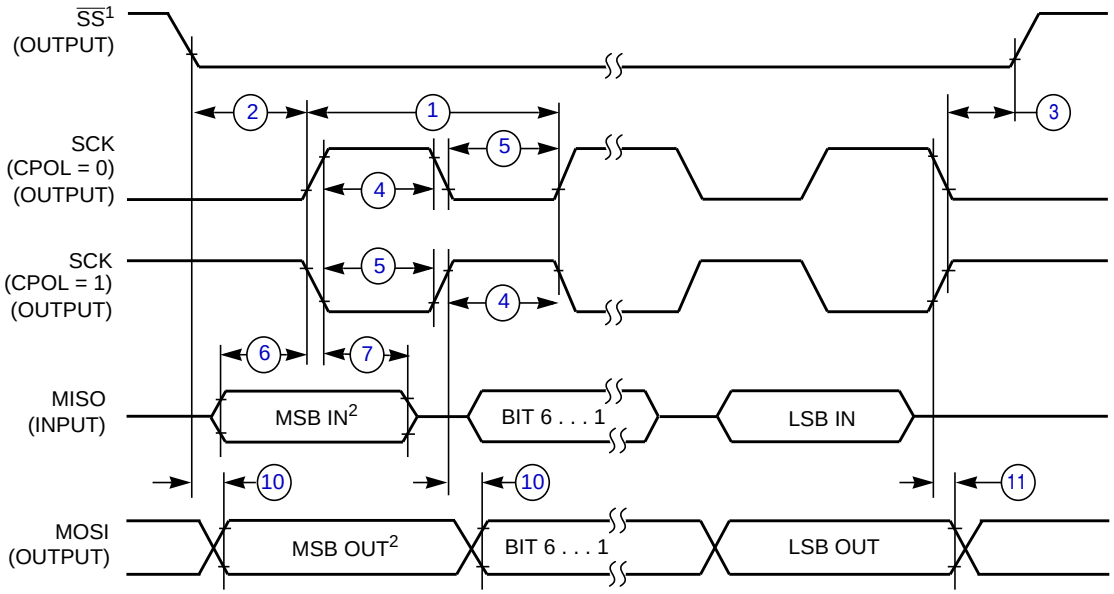
Table A-15. SPI Electrical Characteristic

Num[1]	C	Rating[2]	Symbol	Min	Max	Unit	Temp Rated	
							Standard	AEC Grade 0
1	D	Cycle time Master Slave	t_{SCK} t_{SCK}	2 4	2048 —	t_{cyc} t_{cyc}	♦	♦
2	D	Enable lead time Master Slave	t_{Lead} t_{Lead}	— 1/2	1/2 —	t_{SCK} t_{SCK}	♦	♦
3	D	Enable lag time Master Slave	t_{Lag} t_{Lag}	— 1/2	1/2 —	t_{SCK} t_{SCK}	♦	♦
4	D	Clock (SPSCK) high time Master and Slave	t_{SCKH}	1/2 t_{SCK} – 25	—	ns	♦	♦
5	D	Clock (SPSCK) low time Master and Slave	t_{SCKL}	1/2 t_{SCK} – 25	—	ns	♦	♦
6	D	Data setup time (inputs) Master Slave	$t_{SI(M)}$ $t_{SI(S)}$	30 30	— —	ns ns	♦	♦
7	D	Data hold time (inputs) Master Slave	$t_{HI(M)}$ $t_{HI(S)}$	30 30	— —	ns ns	♦	♦
8	D	Access time, slave[3]	t_A	0	40	ns	♦	♦
9	D	Disable time, slave[4]	t_{dis}	—	40	ns	♦	♦
10	D	Data setup time (outputs) Master Slave	t_{SO} t_{SO}	— —	25 25	ns ns	♦	♦
11	D	Data hold time (outputs) Master Slave	t_{HO} t_{HO}	–10 –10	— —	ns ns	♦	♦
12	D	Operating frequency Master Slave	f_{op} f_{op}	f_{Bus}/2048 dc	5^5 f_{Bus}/4	MHz	♦	♦

1 Refer to Figure A-14 through Figure A-17.

2 All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

3 Time to data active from high-impedance state.
4 Hold time to high-impedance state.
5 Maximum baud rate must be limited to 5 MHz due to input filter characteristics.



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-14. SPI Master Timing (CPHA = 0)

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