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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Networking and Communications
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	KSZ
RAM Size	-
Interface	EBI/EMI, Ethernet, I²C, I²S,PCI, SPI, UART/USART, USB
Number of I/O	20
Voltage - Supply	1.235V ~ 1.365V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	400-BGA
Supplier Device Package	400-PBGA (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ksz9692pb

Revision History

Revision	Date	Summary of Changes
1.0	10/14/08	Initial Release
2.0	3/10/09	Power Sequencing, Added A1 (PMEN) to pin list, 1.3V Supply for Core, Power Consumption table
3.0	8/10/09	DDR Data Width Changed to 16-bit
4.0	01/28/10	DDR Data Width Changed to 32-bit
4.1	06/10/10	Remove NAND Boot support
5.0	04/14/11	Add small packet device KSZ9692PB-S
	09/13/11	Change the USB Port 0 to Port 2 in Figure 12 and 13. Change RSVD to DATA[31..16] in Figure 20.

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System Level Applications

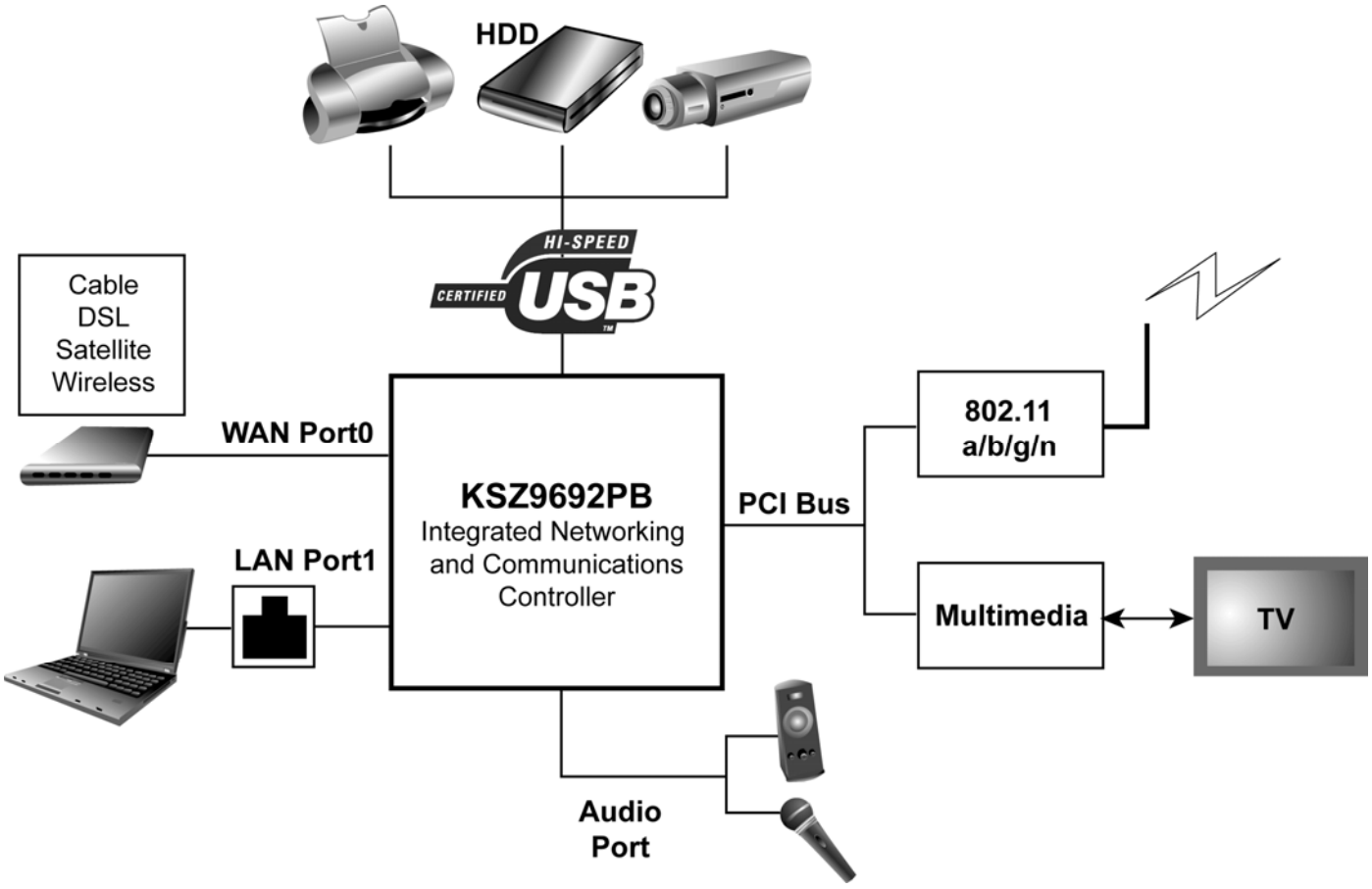


Figure 2. Peripheral Options and Examples

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
T2, U1, L5, N4, P3, R2, T1, M4, K5, N3, P2, R1, L4, M3, P1, K4	SDATA[15..0]	Ipu/O	SRAM DATA Bus. Bidirectional Bus for 16-bit DATA In and DATA Out. The KSZ9692PB, KSZ9692PB-S also supports 8-bit data bus for ROM/SRAM/FLASH/EXTIO cycles. This data bus is shared between NAND, ROM/SRAM/FLASH/EXTIO devices.
L3	ECS2	O	External I/O Chip Select 2, asserted Low. Three External I/O banks are provided for external memory-mapped I/O operations. Each I/O bank stores up to 16Kbytes. ECSN signals indicate which of the three I/O banks is selected.
N1	ECS1	O	External I/O Chip Select 1, asserted Low. Three External I/O banks are provided for external memory-mapped I/O operations. Each I/O bank stores up to 16Kbytes. ECSN signals indicate which of the three I/O banks is selected.
M2	ECS0	O	External I/O Chip Select 0, asserted Low. Three External I/O banks are provided for external memory-mapped I/O operations. Each I/O bank stores up to 16Kbytes. ECSN signals indicate which of the three I/O banks is selected.
K3	RCSN1	O	ROM/SRAM/FLASH(NOR) Chip select 1, asserted Low. The KSZ9692PB, KSZ9692PB-S can access up to two external ROM/SRAM/FLASH memory banks. The RCSN pins can be controlled to map the CPU addresses into physical memory banks.
L1	RCSN0	O	ROM/SRAM/FLASH(NOR) Chip select 0, asserted Low. The KSZ9692PB, KSZ9692PB-S can access up to two external ROM/SRAM/FLASH memory banks. The RCSN pins can be controlled to map the CPU addresses into physical memory banks. This bank is configurable as boot option
N2	EWAITN	I	External Wait asserted Low. This signal is asserted when an external I/O device or ROM/SRAM/FLASH(NOR) bank needs more access cycles than those defined in the corresponding control register.
M1	EROEN (WRSTPLS)	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Output Enable, asserted Low. When asserted, this signal controls the output enable port of the specified ROM/SRAM/FLASH memory and EXTIO device.
J5	ERWEN1	O	ROM/SRAM/FLASH(NOR) and EXTIO Write Byte Enable, asserted Low. When asserted, this signal controls the byte write enable of the memory device SDATA[15..8] for ROM/SRAM/FLASH and EXTIO access.
J4	ERWEN0	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Write Byte Enable, asserted Low. When asserted, this signal controls the byte write enable of the memory device SDATA[7..0 or 15..0] for ROM/SRAM/FLASH and EXTIO access.

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
T17, V18, U17, T16, W20, W19, Y20, Y19, W18, V17, U16, T15, Y18, V16	DADDR[13..0]	O	DDR Address Bus.
V13, U11, V12, W13, Y13, W12, V11, U10, V10, Y11, W10, U9, Y10, V9, W9, Y9, W8, Y8, Y7, W7, V7, Y6, W6, V6, Y5, V5, W5, U5, T5, Y4, V4, W4	DDATA[31..0]	I/O	DDR Data Bus.
T13, V14	BA[1:0]	O	DDR Bank Address.
U14	CSN	O	DDR Chip Select, asserted Low. Chip select pins for DDR, the KSZ9692PB, KSZ9692PB-S supports only one DDR bank.
T14	RASN	O	DDR Row Address Strobe, asserted Low. The Row Address Strobe pin for DDR.
U15	CASN	O	DDR Column Address Strobe, asserted Low. The Column Address Strobe pin for DDR.
V15	WEN	O	DDR Write Enable, asserted Low. The write enable signal for DDR.
U8, T6 T12,Y12	DM[3:0]	O	Data Input/Output mask signals for DDR. DM is sampled High and is an output mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a Write cycle. DM0 corresponds to DDATA[7:0], DM1 corresponds to DDATA[15:8], DM2 corresponds to DDATA[23:16] and DM3 corresponds to DDATA[31:24].
V8, U6 U12,W11	DQS[3:0]	I/O	DDR only Data Strobe Input with read data, output with write data. DQS0 corresponds to DDATA[7:0], DQS1 corresponds to DDATA[15:8].

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
D13	KSDWP	I	Active high used for Card write protection
General Purpose I/O			
B14	SLED/GPIO[19]	I/O	SDIO Line Status LED output or General Purpose I/O Pin[19]
B15	CPUINTN/ GPIO[18]	I/O	Internal CPU interrupt request or General Purpose I/O Pin[18] As CPUINTN, any interrupt generated to ARM CPU asserts logic low on this pin. Useful for software development.
B16, B17, B18, D18, E15, D19	GPIO[17:12]	I/O	General Purpose I/O Pin[17:12]
F14	UART 4 RTSN /GPIO[11]	I/O	UART 4 RTS or general purpose I/O Pin[11]
E16	UART 4 CTSN /GPIO[10]	I/O	UART 4 CTS or general purpose I/O Pin[10]
E17	UART 3 RTSN /GPIO[9]	I/O	UART 3 RTS or general purpose I/O Pin[9]
E19	UART 3 CTSN /GPIO[8]	I/O	UART 3 CTS or general purpose I/O Pin[8]
E20	UART 2 RTSN /GPIO[7]	I/O	UART 2 RTS or general purpose I/O Pin[7]
E18	UART 2 CTSN /GPIO[6]	I/O	UART 2 CTS or general purpose I/O Pin[6]
U20, U19	TOUT[1:0]/ GPIO[5:4]	I/O	Timer 1/0 out or General Purpose I/O Pin[5:4]
V20, T18, V19, U18	EINT[3:0]/ GPIO[3:0]	I/O	External Interrupt Request or General Purpose I/O Pin[3:0]
I2S Interface			
C20	SCKIN	I	External crystal or clock input for I2S clock The maximum supported frequency is 49.2MHz
D20	SCKOUT	O	External Crystal out for I2S clock
C19	I2S_MCLK	O	I2S master clock out This clock is of same frequency as SCKIN
B20	I2S_BCLK	O	I2S bit clock out
B19	I2S_LRCLK	O	Left/right select
A19	I2S_SDO	O	Serial data out
A20	I2S_SDI	I	Serial data in
MDIO/MDC Interface			
H18	MDC	Ipu/O	Clock for station management
H17	MDIO	Ipu/O	Serial data for station management
I2C/SPI Interface			

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
B1	GNT1N	O	PCI Bus Grant 1 Assert Low. In Host Bridge Mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the master driving REQ1N. In Guest Bridge Mode, this is an output signal to indicate to the external PCI bus arbiter that KSZ9692PB, KSZ9692PB-S is requesting access to the PCI bus.
D3	REQ3N	I	PCI Bus Request 3 Assert Low. In Host Bridge Mode, this is an input signal from the external PCI device to request for PCI bus access In Guest Bridge Mode, this is unused.
E6	REQ2N	I	PCI Bus Request 2 Assert Low. In Host Bridge Mode, this is an input signal from the external PCI device to request for PCI bus access In Guest Bridge Mode, this is unused.
C1	REQ1N	I	PCI Bus Request 1 Assert Low. In Host Bridge Mode, this is an input signal from the external PCI device to request for PCI bus access In Guest Bridge Mode, this signal comes from the external arbiter to indicate that the bus is granted to KSZ9692PB, KSZ9692PB-S.
B3, E7, D6, A2, B4, A3, D7, C5, C6, B5, A4, A5, B6, E8, C7, D8, D10, B10, A11, B11, C11, A12, E11, D11, B12, A13, C12, B13, F12, C13, D12, E12	PAD[31..0]	I/O	32-bit PCI address and data lines Addresses and data bits are multiplexed on the same pins. During the first clock cycle of a PCI transaction, the PAD bus contains the first clock cycle of a PCI transaction, the PAD bus contains the physical address. During subsequent clock cycles, these lines contain the 32-bit data to be transferred. Depending on the type of the transaction, the source of the data will be the KSZ9692PB, KSZ9692PB-S if it initiates a PCI write transaction, or the data source will be the target if it is a PCI Read transaction. The KSZ9692PB, KSZ9692PB-S bus transaction consists of an address phase followed by one or more data phases. The KSZ9692PB, KSZ9692PB-S supports both Read and Write burst transactions. In case of a Read transaction, a special data turn around cycle is needed between the address phase and the data phase.
A6, A7, E10, C10	CBEN[3..0]	I/O	PCI Commands and Byte Enable, asserted Low. The PCI command and byte enable signals are multiplexed on the same pins. During the first clock cycle of a PCI transaction, the CBEN bus contains the command for the transaction. The PCI transaction consists of the address phases and one or more data phases. During the data phases of the transaction, the bus carries the byte enable for the current data phases.
C8	PAR	I/O	Parity PCI Bus parity is even across PAD[31:0] and CBEN[3:0]. The KSZ9692PB, KSZ9692PB-S generates PAR during the address phase and write data phases as a bus master, and during read data phases as a target. It checks for correct PAR during read data phase as a bus master, during every address phase as a bus slave, and during write data phases as a target.

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
TAP Control Signals			
A18	TCK	I	JTAG Test Clock
A17	TMS	I	JTAG Test Mode Select
A16	TDI	I	JTAG Test Data In
A15	TDO	O	JTAG Test Data Out
A14	TRSTN	I	JTAG Test Reset, asserted Low
Test Signals			
P5	SCANEN	Ipd	1 = Scan Enable (Factory reserved) 0 = Normal Operation
V2	TESTEN	Ipd	1 = Test Enable (Factory reserved) 0 = Normal Operation
V1	TESTEN1	Ipd	1 = Test Enable1 (Factory reserved) 0 = Normal Operation
Y2	TEST1	O (analog)	Factory reserved
W2	TEST2	O (analog)	Factory reserved
Power and Ground (96)			
N6, M6, M7, G7, G8, G9, M14, M15, N14, P11, P12, P13, P14	VDD1.2	P	Digital power supply 1.3V (13)
G6, H6, J6, K6, F7, F8, F9, F10, F11, G10, G11, H14, J14, K14, K15, L15	VDD3.3	P	Digital power supply 3.3V (16)
R6, R7, R8, R9, R10, R11, R12, R13, R14, T8, T9, T10, T11	VDD2.5	P	DDR Pad Driver 2.5V or 2.6V Power Supply. (13)
H7, H8, H9, H10, H11, J7, J8, J9, J10, J11, K7, K8, K9, K10, K11, K12, L7, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, N9, N10, N11, N12, N13, P7, P8, P9, P10	GND	GROUND	Digital Ground. (37)

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
L6	PLLVDDA3.3	P	Band Gap Reference Analog Power. (1)
M8	PLLVSSA3.3	GROUND	Band Gap Reference Analog Ground. (1)
P6	PLLDVDD1.2	P	De-skew PLL Analog and Digital Power. (1)
M5	PLLSVDD1.2	P	System PLL Analog and Digital Power. (1)
N7, N8	PLLVSS1.2	GROUND	De-skew PLL and System PLL Ground. (2)
L8	PLLVSSISO	GROUND	Ground Isolation PLL and other circuit. (1)
G12	USB1VDDA3.3	P	Analog Power for USB Channel 1. (1)
G13	USBCVDDA3.3	P	Analog Power for Common Circuit of USB Channel 1 and 2. (1)
G14	USB2VDDA3.3	P	Analog Power for USB Channel 2. (1)
H13, J13, K13	USBVSSA3.3	GROUND	Analog Ground for both USB Channels Analog Circuit. (3)
J15	USB1VDD1.2	P	Digital Power for USB Channel 1 Controller. (1)
H15	USB2VDD1.2	P	Digital Power for USB Channel 2 Controller. (1)
J12	USBVSS1	GROUND	Digital Ground for USB Channel 1 Controller. (1)
H12	USBVSS2	GROUND	Digital Ground for USB Channel 2 Controller. (1)

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   O/I = Output in normal mode; input pin during reset.
   Ipu = Internal 55kΩ pull-up resistor.
   Ipd = Internal 55kΩ pull-down resistor.

Pin Description: Power-up Strapping Options (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
G3	SADDR[11]	Ipd/O	During reset, this pin is input strap option to enable either MII or RGMII mode at port1 (LAN port) 0: MII mode (default) 1: RGMII mode
M1	EROEN (WRSTPLS)	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Output Enable, asserted Low. When asserted, this signal controls the output enable port of the specified ROM/SRAM/FLASH memory and EXTIO device. During reset, this pin is used for Watchdog Timer Reset Polarity Select. This is a power strapping option pin for watchdog reset output polarity. “0” = WRSTO is selected as active high (default) “1” = WRSTO is selected as active low. This pin is shared with the EROEN pin.
J4	ERWEN0	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Write Byte Enable, asserted Low. When asserted, these signals control the byte write enable of the memory device for ROM/SRAM/FLASH and EXTIO access. During ARM tic test mode, this pin is TESTACK. During reset, this pin is the input strap option to enable either MII or RGMII mode at port0 (WAN port) 0: MII mode (default) 1: RGMII mode
R3	NCLE	Ipd/O	NAND command Latch Enable NCLE controls the activating path for command sent to NAND flash. During reset, this pin is input strap option for NAND Flash configuration register (0x8054) bit [2]. This bit along with configuration register bits [1:0] is used for boot program. This pin along with NALE and NWEN is used to specify NAND Flash size. [NCLE, NALE, NWEN] 000 = 64Mbit 001 = 128Mbit (default) 010 = 256Mbit 011 = 512Mbit 100 = 1Gbit 101 = 2Gbit 110 = 4Gbit 111 = 8Gbit (Not support NAND Boot)

ARM High-Performance Processor

The KSZ9692PB, KSZ9692PB-S is built around the 16/32-bit ARM922T RISC processor designed by Advanced RISC Machines. The ARM922T is a scalable, high-performance processor that was developed for highly integrated SoC applications. Its simple, elegant, and fully static design is particularly suited to cost-effective and power-sensitive embedded systems. It also offers a separate 8KB D-cache and 8KB I-cache that reduces memory access latency.16-bit thumb instruction sets are supported to minimize memory footprint. The ARM processor core can be programmed to maximum of 250 MHz for highest possible performance.

The Advanced Microprocessor Bus Architecture/Advanced High Performance Bus (AMBA AHB) is a 32-bit wide ARM system bus to which is connected the processor, the register ports of the DDR memory controller, the FLASH/ROM/SRAM/External I/O controller, the NAND memory controller, the Ethernet MACs, the PCI bridge, the USB ports and the SDIO controller. The ARM processor is the master of AHB and responsible for configuring the operational characteristics of each AHB device via their individual register port. The AHB is programmable up to 166MHz for maximum system bus performance. AHB interfaces to devices are shown in functional the block diagram.

Also connected to the AHB is ARM Advanced Peripheral Bus or APB bridge which is attached the standard peripherals. The APB Bridge transparently converts the AHB accesses into slower APB accesses. The ARM processor is the master of APB bridge and responsible for configuring the operational characteristics and transfer of data for each APB attached peripheral. APB interfaces to standard peripherals are shown in the functional block diagram.

- 250MHz ARM922T RISC processor core
- 166MHz AMBA Bus 2.0
- 16-bit thumb instruction sets
- 8KB D-cache and 8KB I-cache
- Supports Little-Endian mode
- Configurable MMU
- Power saving options include clock down of both processor core and AMBA AHB

FLASH/ROM/SRAM Memory and External I/O Interface

The KSZ9692PB, KSZ9692PB-S memory controller provides glueless interface for static memory, i.e., ROM, SRAM, and NOR Flash and three banks of external I/O. NOR Flash bank0 can be configured by power-up strap option to operate as boot bank from a 8 or 16 bit device.

- Glueless connection to two banks of FLASH/ROM/SRAM memory with programmable 8 or 16 bit data width and programmable access timing
- Support for AMD/Intel like Flash
- Automatic address line mapping for 8 or 16-bit accesses on Flash, ROM, and SRAM interfaces
- Supports three external I/O banks with programmable 8 or 16 bit data width and programmable access timing
- Total 64MB address space for two banks of FLASH/ROM/SRAM and and three banks of external I/O

The memory interface for the static memory has a special automatic address mapping feature. This allows the designer to connect address bit 0 on the memory to ADDR[0] on the KSZ9692PB, KSZ9692PB-S and address bit 1 on the memory to ADDR[1] on the KSZ9692PB, KSZ9692PB-S, regardless of whether the designer is trying to achieve half word or byte addressing. The KSZ9692PB, KSZ9692PB-S memory controller performs the address mapping internally. This gives the designer the flexibilty to use 8 or 16 bit data width devices interchangeably on the same PCB (see Figure 4). For external I/O, however, the designer still needs to resolve the address mapping (see Figure 5).

NAND Flash Memory Interface

The KSZ9692PB, KSZ9692PB-S NAND controller provides interface to external NAND Flash memory. A total of two banks are supported. NAND Flash bank0 can be configured by power-up strap option to operate as boot bank. Both NAND Flash banks share data bus with FLASH/ROM/SRAM memory banks.

- Glueless connection to two banks with programmable 8 or 16 bit data width and programmable access timing
- Hardware ECC not supported
- Small page size 512 + 16 bytes
- Large page size 2048 + 64 bytes
- Large and small block size
- Boot option with automatic page crossing where pages are automatically opened sequentially by hardware
- Boot option with two 8-bit device in parallel to form a 16-bit bank
- Boot option with bank0 and bank1 as active banks in cascade
- Support for following device densities:
  - 64Mbit
  - 128Mbit
  - 256Mbit
  - 512Mbit
  - 1Gbit
  - 2Gbit
  - 4Gbit
  - 8Gbit

The following figures illustrate examples of NAND Flash bank configuration:

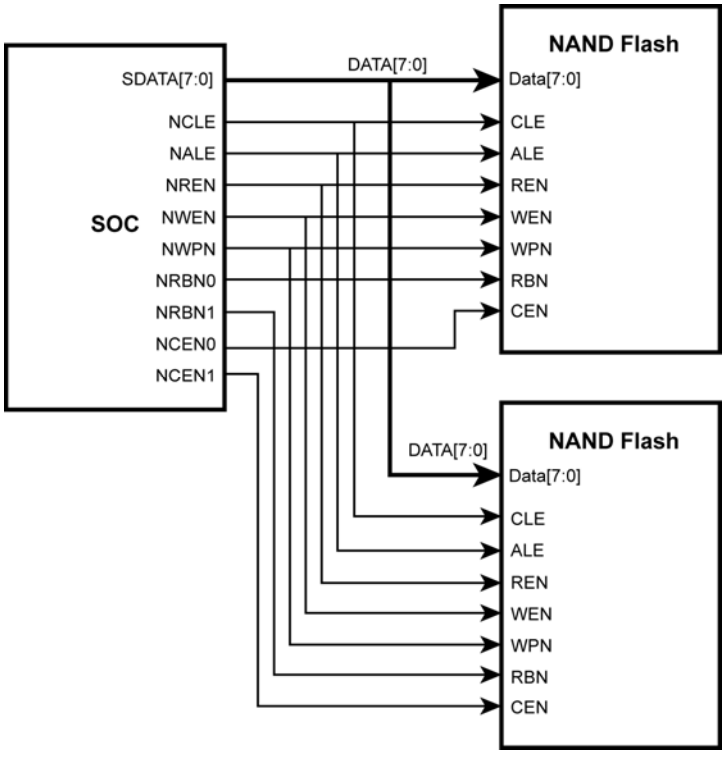


Figure 6. 8-bit NAND Interface Examples

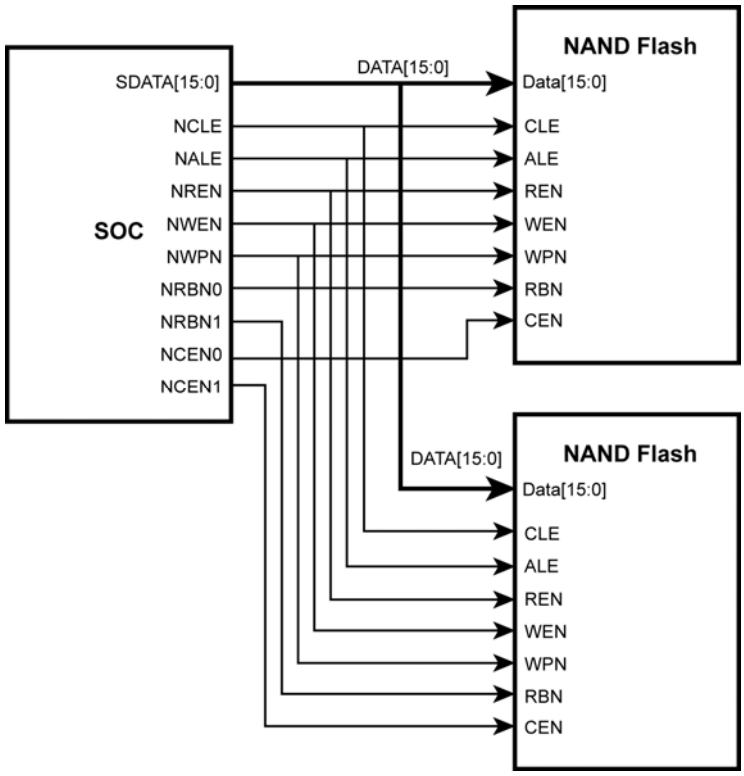


Figure 7. 16-bit NAND Interface Examples

DDR Controller

The KSZ9692PB, KSZ9692PB-S DDR memory controller provides interface for accessing external Double Data Rate Synchronous DRAM. In addition the KSZ9692PB, KSZ9692PB-S provides two integrated DDR differential clock drivers for a complete glueless DDR interface solution.

- Up to 200 MHz clock frequency (400 MHz data rate)
- Supports one 32-bit data width bank (16-bit optional)
- Up to 128MB of addressable space is available with 12 columns and 14 row address lines
- Supports all DDR device densities up to 1Gb
- Supports all DDR device data width x8 and x16
- Configurable DDR RAS and CAS timing parameters
- Two integrated JEDEC Specification JESD82-1 compliant differential clock drivers for a glueless DDR interface solution
- JEDEC Specification SSTL_2 I/Os

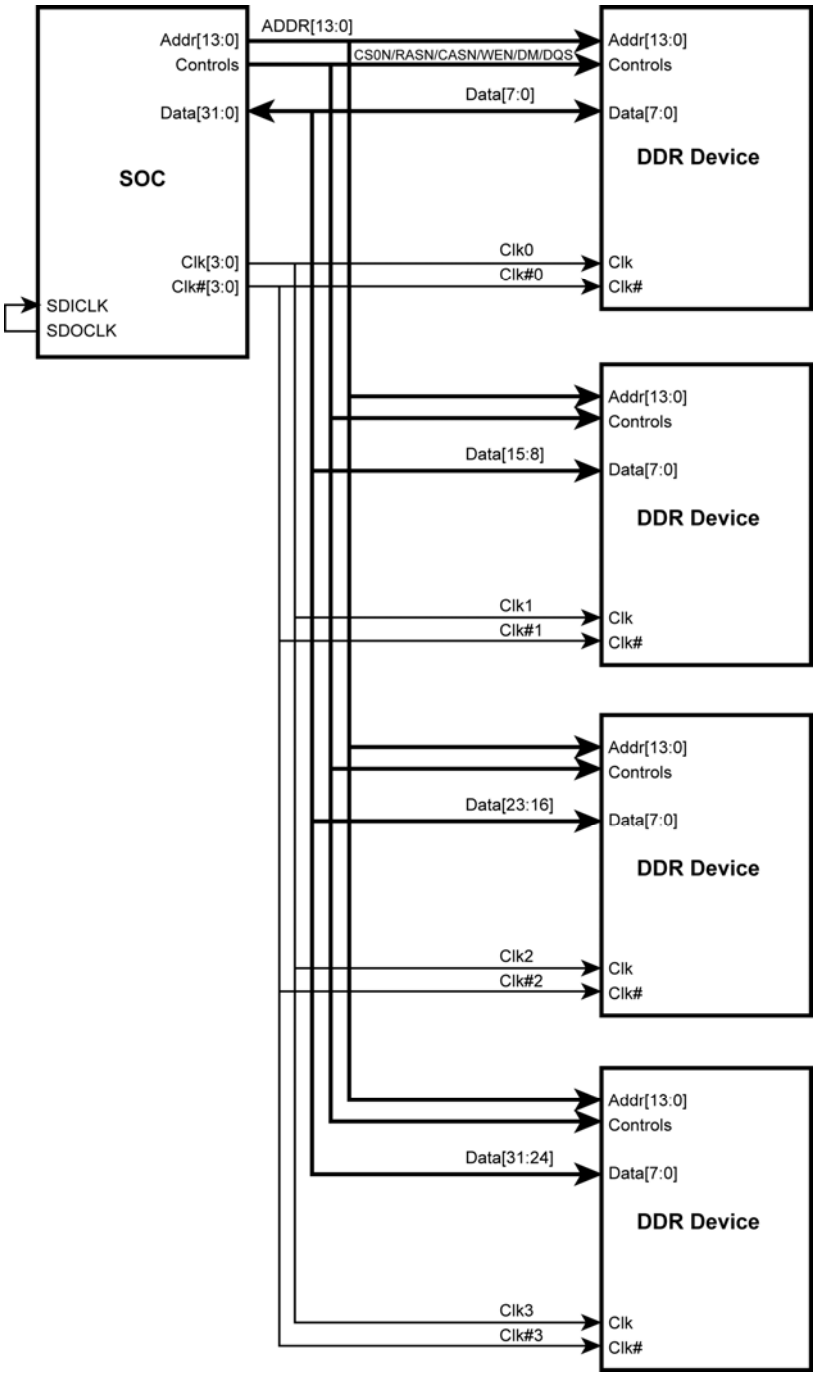


Figure 9. Two 8-bit DDR Memory Devices Interface Example

PCI Interface

The KSZ9692PB, KSZ9692PB-S integrates a PCI-to-AHB bridge solution for interfacing with 32-bit PCI, including miniPCI, and cardbus devices where it is common for 802.11x-based Wireless products. The PCI-AHB bridge supports two modes of operation in the PCI bus environment; host bridge mode and guest bridge mode. In the host bridge mode, the ARM processor acts as the host of the entire system. It configures other PCI devices and coordinates their transactions, including initiating transactions between the PCI devices and AHB bus subsystem. An on-chip PCI arbiter is included to determine the PCI bus ownership among up to three PCI master devices.

In guest bridge mode, all of the I/O registers are programmed by either the external host CPU on the PCI bus or the local ARM host processor through the AHB bus and the KSZ9692PB, KSZ9692PB-S can be configured by either the ARM or the PCI host CPU. In guest bridge mode, the on-chip PCI arbiter is disabled. In both cases, the KSZ9692PB, KSZ9692PB-S memory subsystem is accessible from either the PCI host or the ARM processor. Communications between the external host CPU and the ARM processor is accomplished through message passing or through shared memory.

- Compliant to PCI revision 2.3
- Support 33 and 66MHz, 32-bit data PCI bus
- Support 32-bit miniPCI or cardbus devices
- Supports both regular and memory-mapped I/O on the PCI interface
- AHB bus and PCI bus operate at independent clock domains
- Supports big endian and little endian on AHB
- PCI bus Round Robin arbiter for three external masters
- Supports high speed bus request and bus parking
- Dedicated DMA channel for bulk data transfer to/from DDR memory

Ethernet MAC Ports (Port 0 = WAN, Port 1 = LAN)

The KSZ9692PB, KSZ9692PB-S integrates two Gigabit Ethernet controllers that operate at 10, 100, and 1000 Mbps. Each controller has an interface that can operate as MII or RGMII to an external 10/100 or 10/100/1000 PHY to complete Ethernet network connectivity. An integrated 25 MHz clock eliminates external crystal or oscillator requirement for PHY to reduce cost. Integrated 2-pin (MDC & MDIO) Station Manager allows ARM processor to access PHY registers and pass control and status parameters. Wake-on-LAN is supported as part of the power management mechanism. Each port has a dedicated MIB counter to accumulate statistics for received and transmitted traffic.

- IEEE 802.3 compliant MAC layer function
- Configurable as MII or RGMII interface
- RGMII interface compliant to Reduced Gigabit Media Independent Interface(RGMII) Version 1.3
- MII interface compliant to Clause 22.2.4.5 of the IEEE 802.3u Specification
- 10/100/1000 Mbps half and full-duplex operation
- Automatic CRC generation and checking
- Automatic error packet discard
- Supports IPv4 Header and IPv4/IPv6 TCP/UDP checksum generation to offload host CPU
- Supports IPv4 Header and IPv4/IPv6 TCP/UDP checksum error detection
- Supports 32 rules ACL filtering
- Maximum frame length support is 2000 Byte at WAN port and 9K-byte at LAN port
- Contains large independent receive and transmit FIFOs (8KB receive / 8KB transmit at WAN and 24KB receive / 22KB transmit at LAN) for back-to-back packet receive, and guaranteed no-under run packet transmit
- Data alignment logic and scatter gather capability
- Configurable as MAC or PHY mode
- Separate transmit and receive DMA channels for each port

Wake-on-LAN

Wake-up frame events are used to wake the system whenever meaningful data is presented to the system over the network. Examples of meaningful data include the reception of a Magic Packet, a management request from a remote administrator,

frame's destination.

If the network controller scans a frame and does not find the specific sequence shown above, it discards the frame and takes no further action. If the KSZ9692PB, KSZ9692PB-S controller detects the data sequence, however, it then alerts the device's power management circuitry to wake up the system.

IPv6 Support

The KSZ9692PB, KSZ9692PB-S provides the following IPv6 support in the hardware:

- Generates the checksum for IPv6 TCP/UDP packets based on register configuration (LAN MAC DMA Transmit Control Register and WAN MAC DMA Transmit Control Register) or Transmit Descriptor 1 (TDES1). The register setting is static configuration and the TDES1 setting is packet based configuration.
- Filters IPv6 packets with TCP/UDP errors (LAN MAC DMA Receive Control Register and WAN MAC DMA Receive Control Register).
- Supports up to 8 Source IP or Destination IP based filtering (LAN/WAN Access Control List)

Refer to the Register Description Document for more details.

DMA Controller

Integrated DMA controller connects data port of IP Security Engine, two Gb Ethernet MACs, two USB 2.0 ports, PCI 2.3 bus interface, and SDIO interface via dedicated channels to DDR memory controller for moving large amounts of data without significant ARM processor intervention. A typical DMA channel usage is to move data from these interfaces into DDR memory. The data in the memory is processed by the ARM processor and driven back by the DMA channel to the external interface. Additionally, the ARM processor itself has a dedicated DMA channel to access the DDR memory controller. Flash/ROM/SRAM, NAND controller, and peripherals do not have dedicated DMA channel and therefore depend on the ARM processor for transfer of data to DDR memory. DMA channel interfaces are shown in the functional block diagram on page 7.

The arbitration of all requests from DMA channels are handled by the DDR memory controller and pipelined for best performance. The memory controller supports programmable bandwidth allocation for each DMA channel, thus enabling the designer to optimize I/O resource utilization of memory.

UART Interface

The KSZ9692PB, KSZ9692PB-S support four independent high-speed UARTs; UART1, UART2, UART3 and UART4. The UART ports enhance the system availability for legacy serial communication application and console port display.

UART1, UART2, UART3 and UART4 support maximum baud rate of 5 Mbps including standard rates. The higher rates allow for Bluetooth and GSM applications.

UART1 supports CTSN, DSRN, DCDN modem control pins in addition to RXD and TXD data pins. For UART2, UART3, UART4 only CTSN and RTSN control pins in addition to RXD and TXD data pins are supported.

Timers and Watchdog

Two programmable 32-bit timers with one capable of watchdog timer function. These timers can operate in a very flexible way. The host can control the timeout period as well as the pulse duration. Both timers can be enabled with interrupt capability. When the watchdog timer is programmed and the timer setting expires, the KSZ9692PB, KSZ9692PB-S resets itself and also asserts WRSTO to reset other devices in the system.

GPIO

Twenty general purpose I/O (GPIO) are individually programmable as input or output. Some GPIO ports are programmable for alternate function as listed below:

- Four GPIO programmable as inputs for external interrupts
- Two GPIO programmable as 32-bit timers output
- Six GPIO programmable as CTSN and RTSN control pins for UART2, UART3, UART4
- One GPIO programmable as SDIO Line Status LED driver
- One GPIO programmable as ARM CPU interrupt line activity.

See Signal Description list for detailed GPIO map.

Timing Specifications

Figure 16 provides power sequencing requirement with respect to system reset.

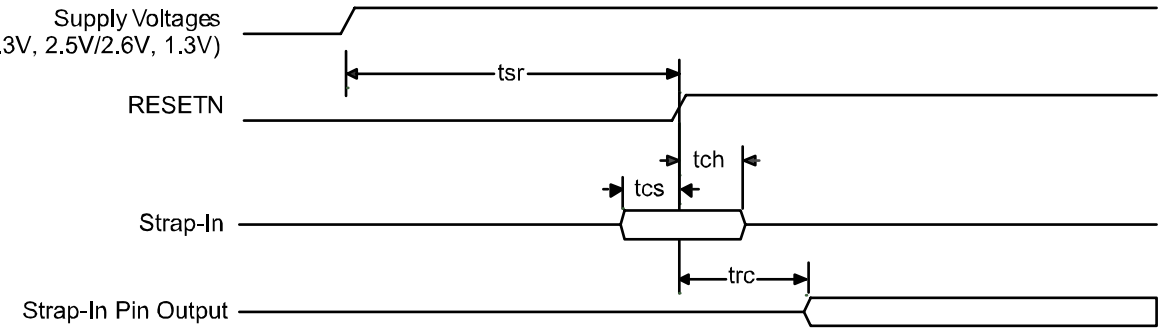


Figure 16. Reset Timing

Note: Power sequencing of supply voltages must be in order of 3.3V first, 2.5V/2.6V next and 1.3V last.

Symbol	Parameter	Min	Typ	Max	Units
t_{SR}	Stable supply voltages to reset high	10			ms
t_{CS}	Configuration set-up time	50			ns
t_{CH}	Configuration hold time	50			ns
t_{RC}	Reset to strap-in pin output	50			ns

Table 1. Reset Timing Parameters

Figure 17 and Figure 18 provide NOR FLASH, ROM and SRAM interface timing.

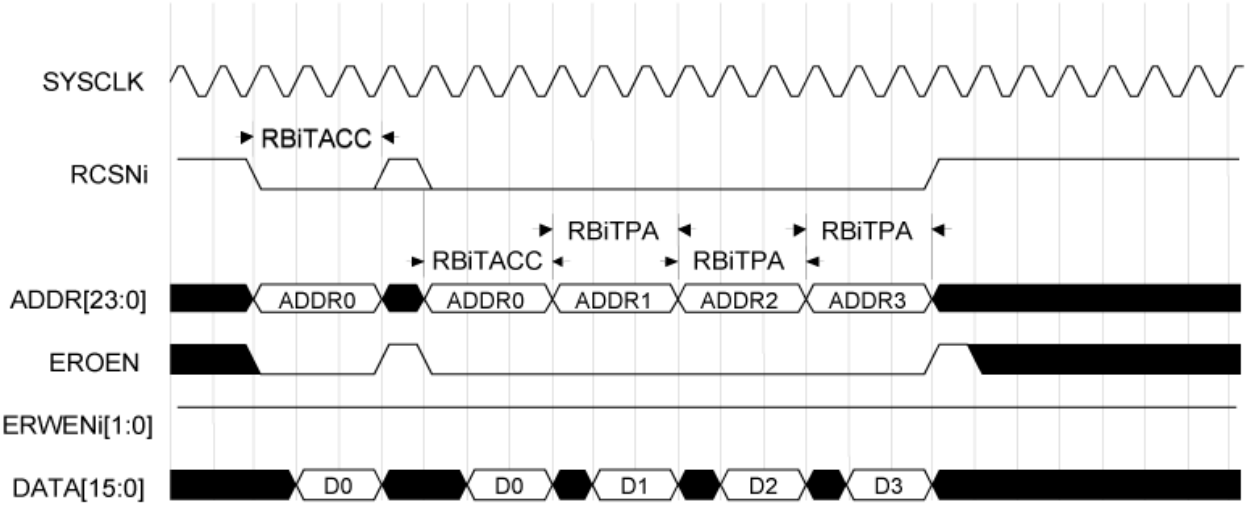


Figure 17. Static Memory Read Cycle

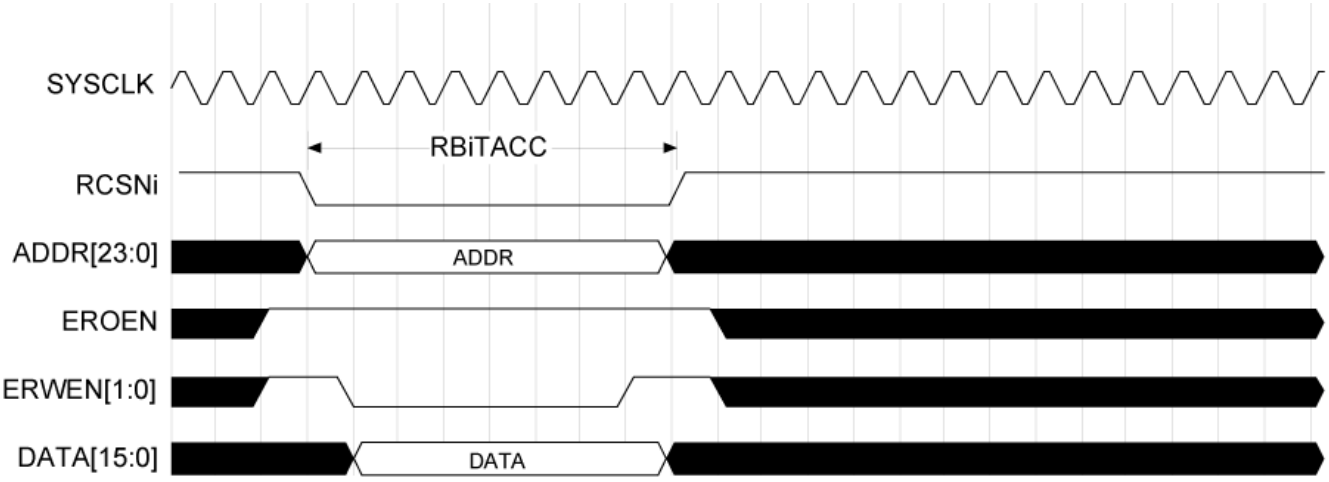


Figure 18. Static Memory Write Cycle

Symbol	Parameter[1]	Registers
RBiTACC	Programmable bank i access time	0x5010, 0x5014
RBiTPA	Programmable bank i page access time	0x5010, 0x5014

Table 2. Programmable Static Memory Timing Parameters

Note:

1. "i" Refers to chip select parameters 0 and 1.

Figure 19 provides external I/O ports interface timing.

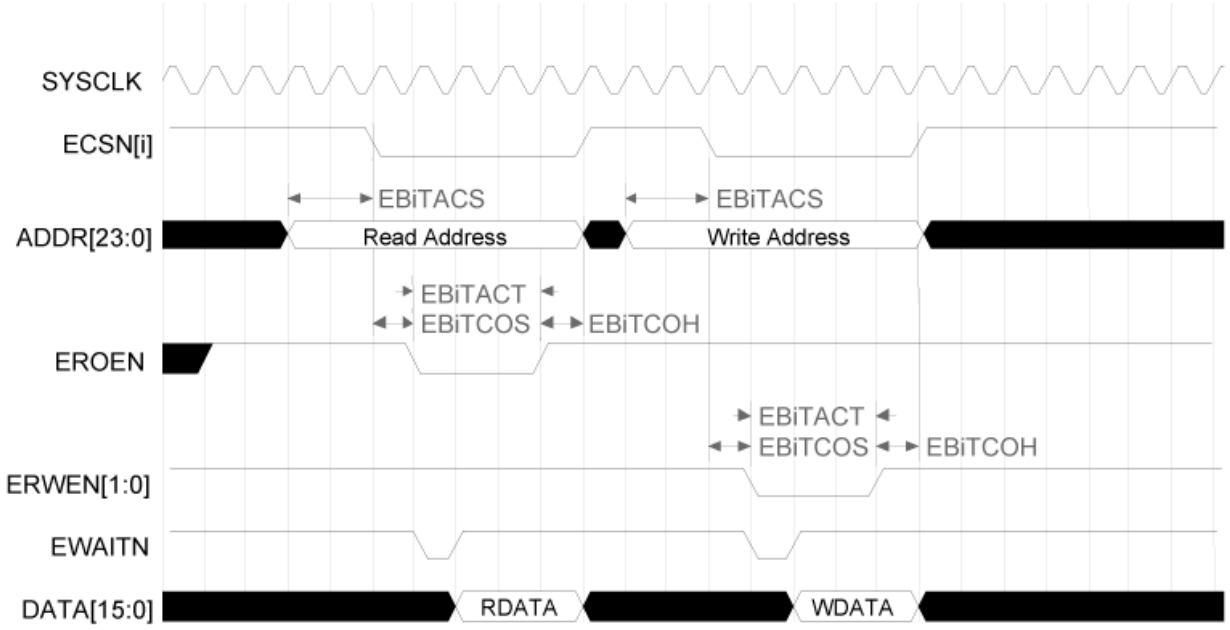
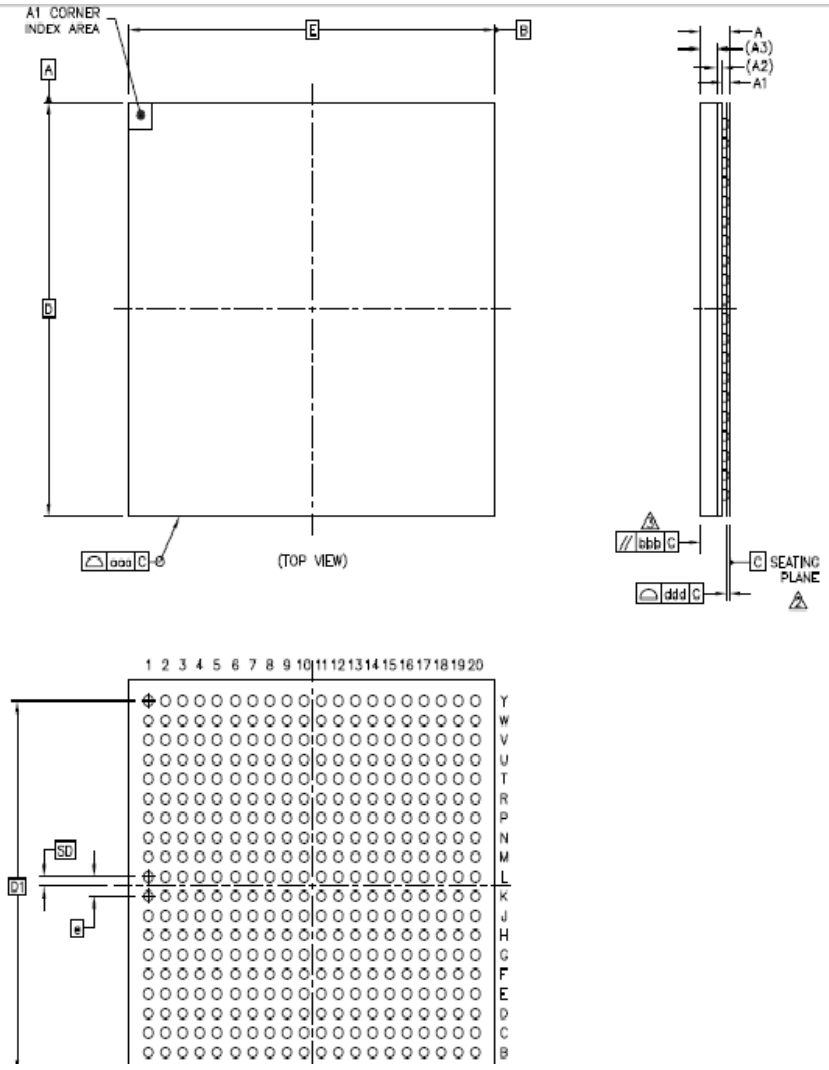


Figure 19. External I/O Read and Write Cycles



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.4
STAND OFF	A1	0.27	---	0.37
SUBSTRATE THICKNESS	A2		0.26	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		17	BSC
	E		17	BSC
BALL DIAMETER			0.4	
BALL OPENING			0.35	
BALL WIDTH	b	0.38	---	0.48
BALL PITCH	e		0.8	BSC
BALL COUNT	n		400	
EDGE BALL CENTER TO CENTER	D1		15.2	BSC
	E1		15.2	BSC
BODY CENTER TO CONTACT BALL	SD		0.4	BSC
	SE		0.4	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.12	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 22. KSZ9692PB-S 400-Pin PBGA (17X17X1.4 MM)

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