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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Networking and Communications
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	KSZ
RAM Size	-
Interface	EBI/EMI, Ethernet, I²C, I²S,PCI, SPI, UART/USART, USB
Number of I/O	20
Voltage - Supply	1.235V ~ 1.365V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	400-BGA
Supplier Device Package	400-PBGA (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ksz9692pbi

Revision History

Revision	Date	Summary of Changes
1.0	10/14/08	Initial Release
2.0	3/10/09	Power Sequencing, Added A1 (PMEN) to pin list, 1.3V Supply for Core, Power Consumption table
3.0	8/10/09	DDR Data Width Changed to 16-bit
4.0	01/28/10	DDR Data Width Changed to 32-bit
4.1	06/10/10	Remove NAND Boot support
5.0	04/14/11	Add small packet device KSZ9692PB-S
	09/13/11	Change the USB Port 0 to Port 2 in Figure 12 and 13. Change RSVD to DATA[31..16] in Figure 20.

Contents

System Level Applications

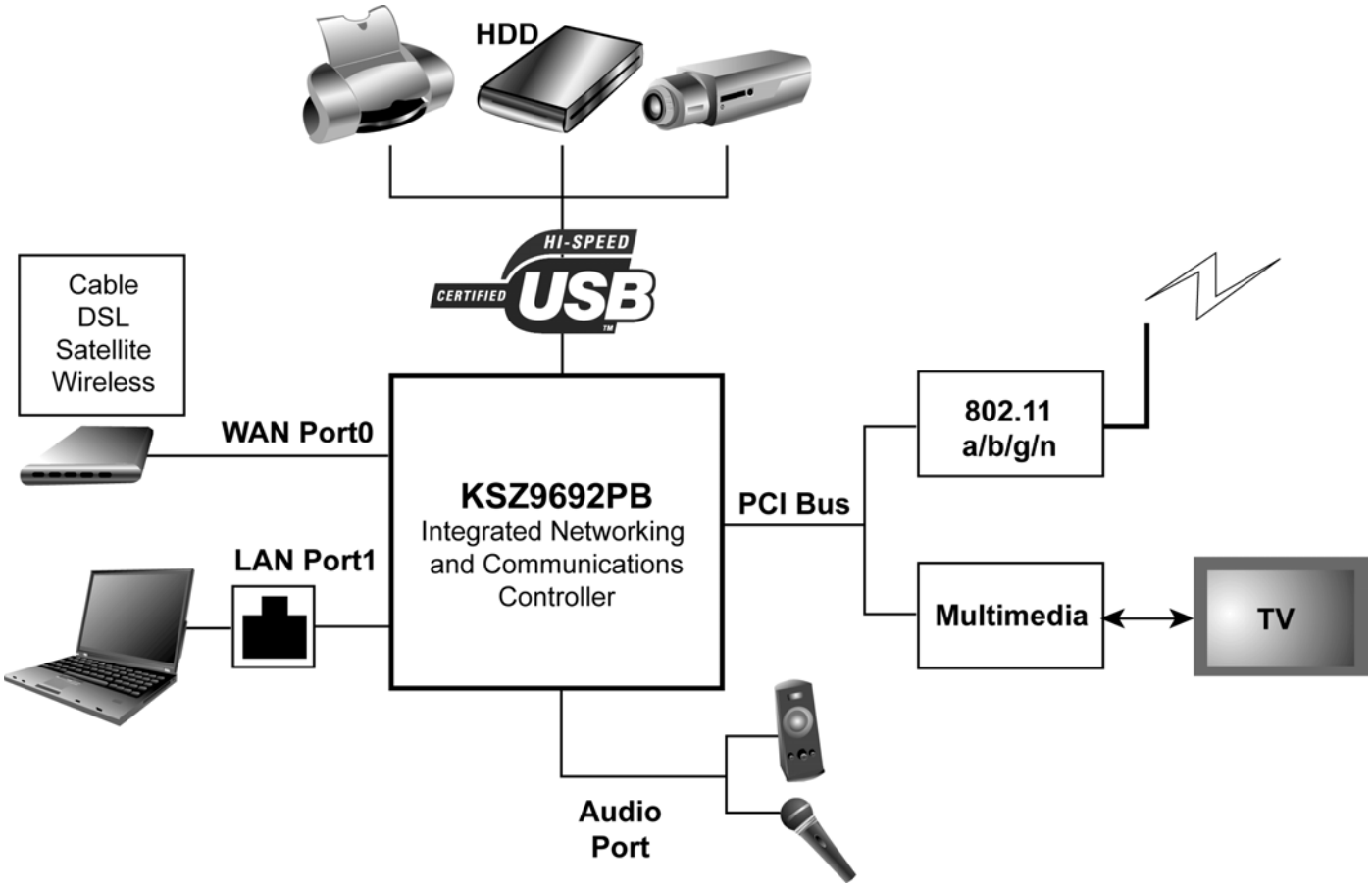


Figure 2. Peripheral Options and Examples

Pin Description: Signal Descriptions by Group

Pin Number	Pin Name	Pin Type	Pin Description
System Interface			
R5	RESETN	I	Reset, asserted Low. RESETN will force the KSZ9692PB, KSZ9692PB-S to reset ARM9 CPU and all functional blocks. Once asserted, RESETN must remain asserted for a minimum duration of 256 system clock cycles. When in the reset state, all the output pins are put into Tri-state and all open drain signals are floated.
N5	WRSTO	O	Watchdog Timer Reset Output When the Watchdog Timer expires, this signal will be asserted for at least 200 msec.
W1	XCLK2	I	System Clock Input 2. External crystal or clock input 2. The clock frequency should be 25MHz ± 50ppm.
Y1	XCLK1	I	System Clock Input 1. Used with XCLK1 pin when other polarity of crystal is needed. This is unused for a normal clock input.
H19	CLK25MHz	O	25MHz output to external PHY
Y15, Y14	DDCLKO[1:0]	O	DDR Clock Out [1:0]. Output of the internal system clock, it is also used as the clock signal for DDR interface.
W15, W14	DDCLKON[1:0]	O	The negative of differential pair of DDR Clock Out [1:0]. Output of the internal system clock, it is also used as the clock signal for DDR interface.
U13	SDCLKEO	O	Clock Enable output for SDRAM (for Power Down Mode)
T7, U7	VREF	I	Reference Voltage for SSTL interface. Must be half of the voltage for the DDR VDD supply. See EIA/JEDEC standard EIA/JESD8-9 (Stub series terminated logic for 2.5V, SSTL_2)
W3	SDOCLK	O	DDR Clock Out for loopback from De-skew PLL
Y3	SDICLK	I	DDR Clock In from loopback to De-skew PLL. This pin must connect to SDOCLK with appropriate de-skew length. See Engineering Evaluation Design Kit for detailed implementation.
Y17, Y16	DDCLKO[3:2]	O	Factory Reserved.
W17, W16	DDCLKON[3:2]	O	Factory Reserved.
NAND/SRAM/ROM/EXIO Interface			
L2, K1, K2, J3, H5, H4, J2, H3, J1, H2, G5, H1, G3, G4, G2, F1, G1, F2, F3, F5, F4, E1, E2, E3	SADDR[23..0]	O	SRAM Address Bus. The 24-bit address bus covers 16M word memory space of ROM/SRAM/FLASH, and 16M byte external I/O banks. This address bus is shared between ROM/SRAM/FLASH/EXTIO devices.

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
R3	NCLE	Ipd/O	NAND command Latch Enable NCLE controls the activating path for command sent to NAND flash.
U2	NALE	Ipd/O	NAND Address Latch Enable NALE controls the activating path for address sent to NAND flash.
T3	NCEN1	O	NAND Bank Chip Enable 1, asserted low NAND device bank 1 selection control.
V3	NCEN0	O	NAND Bank Chip Enable 0, asserted low NAND device bank 0 selection control.
R4	NREN	Ipu/O	NAND Read Enable, asserted low
T4	NWEN	Ipu/O	NAND Write Enable, asserted low
U3	NWPN	Ipu/O	NAND Write Protection, asserted low
P4, U4	NRBN[1:0]	I	NAND Ready/Busy, asserted low for busy.
DDR Interface			

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
T17, V18, U17, T16, W20, W19, Y20, Y19, W18, V17, U16, T15, Y18, V16	DADDR[13..0]	O	DDR Address Bus.
V13, U11, V12, W13, Y13, W12, V11, U10, V10, Y11, W10, U9, Y10, V9, W9, Y9, W8, Y8, Y7, W7, V7, Y6, W6, V6, Y5, V5, W5, U5, T5, Y4, V4, W4	DDATA[31..0]	I/O	DDR Data Bus.
T13, V14	BA[1:0]	O	DDR Bank Address.
U14	CSN	O	DDR Chip Select, asserted Low. Chip select pins for DDR, the KSZ9692PB, KSZ9692PB-S supports only one DDR bank.
T14	RASN	O	DDR Row Address Strobe, asserted Low. The Row Address Strobe pin for DDR.
U15	CASN	O	DDR Column Address Strobe, asserted Low. The Column Address Strobe pin for DDR.
V15	WEN	O	DDR Write Enable, asserted Low. The write enable signal for DDR.
U8, T6 T12,Y12	DM[3:0]	O	Data Input/Output mask signals for DDR. DM is sampled High and is an output mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a Write cycle. DM0 corresponds to DDATA[7:0], DM1 corresponds to DDATA[15:8], DM2 corresponds to DDATA[23:16] and DM3 corresponds to DDATA[31:24].
V8, U6 U12,W11	DQS[3:0]	I/O	DDR only Data Strobe Input with read data, output with write data. DQS0 corresponds to DDATA[7:0], DQS1 corresponds to DDATA[15:8].

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
Ethernet Port 0			
M16	P0_RXC	Ipd/O	MAC mode MII: input RX clock / PHY mode MII: output RX clock RGMII mode: input RX clock
P18, N17, P17, N16	P0_RXD[3:0]	I	RX data[3:0]
N18	P0_RXDV	I	MII mode: RX data valid RGMII mode: as RX_CTL. RXDV on rising edge of RXC, logic derivative of RXDV and RXER on falling edge of RXC
P19	P0_RXER	I	MII mode: RX error RGMII mode: input SEL
M17	P0_CRS	I	MAC mode MII: input carrier sense RGMII mode: not used
P20	P0_COL	I	MAC mode MII: input collision RGMII mode: not used
M18	P0_TXC	Ipd/O	MAC mode MII: input TX clock / PHY mode MII: output TX clock RGMII mode: output TX clock
L17, M19, N20, N19	P0_TXD[3:0]	O	TX data[3:0]
L16	P0_TXEN	O	MII: TX enable RGMII: as TX_CTL input. TXEN on rising edge of TXC, logic derivative of TXEN and TXER on falling edge of TXC.
Ethernet Port 1			
K19	P1_RXC	Ipd/O	MAC mode MII: input RX clock / PHY mode MII: output RX clock RGMII mode: input RX clock
L20, L19, L18, M20	P1_RXD[3:0]	I	RX data[3:0]
K16	P1_RXDV	I	MII mode: RX data valid RGMII mode: as RX_CTL. RXDV on rising edge of RXC, logic derivative of RXDV and RXER on falling edge of RXC
K17	P1_RXER	I	MII mode: RX error RGMII mode: input SEL
K18	P1_CRS	I	MAC mode MII: input carrier sense RGMII mode: not used
K20	P1_COL	I	MAC mode MII: input collision RGMII mode: not used
J17	P1_TXC	Ipd/O	MAC mode MII: input TX clock / PHY mode MII: output TX clock RGMII mode: output TX clock
H20, J19, J18, J20	P1_TXD[3:0]	O	TX data[3:0] output.
J16	P1_TXEN	O	MII: TX enable RGMII: as TX_CTL input. TXEN on rising edge of TXC, logic derivative of TXEN and TXER on falling edge of TXC.

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
USB Interface			
G19	U1P	I/O (analog)	USB port 1 differential + signal
G20	U1M	I/O (analog)	USB port 1 differential - signal
F19	U2P	I/O (analog)	USB port 2 differential + signal
F20	U2M	I/O (analog)	USB port 2 differential - signal
G17	USBXI	I (analog)	Crystal in for USB PLL
G18	USBXO	O (analog)	Crystal out for USB PLL
H16	USBREXT	I (analog)	Connect to an external resistor 3.4K ohm to GND
G16	USBTEST	O (Analog)	USB analog test output (factory reserved)
G15	USBCFG	I	USB port 2 configuration "1" = port 2 is host "0" = port 2 is device (port 1 is always host)
F18	USBHOVC0	I	Over current sensing input for Host Controller downstream port 1.
F15	USBHOVC1	I	Over current sensing input for Host Controller downstream port 2.
F17	USBHPWR0	Ipu/O (open drain)	Power switching control output for downstream port 1; open drain output.
F16	USBHPWR1	Ipu/O (open drain)	Power switching control output for downstream port 2; open drain output.
SDIO Interface			
D14	KCMD	Ipd/O	SD 4-bit mode: Command line SD 1-bit mode: Command line
C18	KCLK	Ipd/O	SDIO/SD Clock
C15	KDATA3	I/O	SD 4-bit mode : data line 3 SD 1-bit mode : not used
C16	KDATA2	I/O	SD 4-bit mode : data line 2 or read wait (optional) SD 1-bit mode : read wait (optional)
E13	KDATA1	I/O	SD 4-bit mode : data line 1 or interrupt (optional) SD 1-bit mode : interrupt
C17	KDATA0	I/O	SD 4-bit mode : data line 0 SD 1-bit mode : data line
C14	KSDCDN	I	Active low used for Card Detection

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
TAP Control Signals			
A18	TCK	I	JTAG Test Clock
A17	TMS	I	JTAG Test Mode Select
A16	TDI	I	JTAG Test Data In
A15	TDO	O	JTAG Test Data Out
A14	TRSTN	I	JTAG Test Reset, asserted Low
Test Signals			
P5	SCANEN	Ipd	1 = Scan Enable (Factory reserved) 0 = Normal Operation
V2	TESTEN	Ipd	1 = Test Enable (Factory reserved) 0 = Normal Operation
V1	TESTEN1	Ipd	1 = Test Enable1 (Factory reserved) 0 = Normal Operation
Y2	TEST1	O (analog)	Factory reserved
W2	TEST2	O (analog)	Factory reserved
Power and Ground (96)			
N6, M6, M7, G7, G8, G9, M14, M15, N14, P11, P12, P13, P14	VDD1.2	P	Digital power supply 1.3V (13)
G6, H6, J6, K6, F7, F8, F9, F10, F11, G10, G11, H14, J14, K14, K15, L15	VDD3.3	P	Digital power supply 3.3V (16)
R6, R7, R8, R9, R10, R11, R12, R13, R14, T8, T9, T10, T11	VDD2.5	P	DDR Pad Driver 2.5V or 2.6V Power Supply. (13)
H7, H8, H9, H10, H11, J7, J8, J9, J10, J11, K7, K8, K9, K10, K11, K12, L7, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, N9, N10, N11, N12, N13, P7, P8, P9, P10	GND	GROUND	Digital Ground. (37)

Pin Description: Signal Descriptions by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
L6	PLLVDDA3.3	P	Band Gap Reference Analog Power. (1)
M8	PLLVSSA3.3	GROUND	Band Gap Reference Analog Ground. (1)
P6	PLLDVDD1.2	P	De-skew PLL Analog and Digital Power. (1)
M5	PLLSVDD1.2	P	System PLL Analog and Digital Power. (1)
N7, N8	PLLVSS1.2	GROUND	De-skew PLL and System PLL Ground. (2)
L8	PLLVSSISO	GROUND	Ground Isolation PLL and other circuit. (1)
G12	USB1VDDA3.3	P	Analog Power for USB Channel 1. (1)
G13	USBCVDDA3.3	P	Analog Power for Common Circuit of USB Channel 1 and 2. (1)
G14	USB2VDDA3.3	P	Analog Power for USB Channel 2. (1)
H13, J13, K13	USBVSSA3.3	GROUND	Analog Ground for both USB Channels Analog Circuit. (3)
J15	USB1VDD1.2	P	Digital Power for USB Channel 1 Controller. (1)
H15	USB2VDD1.2	P	Digital Power for USB Channel 2 Controller. (1)
J12	USBVSS1	GROUND	Digital Ground for USB Channel 1 Controller. (1)
H12	USBVSS2	GROUND	Digital Ground for USB Channel 2 Controller. (1)

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   O/I = Output in normal mode; input pin during reset.
   Ipu = Internal 55kΩ pull-up resistor.
   Ipd = Internal 55kΩ pull-down resistor.

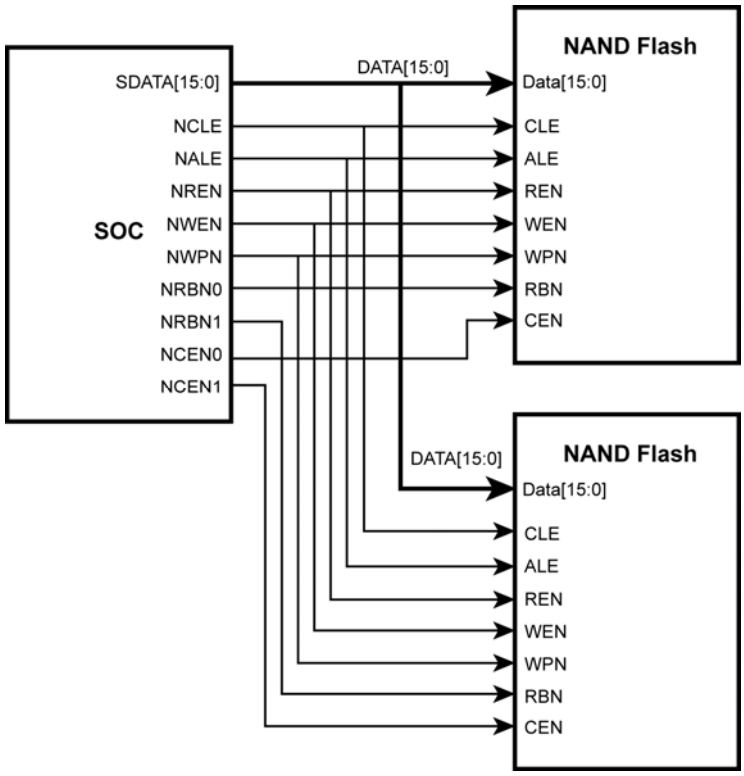


Figure 7. 16-bit NAND Interface Examples

DDR Controller

The KSZ9692PB, KSZ9692PB-S DDR memory controller provides interface for accessing external Double Data Rate Synchronous DRAM. In addition the KSZ9692PB, KSZ9692PB-S provides two integrated DDR differential clock drivers for a complete glueless DDR interface solution.

- Up to 200 MHz clock frequency (400 MHz data rate)
- Supports one 32-bit data width bank (16-bit optional)
- Up to 128MB of addressable space is available with 12 columns and 14 row address lines
- Supports all DDR device densities up to 1Gb
- Supports all DDR device data width x8 and x16
- Configurable DDR RAS and CAS timing parameters
- Two integrated JEDEC Specification JESD82-1 compliant differential clock drivers for a glueless DDR interface solution
- JEDEC Specification SSTL_2 I/Os

SDIO/SD Host Controller

Integrated SDIO/SD host controller provides interface for removable mass storage memory card and I/O devices.

- Meets SD Host Controller Standard Specification Version 1.0
- Meets SD memory card spec 1.01. MMC spec 3.31
- Meets SDIO card specification version 1.0
- 1or 4 bit mode supported
- Card detection-insertion/removal
- Line Status LED driver
- Password protection of cards
- Supports read wait control, suspend/resume operation
- Support multi block read and write
- Up to 12.5 Mbytes per second read and write rates using 4 parallel line for full speed card.
- Dedicated DMA or programmed I/O data transfer

IP Security Engine

Integrated hardware security engine performs complex encryption, decryption and authentication tasks with minimum ARM processor intervention to peak line rate of 100Mbps.

- ESP, AH mode
- Transport mode
- Tunnel mode
- IPv4
- Extended Sequence Numbers
- Data Descriptor Table (DDT)based packet memory
- AES-ECB/CBC; 128/192/256-bit keys
- DES/3DES-ECB/CBC
- RC4; 40/128 bit keys
- MD5, SHA-1, SHA-256
- HMAC-MD5
- HMAC-SHA1
- HMAC-SHA-256
- SSLMAC SHA-1
- SSLMAC MD5
- Dedicated DMA channel

USB 2.0 Interface

Integrated dual USB 2.0 interface can be configured as 2-port host, or host + device. Figures 12 and 13 illustrate examples of USB 2.0 interface applications.

- Compliant with USB Specification Revision 2.0
- Compliant with Open Host Controller Interface (OHCI) Specification Rev 1.0a
- Compliant with Enhanced Host Controller Interface (EHCI) Specification Rev 1.0
- Root hub with 2 (max) downstream facing ports which are shared by OHCI and EHCI host controller cores
- All downstream facing ports can handle High-Speed (480Mbps), Full-Speed (12Mbps), and Low-Speed (1.5Mbps) transaction
- OTG not supported
- Integrated 45-ohm termination, 1.5K pull-up and 15K pull-down resistors
- Support endpoint zero, and up to 6 configurable endpoints (IN/OUT, isochronous/ control/ interrupt/ bulk)
- One isochronous endpoint (IN or OUT)
- Dedicated DMA Channel for each port

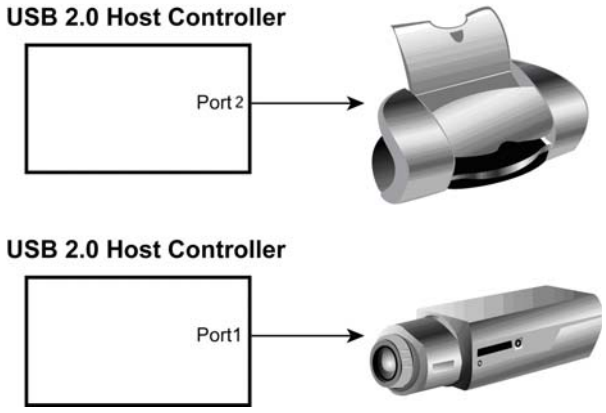


Figure 12. USB 2.0 Configuration as Two-Port Host

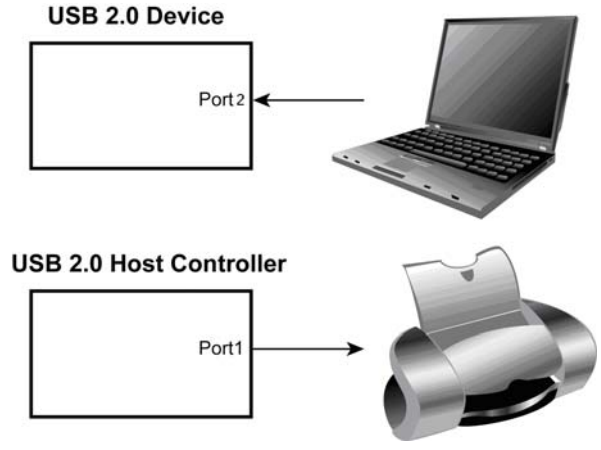


Figure 13. USB 2.0 Configuration as Host + Device

frame's destination.

If the network controller scans a frame and does not find the specific sequence shown above, it discards the frame and takes no further action. If the KSZ9692PB, KSZ9692PB-S controller detects the data sequence, however, it then alerts the device's power management circuitry to wake up the system.

IPv6 Support

The KSZ9692PB, KSZ9692PB-S provides the following IPv6 support in the hardware:

- Generates the checksum for IPv6 TCP/UDP packets based on register configuration (LAN MAC DMA Transmit Control Register and WAN MAC DMA Transmit Control Register) or Transmit Descriptor 1 (TDES1). The register setting is static configuration and the TDES1 setting is packet based configuration.
- Filters IPv6 packets with TCP/UDP errors (LAN MAC DMA Receive Control Register and WAN MAC DMA Receive Control Register).
- Supports up to 8 Source IP or Destination IP based filtering (LAN/WAN Access Control List)

Refer to the Register Description Document for more details.

DMA Controller

Integrated DMA controller connects data port of IP Security Engine, two Gb Ethernet MACs, two USB 2.0 ports, PCI 2.3 bus interface, and SDIO interface via dedicated channels to DDR memory controller for moving large amounts of data without significant ARM processor intervention. A typical DMA channel usage is to move data from these interfaces into DDR memory. The data in the memory is processed by the ARM processor and driven back by the DMA channel to the external interface. Additionally, the ARM processor itself has a dedicated DMA channel to access the DDR memory controller. Flash/ROM/SRAM, NAND controller, and peripherals do not have dedicated DMA channel and therefore depend on the ARM processor for transfer of data to DDR memory. DMA channel interfaces are shown in the functional block diagram on page 7.

The arbitration of all requests from DMA channels are handled by the DDR memory controller and pipelined for best performance. The memory controller supports programmable bandwidth allocation for each DMA channel, thus enabling the designer to optimize I/O resource utilization of memory.

UART Interface

The KSZ9692PB, KSZ9692PB-S support four independent high-speed UARTs; UART1, UART2, UART3 and UART4. The UART ports enhance the system availability for legacy serial communication application and console port display.

UART1, UART2, UART3 and UART4 support maximum baud rate of 5 Mbps including standard rates. The higher rates allow for Bluetooth and GSM applications.

UART1 supports CTSN, DSRN, DCDN modem control pins in addition to RXD and TXD data pins. For UART2, UART3, UART4 only CTSN and RTSN control pins in addition to RXD and TXD data pins are supported.

Timers and Watchdog

Two programmable 32-bit timers with one capable of watchdog timer function. These timers can operate in a very flexible way. The host can control the timeout period as well as the pulse duration. Both timers can be enabled with interrupt capability. When the watchdog timer is programmed and the timer setting expires, the KSZ9692PB, KSZ9692PB-S resets itself and also asserts WRSTO to reset other devices in the system.

GPIO

Twenty general purpose I/O (GPIO) are individually programmable as input or output. Some GPIO ports are programmable for alternate function as listed below:

- Four GPIO programmable as inputs for external interrupts
- Two GPIO programmable as 32-bit timers output
- Six GPIO programmable as CTSN and RTSN control pins for UART2, UART3, UART4
- One GPIO programmable as SDIO Line Status LED driver
- One GPIO programmable as ARM CPU interrupt line activity.

See Signal Description list for detailed GPIO map.

Timing Specifications

Figure 16 provides power sequencing requirement with respect to system reset.

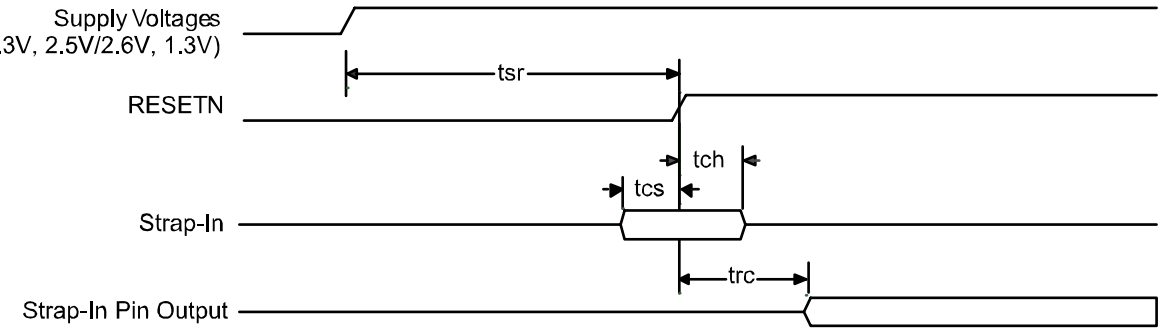


Figure 16. Reset Timing

Note: Power sequencing of supply voltages must be in order of 3.3V first, 2.5V/2.6V next and 1.3V last.

Symbol	Parameter	Min	Typ	Max	Units
t_{SR}	Stable supply voltages to reset high	10			ms
t_{CS}	Configuration set-up time	50			ns
t_{CH}	Configuration hold time	50			ns
t_{RC}	Reset to strap-in pin output	50			ns

Table 1. Reset Timing Parameters

Figure 17 and Figure 18 provide NOR FLASH, ROM and SRAM interface timing.

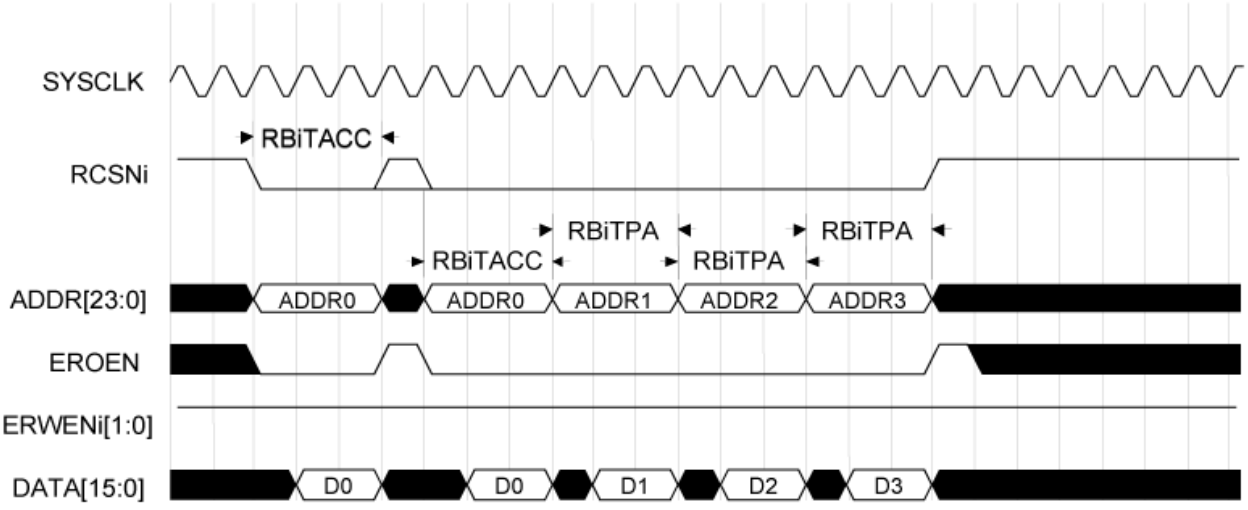


Figure 17. Static Memory Read Cycle

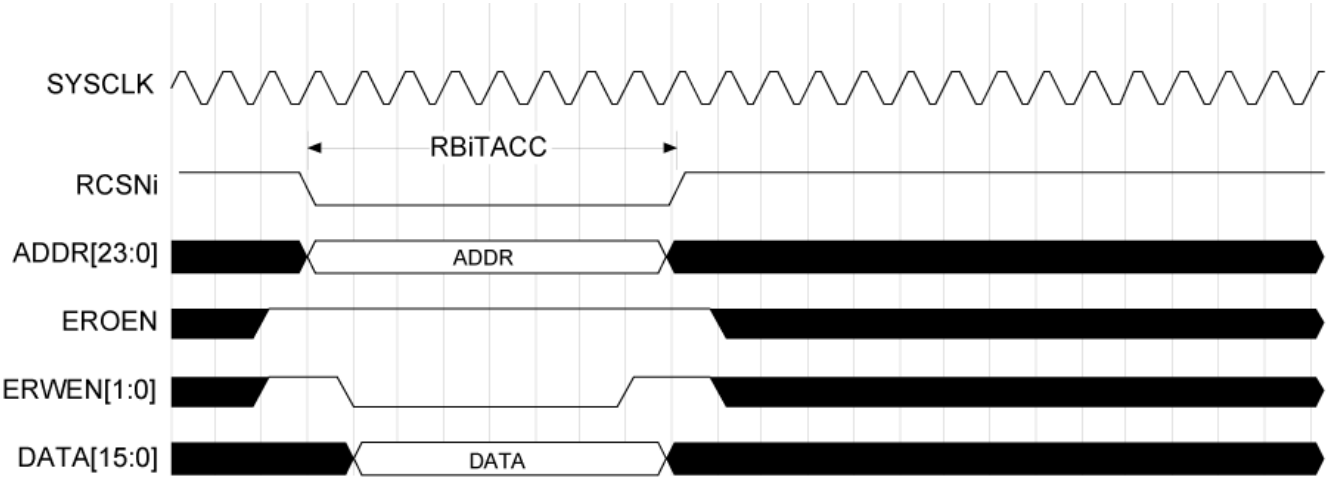


Figure 18. Static Memory Write Cycle

Symbol	Parameter[1]	Registers
RBiTACC	Programmable bank i access time	0x5010, 0x5014
RBiTPA	Programmable bank i page access time	0x5010, 0x5014

Table 2. Programmable Static Memory Timing Parameters

Note:

1. "i" Refers to chip select parameters 0 and 1.

Figure 19 provides external I/O ports interface timing.

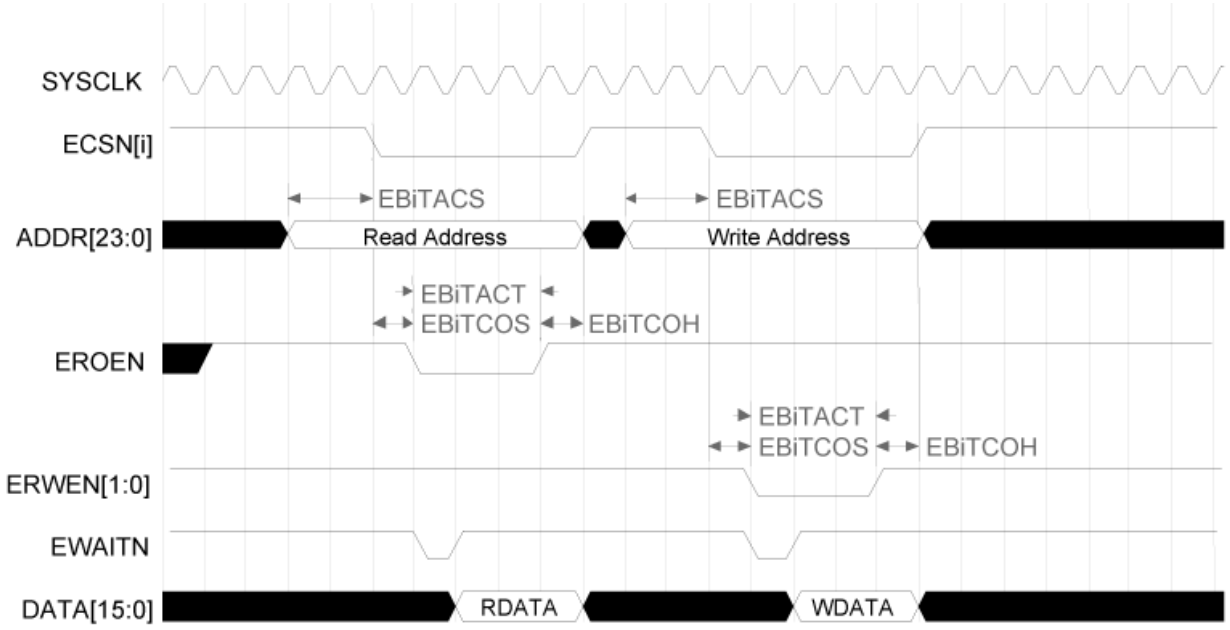


Figure 19. External I/O Read and Write Cycles

Symbol	Parameter	Min[1]	Typ[1]	Max[1]	Units
T_{cta}	Valid address to CS setup time	EBiTACS +0.8	EBiTACS +1.1	EBiTACS +1.3	ns
T_{cos}	OE valid to CS setup time	EBiTCOS +0.6	EBiTCOS +0.6	EBiTCOS +1.0	ns
T_{dsu}	Valid read data to OE setup time	2.0			ns
T_{cws}	WE valid to CS setup time	EBiTCOS +0.6	EBiTCOS +0.6	EBiTCOS +1.0	ns
T_{dh}	Write data to CS hold time	0			ns
T_{cah}	Address to CS hold time	EBiTCOH +1.0	EBiTCOH +1.0	EBiTCOH +1.4	ns
T_{oew}	OE/WE pulsewidth	EBiTACT		EBiTACT	ns
T_{ocs}, T_{csw}	Rising edge CS to OE/WE hold time	0			ns

Table 3. External I/O Memory Timing Parameters

Note:

1. Measurements for minimum were taken at 0°C, typical at 25°C, and maximum at 100°C.

Symbol	Parameter[1]	Registers
EBiTACS	Programmable bank i address setup time before chip select	0x5000, 0x5004, 0x5008
EBiTACT	Programmable bank i write enable/output enable access time	0x5000, 0x5004, 0x5008
EBiTCOS	Programmable bank i chip select setup time before OEN	0x5000, 0x5004, 0x5008
EBiTCOH	Programmable bank i chip select hold time	0x5000, 0x5004, 0x5008

Table 4. Programmable External I/O Timing Parameters

Note:

1. "i" Refers to chip select parameters 0, 1, or 2.

Package Information

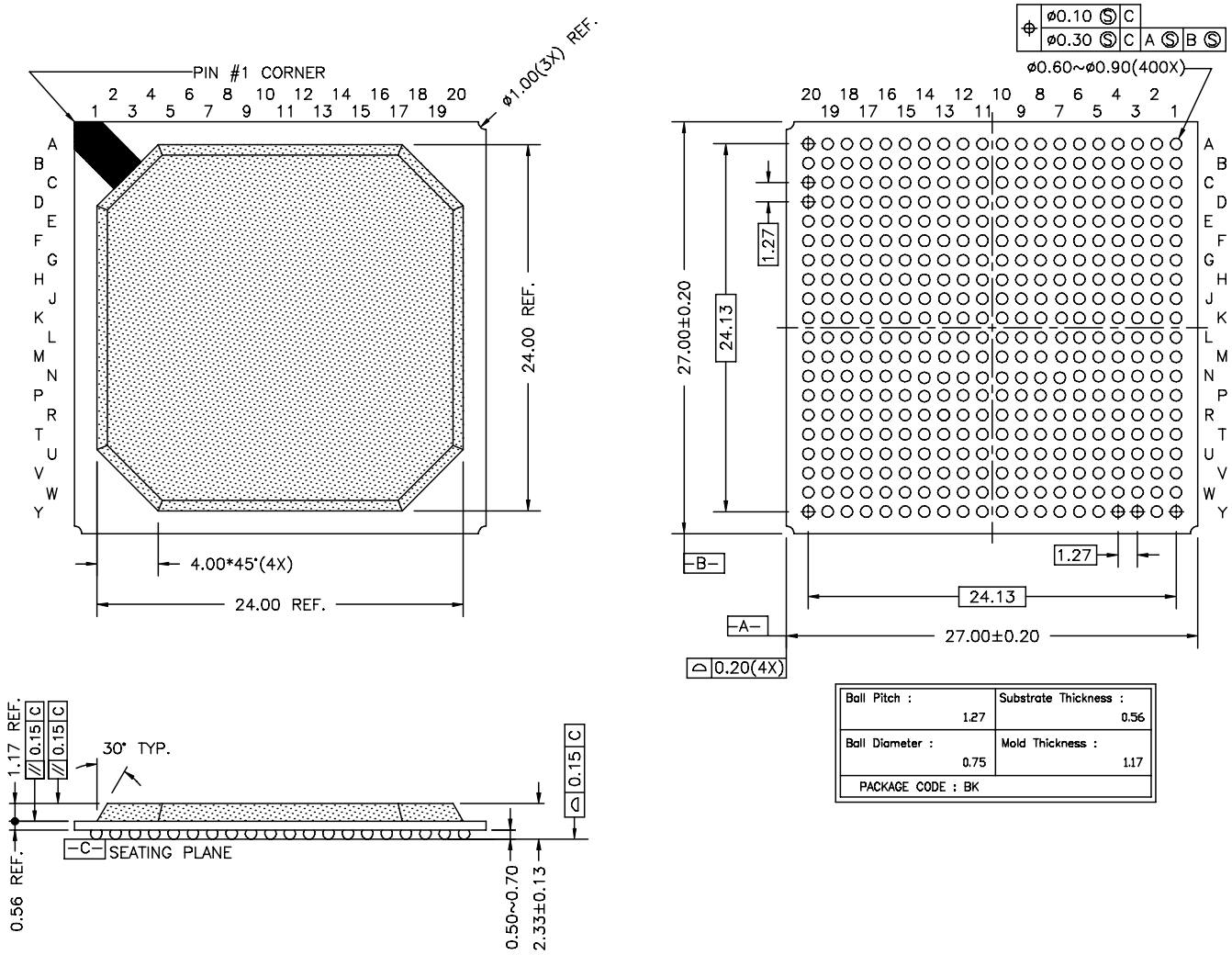
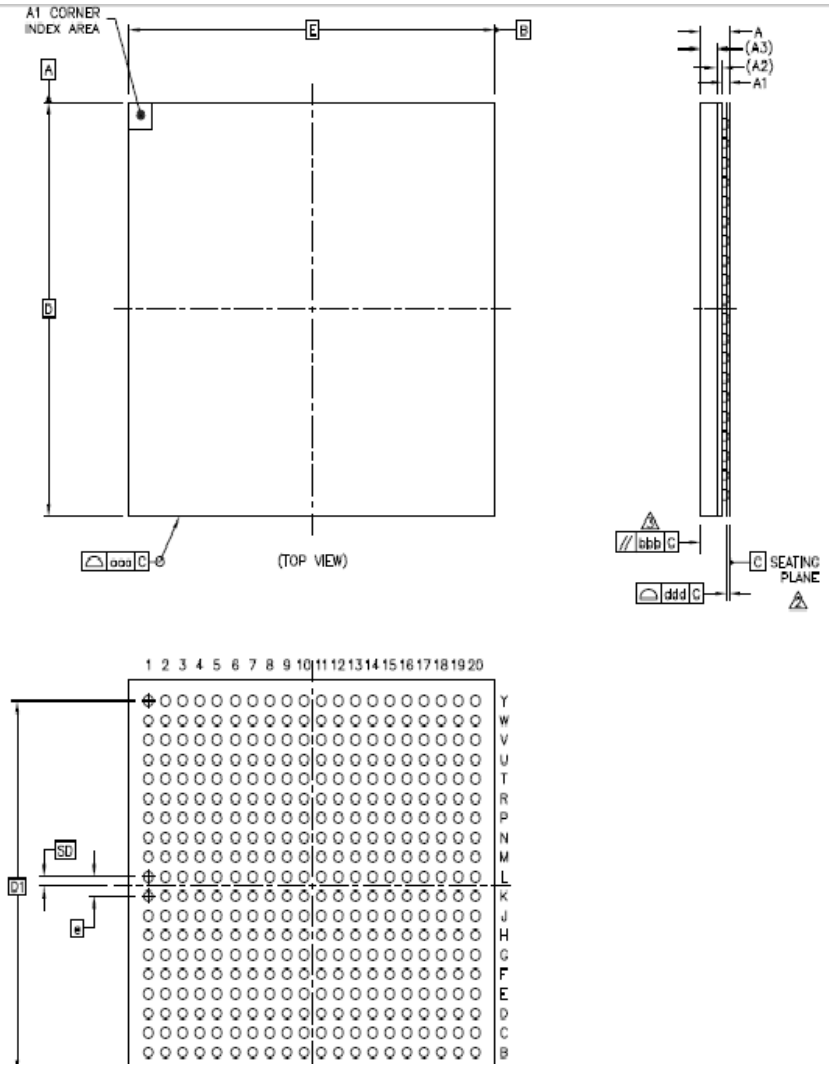


Figure 21. KSZ9692PB 400-Pin PBGA (24X24X2.33 MM)



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.4
STAND OFF	A1	0.27	---	0.37
SUBSTRATE THICKNESS	A2		0.26	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		17	BSC
	E		17	BSC
BALL DIAMETER			0.4	
BALL OPENING			0.35	
BALL WIDTH	b	0.38	---	0.48
BALL PITCH	e		0.8	BSC
BALL COUNT	n		400	
EDGE BALL CENTER TO CENTER	D1		15.2	BSC
	E1		15.2	BSC
BODY CENTER TO CONTACT BALL	SD		0.4	BSC
	SE		0.4	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.12	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 22. KSZ9692PB-S 400-Pin PBGA (17X17X1.4 MM)

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