# E · ) (Lattice Semiconductor Corporation - <u>LCMXO2-1200HC-4TG100IR1 Datasheet</u>



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	79
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-1200hc-4tg100ir1

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# Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), preengineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I<sup>2</sup>C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external V<sub>CC</sub> supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external V<sub>CC</sub> supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pulldown and bus-keeper features are controllable on a "per-pin" basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I<sup>2</sup>C port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE<sup>™</sup> modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.



### **Output Register Block**

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

### Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-14 shows the output register block on the left, top and bottom edges.

Figure 2-14. MachXO2 Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)



### **Right Edge**

The output register block on the right edge is a superset of the output register on left, top and bottom edges of the device. In addition to supporting SDR and Generic DDR modes, the output register blocks for PIOs on the right edge include additional logic to support DDR-memory interfaces. Operation of this block is similar to that of the output register block on other edges.

In DDR memory mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the DQSW90 signal is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-15 shows the output register block on the right edge.



More information on the input gearbox is available in TN1203, Implementing High-Speed Interfaces with MachXO2 Devices.

## **Output Gearbox**

Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDRX4 (8:1) gearbox or as two ODDRX2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

### Table 2-10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]		
GDDRX4(8:1): D[7:0]		
GDDRX2(4:1)(IOL-A): D[3:0]		
GDDRX2(4:1)(IOL-C): D[7:4]		
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-17 shows the output gearbox block diagram.



MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 devices contain three types of sysIO buffer pairs.

### 1. Left and Right sysIO Buffer Pairs

The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential and referenced input buffers.

### 2. Bottom sysIO Buffer Pairs

The sysIO buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential and referenced input buffers. Only the I/Os on the bottom banks have programmable PCI clamps and differential input termination. The PCI clamp is enabled after  $V_{CC}$  and  $V_{CCIO}$  are at valid operating levels and the device has been configured.

### 3. Top sysIO Buffer Pairs

The sysIO buffer pairs in the top bank of the device consist of two single-ended output drivers and two singleended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential and referenced I/O buffers. Half of the sysIO buffer pairs on the top edge have true differential outputs. The sysIO buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver. The referenced input buffer can also be configured as a differential input buffer.

### Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when  $V_{CC}$  and  $V_{CCIO0}$  have reached  $V_{PORUP}$  level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all  $V_{CCIO}$  banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pulldown to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to  $V_{CCIO}$  as the default functionality). The I/O pins will maintain the blank configuration until  $V_{CC}$  and  $V_{CCIO}$  (for I/O banks containing configuration I/Os) have reached  $V_{PORUP}$  levels at which time the I/Os will take on the user-configured settings only after a proper download/configuration.

### **Supported Standards**

The MachXO2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL, and PCI. The buffer supports the LVTTL, PCI, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO2-640U, MachXO2-1200/U and higher devices support on-chip LVDS output buffers on approximately 50% of the I/Os on the top bank. Differential receivers for LVDS, BLVDS, MLVDS and LVPECL are supported on all banks of MachXO2 devices. PCI support is provided in the bottom bank of theMachXO2-640U, MachXO2-1200/U and higher density devices. Table 2-11 summarizes the I/O characteristics of the MachXO2 PLDs.

Tables 2-11 and 2-12 show the I/O standards (together with their supply and reference voltages) supported by the MachXO2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1202, MachXO2 sysIO Usage Guide.



#### Table 2-13. Supported Output Standards

Output Standard	V <sub>CCIO</sub> (Typ.)			
Single-Ended Interfaces				
LVTTL	3.3			
LVCMOS33	3.3			
LVCMOS25	2.5			
LVCMOS18	1.8			
LVCMOS15	1.5			
LVCMOS12	1.2			
LVCMOS33, Open Drain	—			
LVCMOS25, Open Drain	—			
LVCMOS18, Open Drain	—			
LVCMOS15, Open Drain	—			
LVCMOS12, Open Drain	—			
PCI33	3.3			
SSTL25 (Class I)	2.5			
SSTL18 (Class I)	1.8			
HSTL18(Class I)	1.8			
Differential Interfaces				
LVDS <sup>1, 2</sup>	2.5, 3.3			
BLVDS, MLVDS, RSDS <sup>2</sup>	2.5			
LVPECL <sup>2</sup>	3.3			
MIPI <sup>2</sup>	2.5			
Differential SSTL18	1.8			
Differential SSTL25	2.5			
Differential HSTL18	1.8			

1. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers. 2. These interfaces can be emulated with external resistors in all devices.

### sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO2-1200U, MachXO2-2000/U and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO2-1200 and lower density devices have four banks (one bank per side). Figures 2-18 and 2-19 show the sysIO banks and their associated supplies for all devices.



Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe $V_{CC}$ drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1198, Power Estimation and Management for MachXO2 Devices.

## Power On Reset

MachXO2 devices have power-on reset circuitry to monitor  $V_{CCINT}$  and  $V_{CCIO}$  voltage levels during power-up and operation. At power-up, the POR circuitry monitors  $V_{CCINT}$  and  $V_{CCIO0}$  (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the  $V_{PORUP}$  level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices),  $V_{CCINT}$  is the same as the  $V_{CC}$  supply voltage. For devices with voltage regulators (HC devices),  $V_{CCINT}$  is regulated from the  $V_{CC}$  supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time (t<sub>REFRESH</sub>) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tristate. I/Os are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external  $V_{CC}$  voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor  $V_{CCINT}$  levels. If  $V_{CCINT}$  drops below  $V_{PORDNBG}$  level (with the bandgap circuitry switched on) or below  $V_{PORDNSRAM}$  level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the  $V_{CCINT}$  and  $V_{CCIO}$  voltage levels.  $V_{PORDNBG}$  and  $V_{PORDNSRAM}$  are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the  $V_{PORDNSRAM}$  reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the  $V_{CC}$  supply dropping below  $V_{CC}$  (min) they should not shut down the bandgap or POR circuit.



When implementing background programming of the on-chip Flash, care must be taken for the operation of the PLL. For devices that have two PLLs (XO2-2000U, -4000 and -7000), the system must put the RPLL (Right-side PLL) in reset state during the background Flash programming. More detailed description can be found in TN1204, MachXO2 Programming and Configuration Usage Guide.

#### Security and One-Time Programmable Mode (OTP)

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO2 devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile Flash memory spaces. The device can be in one of two modes:

- 1. Unlocked Readback of the SRAM configuration and non-volatile Flash memory spaces is allowed.
- 2. Permanently Locked The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash and SRAM OTP portions of the device. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

#### Dual Boot

MachXO2 devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the on-chip Flash. The golden image MUST reside in an external SPI Flash. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

#### Soft Error Detection

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1206, MachXO2 Soft Error Detection Usage Guide.

### TraceID

Each MachXO2 device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I<sup>2</sup>C, or JTAG interfaces.

## **Density Shifting**

The MachXO2 family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO2 migration files.



# Static Supply Current – HC/HE Devices<sup>1, 2, 3, 6</sup>

Symbol	Parameter	Device	Typ. <sup>4</sup>	Units
	Core Power Supply	LCMXO2-256HC	1.15	mA
		LCMXO2-640HC	1.84	mA
		LCMXO2-640UHC	3.48	mA
		LCMXO2-1200HC	3.49	mA
		LCMXO2-1200UHC	4.80	mA
1		LCMXO2-2000HC	4.80	mA
ICC		LCMXO2-2000UHC	8.44	mA
		LCMXO2-4000HC	8.45	mA
		LCMXO2-7000HC	12.87	mA
		LCMXO2-2000HE	1.39	mA
		LCMXO2-4000HE	2.55	mA
		LCMXO2-7000HE	4.06	mA
I <sub>CCIO</sub>	Bank Power Supply <sup>5</sup> $V_{CCIO} = 2.5 V$	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.

2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V<sub>CCIO</sub> or GND, on-chip oscillator is off, on-chip PLL is off.

3. Frequency = 0 MHz.

4.  $T_J = 25$  °C, power supplies at nominal voltage.

5. Does not include pull-up/pull-down.

6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

# Programming and Erase Flash Supply Current – HC/HE Devices<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Device	Typ.⁵	Units
		LCMXO2-256HC	14.6	mA
		LCMXO2-640HC	16.1	mA
		LCMXO2-640UHC	18.8	mA
		LCMXO2-1200HC	18.8	mA
		LCMXO2-1200UHC	22.1	mA
I <sub>CC</sub>		LCMXO2-2000HC	22.1	mA
	Core Power Supply	LCMXO2-2000UHC	26.8	mA
		LCMXO2-4000HC	26.8	mA
		LCMXO2-7000HC	33.2	mA
		LCMXO2-2000HE	18.3	mA
		LCMXO2-2000UHE	20.4	mA
		LCMXO2-4000HE	20.4	mA
		LCMXO2-7000HE	23.9	mA
I <sub>CCIO</sub>	Bank Power Supply <sup>6</sup>	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.

2. Assumes all inputs are held at  $V_{CCIO}$  or GND and all outputs are tri-stated.

3. Typical user pattern.

4. JTAG programming is at 25 MHz.

5.  $T_J = 25$  °C, power supplies at nominal voltage.

6. Per bank.  $V_{CCIO} = 2.5$  V. Does not include pull-up/pull-down.



# Programming and Erase Flash Supply Current – ZE Devices<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Device	Typ.⁵	Units
I <sub>CC</sub>	Core Power Supply	LCMXO2-256ZE	13	mA
		LCMXO2-640ZE	14	mA
		LCMXO2-1200ZE	15	mA
		LCMXO2-2000ZE	17	mA
		LCMXO2-4000ZE	18	mA
		LCMXO2-7000ZE	20	mA
I <sub>CCIO</sub>	Bank Power Supply <sup>6</sup>	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.

2. Assumes all inputs are held at  $V_{\mbox{CCIO}}$  or GND and all outputs are tri-stated.

3. Typical user pattern.

4. JTAG programming is at 25 MHz.

5. TJ = 25 °C, power supplies at nominal voltage.

6. Per bank.  $V_{CCIO}$  = 2.5 V. Does not include pull-up/pull-down.



### LVDS Emulation

MachXO2 devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.





Note: All resistors are ±1%.

### Table 3-1. LVDS25E DC Conditions

#### **Over Recommended Operating Conditions**

Parameter	Description	Тур.	Units
Z <sub>OUT</sub>	Output impedance	20	Ohms
R <sub>S</sub>	Driver series resistor	158	Ohms
R <sub>P</sub>	Driver parallel resistor	140	Ohms
R <sub>T</sub>	Receiver termination	100	Ohms
V <sub>OH</sub>	Output high voltage	1.43	V
V <sub>OL</sub>	Output low voltage	1.07	V
V <sub>OD</sub>	Output differential voltage	0.35	V
V <sub>CM</sub>	Output common mode voltage	1.25	V
Z <sub>BACK</sub>	Back impedance	100.5	Ohms
I <sub>DC</sub>	DC output current	6.03	mA



### BLVDS

The MachXO2 family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

### Figure 3-2. BLVDS Multi-point Output Example



### Table 3-2. BLVDS DC Conditions<sup>1</sup>

Over Recommended	Operating	Conditions
	operating	oonantions

	Nominal			
Symbol	Description	Zo = 45	Zo = 90	Units
Z <sub>OUT</sub>	Output impedance	20	20	Ohms
R <sub>S</sub>	Driver series resistance	80	80	Ohms
R <sub>TLEFT</sub>	Left end termination	45	90	Ohms
R <sub>TRIGHT</sub>	Right end termination	45	90	Ohms
V <sub>OH</sub>	Output high voltage	1.376	1.480	V
V <sub>OL</sub>	Output low voltage	1.124	1.020	V
V <sub>OD</sub>	Output differential voltage	0.253	0.459	V
V <sub>CM</sub>	Output common mode voltage	1.250	1.250	V
I <sub>DC</sub>	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.



### RSDS

The MachXO2 family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.



### Figure 3-4. RSDS (Reduced Swing Differential Standard)

#### Table 3-4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z <sub>OUT</sub>	Output impedance	20	Ohms
R <sub>S</sub>	Driver series resistor	294	Ohms
R <sub>P</sub>	Driver parallel resistor	121	Ohms
R <sub>T</sub>	Receiver termination	100	Ohms
V <sub>OH</sub>	Output high voltage	1.35	V
V <sub>OL</sub>	Output low voltage	1.15	V
V <sub>OD</sub>	Output differential voltage	0.20	V
V <sub>CM</sub>	Output common mode voltage	1.25	V
Z <sub>BACK</sub>	Back impedance	101.5	Ohms
I <sub>DC</sub>	DC output current	3.66	mA



# Maximum sysIO Buffer Performance

I/O Standard	Max. Speed	Units
LVDS25	400	MHz
LVDS25E	150	MHz
RSDS25	150	MHz
RSDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
SSTL25_I	150	MHz
SSTL25_II	150	MHz
SSTL25D_I	150	MHz
SSTL25D_II	150	MHz
SSTL18_I	150	MHz
SSTL18_II	150	MHz
SSTL18D_I	150	MHz
SSTL18D_II	150	MHz
HSTL18_I	150	MHz
HSTL18_II	150	MHz
HSTL18D_I	150	MHz
HSTL18D_II	150	MHz
PCI33	134	MHz
LVTTL33	150	MHz
LVTTL33D	150	MHz
LVCMOS33	150	MHz
LVCMOS33D	150	MHz
LVCMOS25	150	MHz
LVCMOS25D	150	MHz
LVCMOS25R33	150	MHz
LVCMOS18	150	MHz
LVCMOS18D	150	MHz
LVCMOS18R33	150	MHz
LVCMOS18R25	150	MHz
LVCMOS15	150	MHz
LVCMOS15D	150	MHz
LVCMOS15R33	150	MHz
LVCMOS15R25	150	MHz
LVCMOS12	91	MHz
LVCMOS12D	91	MHz



# **Pinout Information Summary**

	MachXO2-256				MachXO2-640			MachXO2-640U	
	32 QFN <sup>1</sup>	48 QFN <sup>3</sup>	64 ucBGA	100 TQFP	132 csBGA	48 QFN <sup>3</sup>	100 TQFP	132 csBGA	144 TQFP
General Purpose I/O per Bank	•							•	
Bank 0	8	10	9	13	13	10	18	19	27
Bank 1	2	10	12	14	14	10	20	20	26
Bank 2	9	10	11	14	14	10	20	20	28
Bank 3	2	10	12	14	14	10	20	20	26
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Single Ended I/O	21	40	44	55	55	40	78	79	107
Differential I/O per Bank									
Bank 0	4	5	5	7	7	5	9	10	14
Bank 1	1	5	6	7	7	5	10	10	13
Bank 2	4	5	5	7	7	5	10	10	10
Bank 3	1	5	6	7	7	5	10	10	13
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Differential I/O	10	20	22	28	28	20	39	40	54
				_	-	-			-
Dual Function I/O	22	25	27	29	29	25	29	29	33
High-speed Differential I/O	•							•	
Bank 0	0	0	0	0	0	0	0	0	7
Gearboxes									
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	0	0	0	0	0	0	0	0	7
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	0	0	0	0	0	0	0	0	7
DQS Groups								•	•
Bank 1	0	0	0	0	0	0	0	0	2
VCCIO Pins									
Bank 0	2	2	2	2	2	2	2	2	3
Bank 1	1	1	2	2	2	1	2	2	3
Bank 2	2	2	2	2	2	2	2	2	3
Bank 3	1	1	2	2	2	1	2	2	3
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
VCC	2	2	2	2	2	2	2	2	4
GND <sup>2</sup>	2	1	8	8	8	1	8	10	12
NC	0	0	1	26	58	0	3	32	8
Reserved for Configuration	1	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	32	49	64	100	132	49	100	132	144

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.

2. For 48 QFN package, exposed die pad is the device ground.

3. 48-pin QFN information is 'Advanced'.



## Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32C	256	1.2 V	-1	Halogen-Free QFN	32	COM
LCMXO2-256ZE-2SG32C	256	1.2 V	-2	Halogen-Free QFN	32	COM
LCMXO2-256ZE-3SG32C	256	1.2 V	-3	Halogen-Free QFN	32	COM
LCMXO2-256ZE-1UMG64C	256	1.2 V	-1	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-2UMG64C	256	1.2 V	-2	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-3UMG64C	256	1.2 V	-3	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-1TG100C	256	1.2 V	-1	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-2TG100C	256	1.2 V	-2	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-3TG100C	256	1.2 V	-3	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-1MG132C	256	1.2 V	-1	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-2MG132C	256	1.2 V	-2	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-3MG132C	256	1.2 V	-3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100C	640	1.2 V	-1	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-2TG100C	640	1.2 V	-2	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-3TG100C	640	1.2 V	-3	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-1MG132C	640	1.2 V	-1	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-2MG132C	640	1.2 V	-2	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-3MG132C	640	1.2 V	-3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1SG32C	1280	1.2 V	-1	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-2SG32C	1280	1.2 V	-2	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-3SG32C	1280	1.2 V	-3	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-1TG100C	1280	1.2 V	-1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100C	1280	1.2 V	-2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100C	1280	1.2 V	-3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132C	1280	1.2 V	-1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132C	1280	1.2 V	-2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132C	1280	1.2 V	-3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144C	1280	1.2 V	-1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144C	1280	1.2 V	-2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144C	1280	1.2 V	-3	Halogen-Free TQFP	144	COM



### Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32I	256	1.2 V	-1	Halogen-Free QFN	32	IND
LCMXO2-256ZE-2SG32I	256	1.2 V	-2	Halogen-Free QFN	32	IND
LCMXO2-256ZE-3SG32I	256	1.2 V	-3	Halogen-Free QFN	32	IND
LCMXO2-256ZE-1UMG64I	256	1.2 V	-1	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-2UMG64I	256	1.2 V	-2	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-3UMG64I	256	1.2 V	-3	Halogen-Free ucBGA	64	IND
LCMXO2-256ZE-1TG100I	256	1.2 V	-1	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-2TG100I	256	1.2 V	-2	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-3TG100I	256	1.2 V	-3	Halogen-Free TQFP	100	IND
LCMXO2-256ZE-1MG132I	256	1.2 V	-1	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-2MG132I	256	1.2 V	-2	Halogen-Free csBGA	132	IND
LCMXO2-256ZE-3MG132I	256	1.2 V	-3	Halogen-Free csBGA	132	IND
						-
Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100I	640	1.2 V	-1	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-2TG100I	640	1.2 V	-2	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-3TG100I	640	1.2 V	-3	Halogen-Free TQFP	100	IND
LCMXO2-640ZE-1MG132I	640	1.2 V	-1	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-2MG132I	640	1.2 V	-2	Halogen-Free csBGA	132	IND
LCMXO2-640ZE-3MG132I	640	1.2 V	-3	Halogen-Free csBGA	132	IND
	-	- 1	r	1	1	1
Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1UWG25ITR <sup>1</sup>	1280	1.2 V	-1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR50	<sup>3</sup> 1280	1.2 V	-1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1UWG25ITR1K	<sup>2</sup> 1280	1.2 V	-1	Halogen-Free WLCSP	25	IND
LCMXO2-1200ZE-1SG32I	1280	1.2 V	-1	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-2SG32I	1280	1.2 V	-2	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-3SG32I	1280	1.2 V	-3	Halogen-Free QFN	32	IND
LCMXO2-1200ZE-1TG100I	1280	1.2 V	-1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100I	1280	1.2 V	-2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100I	1280	1.2 V	-3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132I	1280	1.2 V	-1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132I	1280	1.2 V	-2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132I	1280	1.2 V	-3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144I	1280	1.2 V	-1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144I	1280	1.2 V	-2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144I	1280	1.2 V	-3	Halogen-Free TQFP	144	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.

2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.

3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100IR11	1280	1.2 V	-1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100IR11	1280	1.2 V	-2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100IR11	1280	1.2 V	-3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132IR1 <sup>1</sup>	1280	1.2 V	-1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132IR1 <sup>1</sup>	1280	1.2 V	-2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132IR11	1280	1.2 V	-3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144IR11	1280	1.2 V	-1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144IR11	1280	1.2 V	-2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144IR11	1280	1.2 V	-3	Halogen-Free TQFP	144	IND

1. Specifications for the "LCMXO2-1200ZE-speed package IR1" are the same as the "LCMXO2-1200ZE-speed package I" devices respectively, except as specified in the R1 Device Specifications section of this data sheet.



Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100IR11	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100IR11	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100IR11	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132IR11	1280	2.5 V / 3.3 V	-4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132IR1 <sup>1</sup>	1280	2.5 V / 3.3 V	-5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132IR11	1280	2.5 V / 3.3 V	-6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144IR1 <sup>1</sup>	1280	2.5 V / 3.3 V	-4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144IR1 <sup>1</sup>	1280	2.5 V / 3.3 V	-5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144IR11	1280	2.5 V / 3.3 V	-6	Halogen-Free TQFP	144	IND

1. Specifications for the "LCMXO2-1200HC-speed package IR1" are the same as the "LCMXO2-1200ZE-speed package I" devices respectively, except as specified in the R1 Device Specifications section of this data sheet.



# **R1 Device Specifications**

The LCMXO2-1200ZE/HC "R1" devices have the same specifications as their Standard (non-R1) counterparts except as listed below. For more details on the R1 to Standard migration refer to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard Non-R1) Devices.

- The User Flash Memory (UFM) cannot be programmed through the internal WISHBONE interface. It can still be programmed through the JTAG/SPI/I<sup>2</sup>C ports.
- The on-chip differential input termination resistor value is higher than intended. It is approximately 200Ω as opposed to the intended 100Ω. It is recommended to use external termination resistors for differential inputs. The on-chip termination resistors can be disabled through Lattice design software.
- Soft Error Detection logic may not produce the correct result when it is run for the first time after configuration. To use this feature, discard the result from the first operation. Subsequent operations will produce the correct result.
- Under certain conditions, IIH exceeds data sheet specifications. The following table provides more details:

Condition	Clamp	Pad Rising IIH Max.	Pad Falling IIH Min.	Steady State Pad High IIH	Steady State Pad Low IIL
VPAD > VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD = VCCIO	ON	10 µA	–10 μA	10 µA	10 µA
VPAD = VCCIO	OFF	1 mA	–1 mA	1 mA	10 µA
VPAD < VCCIO	OFF	10 µA	–10 μA	10 µA	10 µA

- The user SPI interface does not operate correctly in some situations. During master read access and slave write access, the last byte received does not generate the RRDY interrupt.
- In GDDRX2, GDDRX4 and GDDR71 modes, ECLKSYNC may have a glitch in the output under certain conditions, leading to possible loss of synchronization.
- When using the hard I<sup>2</sup>C IP core, the I<sup>2</sup>C status registers I2C\_1\_SR and I2C\_2\_SR may not update correctly.
- PLL Lock signal will glitch high when coming out of standby. This glitch lasts for about 10 μsec before returning low.
- Dual boot only available on HC devices, requires tying VCC and VCCIO2 to the same 3.3 V or 2.5 V supply.



# MachXO2 Family Data Sheet Revision History

March 2017

Data Sheet DS1035

Date	Version	Section	Change Summary						
March 2017	arch 2017 3.3 DC and Switchir Characteristics	DC and Switching Characteristics	Updated the Absolute Maximum Ratings section. Added standards.						
			Updated the sysIO Recommended Operating Conditions section. Added standards.						
			Updated the sysIO Single-Ended DC Electrical Characteristics sec- tion. Added standards.						
			Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the $D_{VB}$ and the $D_{VA}$ parameters were changed to $D_{IB}$ and $D_{IA}$ . The parameter descriptions were also modified.						
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the $D_{VB}$ and the $D_{VA}$ parameters were changed to $D_{IB}$ and $D_{IA}$ . The parameter descriptions were also modified.						
	Pinout Information Ordering Information		Updated the sysCONFIG Port Timing Specifications section. Corrected the $t_{\text{INITL}}$ units from ns to $\mu$ s.						
		Pinout Information	Updated the Signal Descriptions section. Revised the descriptions of the PROGRAMN, INITN, and DONE signals.						
									Updated the Pinout Information Summary section. Added footnote to MachXO2-1200 32 QFN.
		Ordering Information	Updated the MachXO2 Part Number Description section. Corrected the MG184, BG256, FTG256 package information. Added "(0.8 mm Pitch)" to BG332.						
		Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. — Updated LCMXO2-1200ZE-1UWG25ITR50 footnote. — Corrected footnote numbering typo. — Added the LCMXO2-2000ZE-1UWG49ITR50 and LCMXO2- 2000ZE-1UWG49ITR1K part numbers. Updated/added footnote/s.							

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