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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

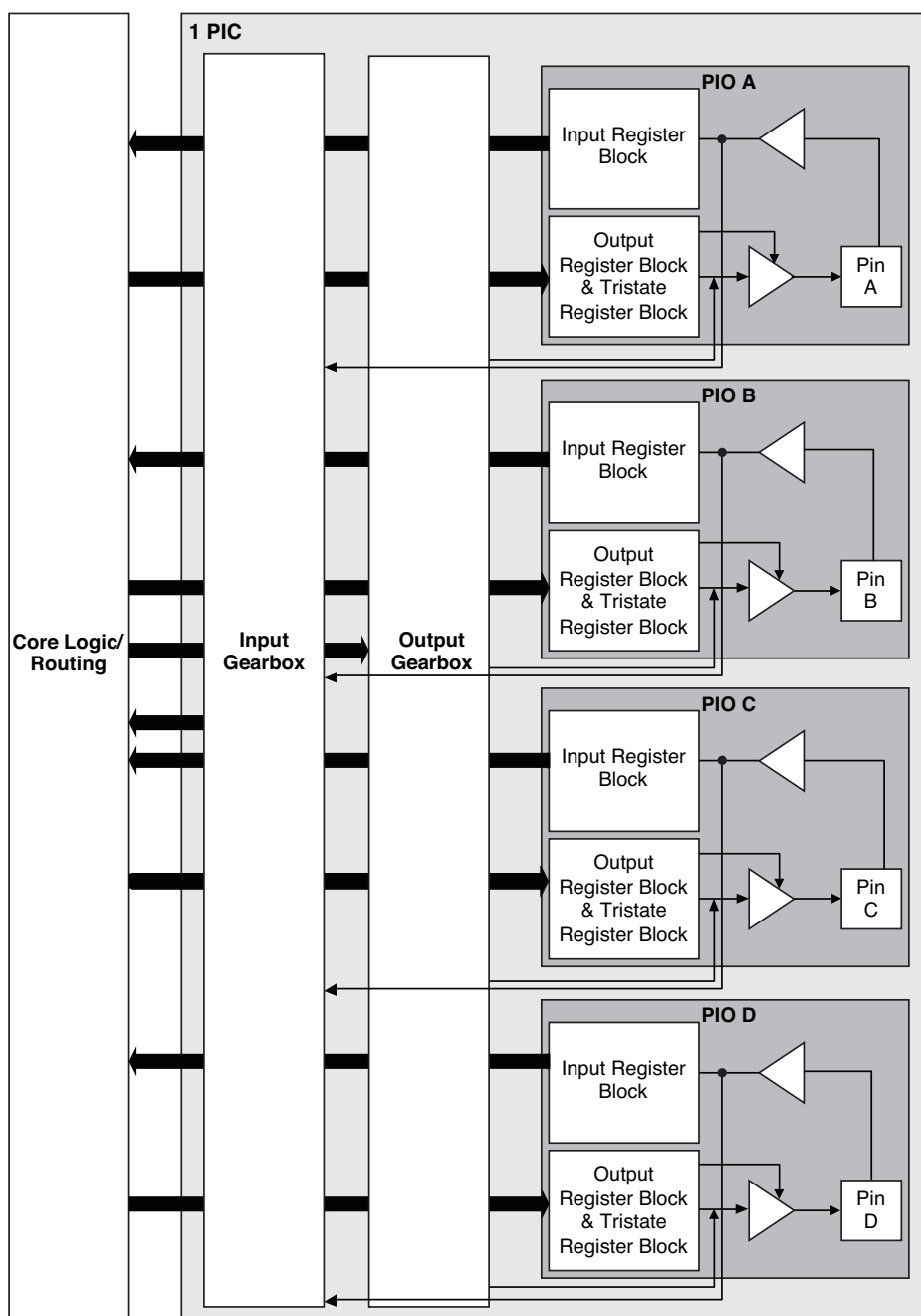
## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Obsolete
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	79
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-1200hc-5tg100cr1">https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-1200hc-5tg100cr1</a>

**Figure 2-11. Group of Four Programmable I/O Cells**



**Notes:**

1. Input gearbox is available only in PIC on the bottom edge of MachXO2-640U, MachXO2-1200/U and larger devices.
2. Output gearbox is available only in PIC on the top edge of MachXO2-640U, MachXO2-1200/U and larger devices.

## Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

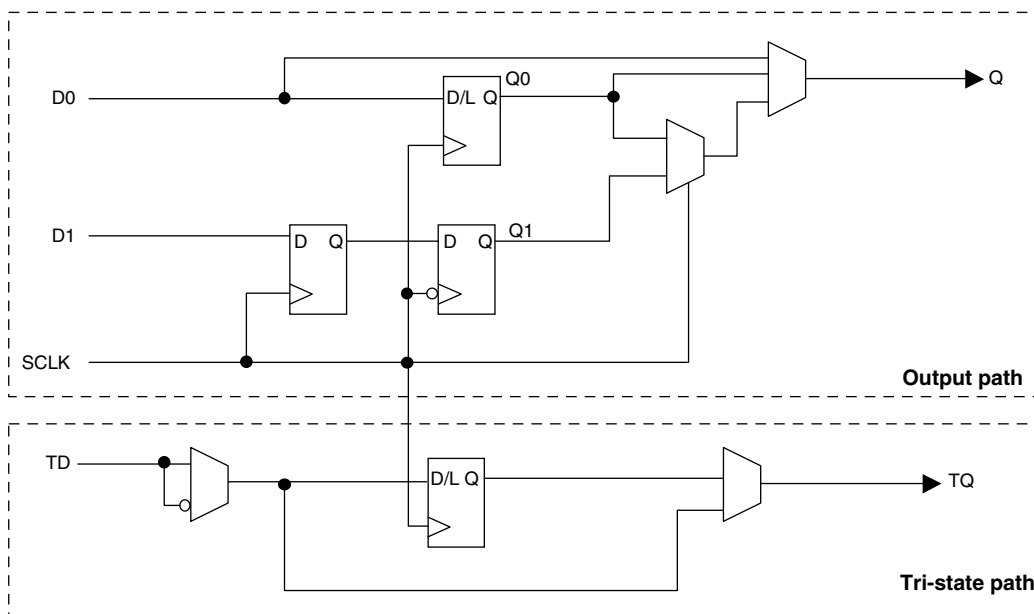
### Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-14 shows the output register block on the left, top and bottom edges.

**Figure 2-14. MachXO2 Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)**



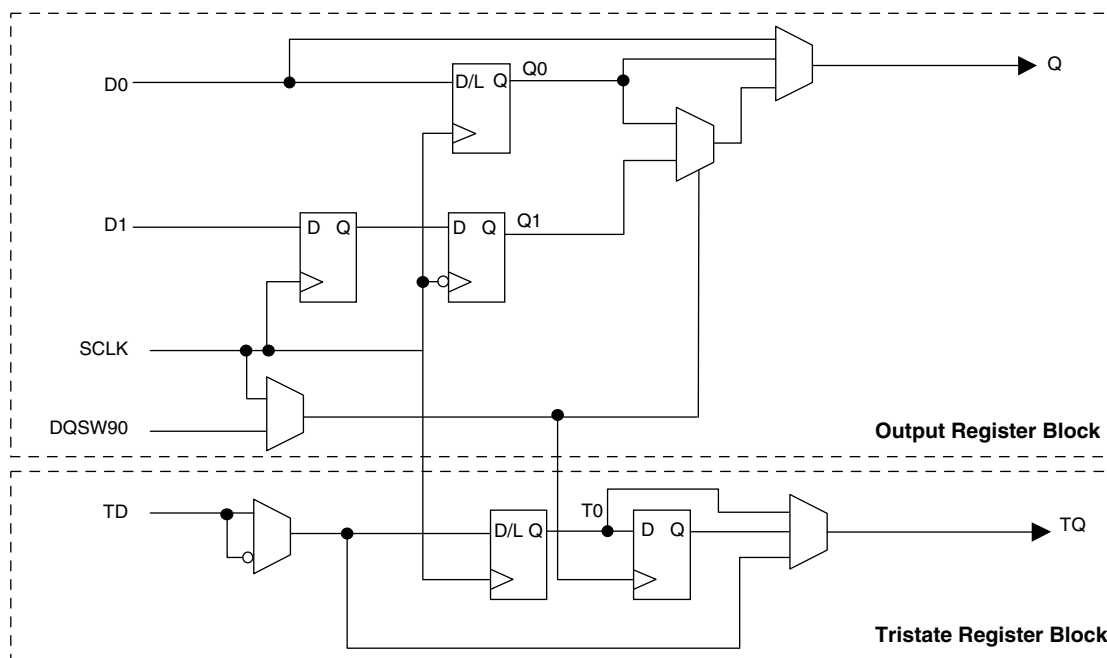
### Right Edge

The output register block on the right edge is a superset of the output register on left, top and bottom edges of the device. In addition to supporting SDR and Generic DDR modes, the output register blocks for PIOs on the right edge include additional logic to support DDR-memory interfaces. Operation of this block is similar to that of the output register block on other edges.

In DDR memory mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the DQSW90 signal is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-15 shows the output register block on the right edge.

**Figure 2-15. MachXO2 Output Register Block Diagram (PIO on the Right Edges)**



### Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

The tri-state register blocks on the right edge contain an additional register for DDR memory operation. In DDR memory mode, the register TS input is fed into another register that is clocked using the DQSW90 signal. The output of this register is used as a tri-state control.

### Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

**Table 2-9. Input Gearbox Signal List**

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDR4(1:8): Q[7:0] GDDR2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDR2(1:4)(IOL-C): Q0, Q1, Q2, Q3

More information on the input gearbox is available in TN1203, [Implementing High-Speed Interfaces with MachXO2 Devices](#).

## Output Gearbox

Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDR4 (8:1) gearbox or as two ODDR2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

**Table 2-10. Output Gearbox Signal List**

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]		
GDDR4(8:1): D[7:0]		
GDDR2(4:1)(IOL-A): D[3:0]		
GDDR2(4:1)(IOL-C): D[7:4]		
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-17 shows the output gearbox block diagram.

**Table 2-11. I/O Support Device by Device**

	MachXO2-256, MachXO2-640	MachXO2-640U, MachXO2-1200	MachXO2-1200U MachXO2-2000/U, MachXO2-4000, MachXO2-7000
Number of I/O Banks	4	4	6
Type of Input Buffers	Single-ended (all I/O banks) Differential Receivers (all I/O banks)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)
Types of Output Buffers	Single-ended buffers with complementary outputs (all I/O banks)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)
Differential Output Emulation Capability	All I/O banks	All I/O banks	All I/O banks
PCI Clamp Support	No	Clamp on bottom side only	Clamp on bottom side only

**Table 2-12. Supported Input Standards**

Input Standard	VCCIO (Typ.)				
	3.3 V	2.5 V	1.8 V	1.5	1.2 V
<b>Single-Ended Interfaces</b>					
LVTTTL	✓	✓ <sup>2</sup>	✓ <sup>2</sup>	✓ <sup>2</sup>	
LVC MOS33	✓	✓ <sup>2</sup>	✓ <sup>2</sup>	✓ <sup>2</sup>	
LVC MOS25	✓ <sup>2</sup>	✓	✓ <sup>2</sup>	✓ <sup>2</sup>	
LVC MOS18	✓ <sup>2</sup>	✓ <sup>2</sup>	✓	✓ <sup>2</sup>	
LVC MOS15	✓ <sup>2</sup>	✓ <sup>2</sup>	✓ <sup>2</sup>	✓	✓ <sup>2</sup>
LVC MOS12	✓ <sup>2</sup>	✓ <sup>2</sup>	✓ <sup>2</sup>	✓ <sup>2</sup>	✓
PCI <sup>1</sup>	✓				
SSTL18 (Class I, Class II)	✓	✓	✓		
SSTL25 (Class I, Class II)	✓	✓			
HSTL18 (Class I, Class II)	✓	✓	✓		
<b>Differential Interfaces</b>					
LVDS	✓	✓			
BLVDS, MVDS, LVPECL, RS DS	✓	✓			
MIPI <sup>3</sup>	✓	✓			
Differential SSTL18 Class I, II	✓	✓	✓		
Differential SSTL25 Class I, II	✓	✓			
Differential HSTL18 Class I, II	✓	✓	✓		

1. Bottom banks of MachXO2-640U, MachXO2-1200/U and higher density devices only.

2. Reduced functionality. Refer to TN1202, [MachXO2 sysIO Usage Guide](#) for more detail.

3. These interfaces can be emulated with external resistors in all devices.

**Table 2-13. Supported Output Standards**

Output Standard	V <sub>CCIO</sub> (Typ.)
<b>Single-Ended Interfaces</b>	
LVTTL	3.3
LVC MOS33	3.3
LVC MOS25	2.5
LVC MOS18	1.8
LVC MOS15	1.5
LVC MOS12	1.2
LVC MOS33, Open Drain	—
LVC MOS25, Open Drain	—
LVC MOS18, Open Drain	—
LVC MOS15, Open Drain	—
LVC MOS12, Open Drain	—
PCI33	3.3
SSTL25 (Class I)	2.5
SSTL18 (Class I)	1.8
HSTL18(Class I)	1.8
<b>Differential Interfaces</b>	
LVDS <sup>1,2</sup>	2.5, 3.3
BLVDS, MLVDS, RSDS <sup>2</sup>	2.5
LVPECL <sup>2</sup>	3.3
MIPI <sup>2</sup>	2.5
Differential SSTL18	1.8
Differential SSTL25	2.5
Differential HSTL18	1.8

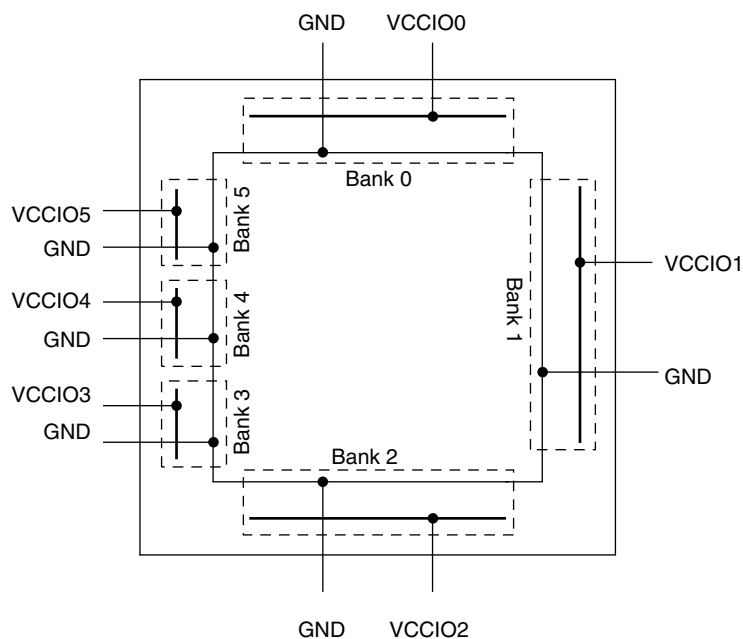
1. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.

2. These interfaces can be emulated with external resistors in all devices.

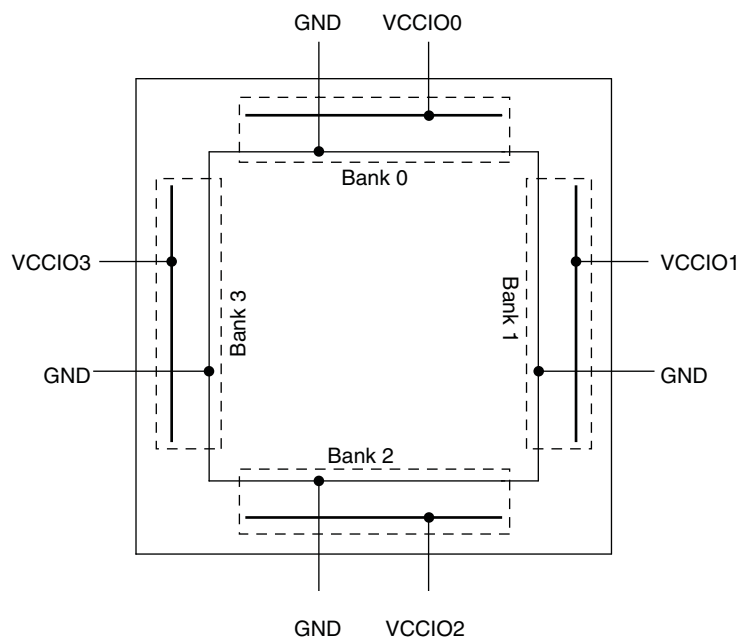
## sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO2-1200U, MachXO2-2000/U and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO2-1200 and lower density devices have four banks (one bank per side). Figures 2-18 and 2-19 show the sysIO banks and their associated supplies for all devices.

**Figure 2-18. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 Banks**



**Figure 2-19. MachXO2-256, MachXO2-640/U and MachXO2-1200 Banks**





When implementing background programming of the on-chip Flash, care must be taken for the operation of the PLL. For devices that have two PLLs (XO2-2000U, -4000 and -7000), the system must put the RPLL (Right-side PLL) in reset state during the background Flash programming. More detailed description can be found in TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

### **Security and One-Time Programmable Mode (OTP)**

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO2 devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile Flash memory spaces. The device can be in one of two modes:

1. Unlocked – Readback of the SRAM configuration and non-volatile Flash memory spaces is allowed.
2. Permanently Locked – The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash and SRAM OTP portions of the device. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

### **Dual Boot**

MachXO2 devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the on-chip Flash. The golden image MUST reside in an external SPI Flash. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

### **Soft Error Detection**

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1206, [MachXO2 Soft Error Detection Usage Guide](#).

### **TraceID**

Each MachXO2 device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I<sup>2</sup>C, or JTAG interfaces.

### **Density Shifting**

The MachXO2 family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the [MachXO2 migration files](#).

### Power-On-Reset Voltage Levels<sup>1, 2, 3, 4, 5</sup>

Symbol	Parameter	Min.	Typ.	Max.	Units
V <sub>PORUP</sub>	Power-On-Reset ramp up trip point (band gap based circuit monitoring V <sub>CCINT</sub> and V <sub>CCIO0</sub> )	0.9	—	1.06	V
V <sub>PORUPEXT</sub>	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V <sub>CC</sub> power supply)	1.5	—	2.1	V
V <sub>PORDNBG</sub>	Power-On-Reset ramp down trip point (band gap based circuit monitoring V <sub>CCINT</sub> )	0.75	—	0.93	V
V <sub>PORDNBGEXT</sub>	Power-On-Reset ramp down trip point (band gap based circuit monitoring V <sub>CC</sub> )	0.98	—	1.33	V
V <sub>PORDNSRAM</sub>	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V <sub>CCINT</sub> )	—	0.6	—	V
V <sub>PORDNSRAMEXT</sub>	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V <sub>CC</sub> )	—	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators V<sub>CCINT</sub> is the same as the V<sub>CC</sub> supply voltage. For devices with voltage regulators, V<sub>CCINT</sub> is regulated from the V<sub>CC</sub> supply voltage.
3. Note that V<sub>PORUP</sub> (min.) and V<sub>PORDNBG</sub> (max.) are in different process corners. For any given process corner V<sub>PORDNBG</sub> (max.) is always 12.0 mV below V<sub>PORUP</sub> (min.).
4. V<sub>PORUPEXT</sub> is for HC devices only. In these devices a separate POR circuit monitors the external V<sub>CC</sub> power supply.
5. V<sub>CCIO0</sub> does not have a Power-On-Reset ramp down trip point. V<sub>CCIO0</sub> must remain within the Recommended Operating Conditions to ensure proper operation.

### Programming/Erase Specifications

Symbol	Parameter	Min.	Max. <sup>1</sup>	Units
N <sub>PROGCYC</sub>	Flash Programming cycles per t <sub>RETENTION</sub>	—	10,000	Cycles
	Flash functional programming cycles	—	100,000	
t <sub>RETENTION</sub>	Data retention at 100 °C junction temperature	10	—	Years
	Data retention at 85 °C junction temperature	20	—	

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

### Hot Socketing Specifications<sup>1, 2, 3</sup>

Symbol	Parameter	Condition	Max.	Units
I <sub>DK</sub>	Input or I/O leakage Current	0 < V <sub>IN</sub> < V <sub>IH</sub> (MAX)	+/-1000	μA

1. Insensitive to sequence of V<sub>CC</sub> and V<sub>CCIO</sub>. However, assumes monotonic rise/fall rates for V<sub>CC</sub> and V<sub>CCIO</sub>.
2. 0 < V<sub>CC</sub> < V<sub>CC</sub> (MAX), 0 < V<sub>CCIO</sub> < V<sub>CCIO</sub> (MAX).
3. I<sub>DK</sub> is additive to I<sub>PU</sub>, I<sub>PD</sub> or I<sub>BH</sub>.

### ESD Performance

Please refer to the [MachXO2 Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

Input/Output Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$ Max. (V)	$V_{OH}$ Min. (V)	$I_{OL}$ Max. <sup>4</sup> (mA)	$I_{OH}$ Max. <sup>4</sup> (mA)
	Min. (V) <sup>3</sup>	Max. (V)	Min. (V)	Max. (V)				
LVC MOS10R25	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain

1. MachXO2 devices allow LVC MOS inputs to be placed in I/O banks where  $V_{CCIO}$  is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO2 devices do not meet the relevant JEDEC specification are documented in the table below.
2. MachXO2 devices allow for LVC MOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1202, [MachXO2 sysIO Usage Guide](#).
3. The dual function I<sup>2</sup>C pins SCL and SDA are limited to a  $V_{IL}$  min of -0.25 V or to -0.3 V with a duration of <10 ns.
4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive  $V_{CCIO}$  or GND pad connections, or between the last  $V_{CCIO}$  or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of  $n * 8$  mA. "n" is the number of I/O pads between the two consecutive bank  $V_{CCIO}$  or GND connections or between the last  $V_{CCIO}$  and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

Input Standard	$V_{CCIO}$ (V)	$V_{IL}$ Max. (V)
LVC MOS 33	1.5	0.685
LVC MOS 25	1.5	0.687
LVC MOS 18	1.5	0.655

## sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of MachXO2-640U, MachXO2-1200/U and higher density devices in the MachXO2 PLD family.

## LVDS

### Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{INP}$ $V_{INM}$	Input Voltage	$V_{CCIO} = 3.3$ V	0	—	2.605	V
		$V_{CCIO} = 2.5$ V	0	—	2.05	V
$V_{THD}$	Differential Input Threshold		±100	—		mV
$V_{CM}$	Input Common Mode Voltage	$V_{CCIO} = 3.3$ V	0.05	—	2.6	V
		$V_{CCIO} = 2.5$ V	0.05	—	2.0	V
$I_{IN}$	Input current	Power on	—	—	±10	μA
$V_{OH}$	Output high voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100$ Ohm	—	1.375	—	V
$V_{OL}$	Output low voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100$ Ohm	0.90	1.025	—	V
$V_{OD}$	Output voltage differential	$(V_{OP} - V_{OM})$ , $R_T = 100$ Ohm	250	350	450	mV
$\Delta V_{OD}$	Change in $V_{OD}$ between high and low		—	—	50	mV
$V_{OS}$	Output voltage offset	$(V_{OP} + V_{OM})/2$ , $R_T = 100$ Ohm	1.125	1.20	1.395	V
$\Delta V_{OS}$	Change in $V_{OS}$ between H and L		—	—	50	mV
$I_{OSD}$	Output short circuit current	$V_{OD} = 0$ V driver outputs shorted	—	—	24	mA

### MachXO2 External Switching Characteristics – HC/HE Devices<sup>1, 2, 3, 4, 5, 6, 7</sup>

Over Recommended Operating Conditions

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f <sub>MAX_PRI</sub> <sup>8</sup>	Frequency for Primary Clock Tree	All MachXO2 devices	—	388	—	323	—	269	MHz
t <sub>W_PRI</sub>	Clock Pulse Width for Primary Clock	All MachXO2 devices	0.5	—	0.6	—	0.7	—	ns
t <sub>SKEW_PRI</sub>	Primary Clock Skew Within a Device	MachXO2-256HC-HE	—	912	—	939	—	975	ps
		MachXO2-640HC-HE	—	844	—	871	—	908	ps
		MachXO2-1200HC-HE	—	868	—	902	—	951	ps
		MachXO2-2000HC-HE	—	867	—	897	—	941	ps
		MachXO2-4000HC-HE	—	865	—	892	—	931	ps
		MachXO2-7000HC-HE	—	902	—	942	—	989	ps
Edge Clock									
f <sub>MAX_EDGE</sub> <sup>8</sup>	Frequency for Edge Clock	MachXO2-1200 and larger devices	—	400	—	333	—	278	MHz
Pin-LUT-Pin Propagation Delay									
t <sub>PD</sub>	Best case propagation delay through one LUT-4	All MachXO2 devices	—	6.72	—	6.96	—	7.24	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t <sub>CO</sub>	Clock to Output – PIO Output Register	MachXO2-256HC-HE	—	7.13	—	7.30	—	7.57	ns
		MachXO2-640HC-HE	—	7.15	—	7.30	—	7.57	ns
		MachXO2-1200HC-HE	—	7.44	—	7.64	—	7.94	ns
		MachXO2-2000HC-HE	—	7.46	—	7.66	—	7.96	ns
		MachXO2-4000HC-HE	—	7.51	—	7.71	—	8.01	ns
		MachXO2-7000HC-HE	—	7.54	—	7.75	—	8.06	ns
t <sub>SU</sub>	Clock to Data Setup – PIO Input Register	MachXO2-256HC-HE	–0.06	—	–0.06	—	–0.06	—	ns
		MachXO2-640HC-HE	–0.06	—	–0.06	—	–0.06	—	ns
		MachXO2-1200HC-HE	–0.17	—	–0.17	—	–0.17	—	ns
		MachXO2-2000HC-HE	–0.20	—	–0.20	—	–0.20	—	ns
		MachXO2-4000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-7000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
t <sub>H</sub>	Clock to Data Hold – PIO Input Register	MachXO2-256HC-HE	1.75	—	1.95	—	2.16	—	ns
		MachXO2-640HC-HE	1.75	—	1.95	—	2.16	—	ns
		MachXO2-1200HC-HE	1.88	—	2.12	—	2.36	—	ns
		MachXO2-2000HC-HE	1.89	—	2.13	—	2.37	—	ns
		MachXO2-4000HC-HE	1.94	—	2.18	—	2.43	—	ns
		MachXO2-7000HC-HE	1.98	—	2.23	—	2.49	—	ns

Parameter	Description	Device	-6		-5		-4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>SU_DEL</sub>	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-256HC-HE	1.42	—	1.59	—	1.96	—	ns
		MachXO2-640HC-HE	1.41	—	1.58	—	1.96	—	ns
		MachXO2-1200HC-HE	1.63	—	1.79	—	2.17	—	ns
		MachXO2-2000HC-HE	1.61	—	1.76	—	2.13	—	ns
		MachXO2-4000HC-HE	1.66	—	1.81	—	2.19	—	ns
		MachXO2-7000HC-HE	1.53	—	1.67	—	2.03	—	ns
t <sub>H_DEL</sub>	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-256HC-HE	–0.24	—	–0.24	—	–0.24	—	ns
		MachXO2-640HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-1200HC-HE	–0.24	—	–0.24	—	–0.24	—	ns
		MachXO2-2000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000HC-HE	–0.25	—	–0.25	—	–0.25	—	ns
		MachXO2-7000HC-HE	–0.21	—	–0.21	—	–0.21	—	ns
f <sub>MAX_IO</sub>	Clock Frequency of I/O and PFU Register	All MachXO2 devices	—	388	—	323	—	269	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)									
t <sub>COE</sub>	Clock to Output – PIO Output Register	MachXO2-1200HC-HE	—	7.53	—	7.76	—	8.10	ns
		MachXO2-2000HC-HE	—	7.53	—	7.76	—	8.10	ns
		MachXO2-4000HC-HE	—	7.45	—	7.68	—	8.00	ns
		MachXO2-7000HC-HE	—	7.53	—	7.76	—	8.10	ns
t <sub>SUE</sub>	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
		MachXO2-2000HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
		MachXO2-4000HC-HE	–0.16	—	–0.16	—	–0.16	—	ns
		MachXO2-7000HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
t <sub>HE</sub>	Clock to Data Hold – PIO Input Register	MachXO2-1200HC-HE	1.97	—	2.24	—	2.52	—	ns
		MachXO2-2000HC-HE	1.97	—	2.24	—	2.52	—	ns
		MachXO2-4000HC-HE	1.89	—	2.16	—	2.43	—	ns
		MachXO2-7000HC-HE	1.97	—	2.24	—	2.52	—	ns
t <sub>SU_DELE</sub>	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200HC-HE	1.56	—	1.69	—	2.05	—	ns
		MachXO2-2000HC-HE	1.56	—	1.69	—	2.05	—	ns
		MachXO2-4000HC-HE	1.74	—	1.88	—	2.25	—	ns
		MachXO2-7000HC-HE	1.66	—	1.81	—	2.17	—	ns
t <sub>H_DELE</sub>	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-2000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000HC-HE	–0.34	—	–0.34	—	–0.34	—	ns
		MachXO2-7000HC-HE	–0.29	—	–0.29	—	–0.29	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)									
t <sub>COPLL</sub>	Clock to Output – PIO Output Register	MachXO2-1200HC-HE	—	5.97	—	6.00	—	6.13	ns
		MachXO2-2000HC-HE	—	5.98	—	6.01	—	6.14	ns
		MachXO2-4000HC-HE	—	5.99	—	6.02	—	6.16	ns
		MachXO2-7000HC-HE	—	6.02	—	6.06	—	6.20	ns
t <sub>SUPLL</sub>	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	0.36	—	0.36	—	0.65	—	ns
		MachXO2-2000HC-HE	0.36	—	0.36	—	0.63	—	ns
		MachXO2-4000HC-HE	0.35	—	0.35	—	0.62	—	ns
		MachXO2-7000HC-HE	0.34	—	0.34	—	0.59	—	ns

## Flash Download Time<sup>1, 2</sup>

Symbol	Parameter	Device	Typ.	Units
$t_{\text{REFRESH}}$	POR to Device I/O Active	LCMXO2-256	0.6	ms
		LCMXO2-640	1.0	ms
		LCMXO2-640U	1.9	ms
		LCMXO2-1200	1.9	ms
		LCMXO2-1200U	1.4	ms
		LCMXO2-2000	1.4	ms
		LCMXO2-2000U	2.4	ms
		LCMXO2-4000	2.4	ms
		LCMXO2-7000	3.8	ms

1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.

2. The Flash download time is measured starting from the maximum voltage of POR trip point.

## JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
$f_{\text{MAX}}$	TCK clock frequency	—	25	MHz
$t_{\text{BTCPH}}$	TCK [BSCAN] clock pulse width high	20	—	ns
$t_{\text{BTCPL}}$	TCK [BSCAN] clock pulse width low	20	—	ns
$t_{\text{BTS}}$	TCK [BSCAN] setup time	10	—	ns
$t_{\text{BTH}}$	TCK [BSCAN] hold time	8	—	ns
$t_{\text{BTCO}}$	TAP controller falling edge of clock to valid output	—	10	ns
$t_{\text{BTCODIS}}$	TAP controller falling edge of clock to valid disable	—	10	ns
$t_{\text{BTCOEN}}$	TAP controller falling edge of clock to valid enable	—	10	ns
$t_{\text{BTCRS}}$	BSCAN test capture register setup time	8	—	ns
$t_{\text{BTCRH}}$	BSCAN test capture register hold time	20	—	ns
$t_{\text{BUTCO}}$	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{\text{BTUODIS}}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{\text{BTUPOEN}}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

### I<sup>2</sup>C Port Timing Specifications<sup>1, 2</sup>

Symbol	Parameter	Min.	Max.	Units
f <sub>MAX</sub>	Maximum SCL clock frequency	—	400	kHz

- MachXO2 supports the following modes:
  - Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)
  - Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)
- Refer to the I<sup>2</sup>C specification for timing requirements.

### SPI Port Timing Specifications<sup>1</sup>

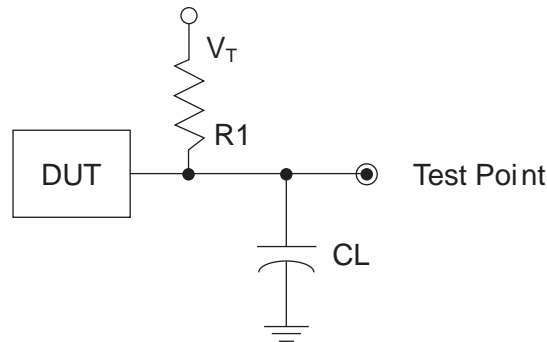
Symbol	Parameter	Min.	Max.	Units
f <sub>MAX</sub>	Maximum SCK clock frequency	—	45	MHz

- Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

### Switching Test Conditions

Figure 3-13 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-5.

**Figure 3-13. Output Test Load, LVTTTL and LVCMOS Standards**



**Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces**

Test Condition	R1	CL	Timing Ref.	VT
LVTTTL and LVCMOS settings (L -> H, H -> L)	$\infty$	0pF	LVTTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = V <sub>CCIO</sub> /2	—
			LVCMOS 1.8 = V <sub>CCIO</sub> /2	—
			LVCMOS 1.5 = V <sub>CCIO</sub> /2	—
			LVCMOS 1.2 = V <sub>CCIO</sub> /2	—
LVTTTL and LVCMOS 3.3 (Z -> H)	188	0pF	1.5 V	V <sub>OL</sub>
LVTTTL and LVCMOS 3.3 (Z -> L)			1.5 V	V <sub>OH</sub>
Other LVCMOS (Z -> H)			V <sub>CCIO</sub> /2	V <sub>OL</sub>
Other LVCMOS (Z -> L)			V <sub>CCIO</sub> /2	V <sub>OH</sub>
LVTTTL + LVCMOS (H -> Z)			V <sub>OH</sub> - 0.15 V	V <sub>OL</sub>
LVTTTL + LVCMOS (L -> Z)			V <sub>OL</sub> - 0.15 V	V <sub>OH</sub>

Note: Output test conditions for all other interfaces are determined by the respective standards.

### Pinout Information Summary

	MachXO2-256					MachXO2-640			MachXO2-640U
	32 QFN <sup>1</sup>	48 QFN <sup>3</sup>	64 ucBGA	100 TQFP	132 csBGA	48 QFN <sup>3</sup>	100 TQFP	132 csBGA	144 TQFP
<b>General Purpose I/O per Bank</b>									
Bank 0	8	10	9	13	13	10	18	19	27
Bank 1	2	10	12	14	14	10	20	20	26
Bank 2	9	10	11	14	14	10	20	20	28
Bank 3	2	10	12	14	14	10	20	20	26
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Single Ended I/O	21	40	44	55	55	40	78	79	107
<b>Differential I/O per Bank</b>									
Bank 0	4	5	5	7	7	5	9	10	14
Bank 1	1	5	6	7	7	5	10	10	13
Bank 2	4	5	5	7	7	5	10	10	14
Bank 3	1	5	6	7	7	5	10	10	13
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
Total General Purpose Differential I/O	10	20	22	28	28	20	39	40	54
<b>Dual Function I/O</b>									
	22	25	27	29	29	25	29	29	33
<b>High-speed Differential I/O</b>									
Bank 0	0	0	0	0	0	0	0	0	7
<b>Gearboxes</b>									
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	0	0	0	0	0	0	0	0	7
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	0	0	0	0	0	0	0	0	7
<b>DQS Groups</b>									
Bank 1	0	0	0	0	0	0	0	0	2
<b>VCCIO Pins</b>									
Bank 0	2	2	2	2	2	2	2	2	3
Bank 1	1	1	2	2	2	1	2	2	3
Bank 2	2	2	2	2	2	2	2	2	3
Bank 3	1	1	2	2	2	1	2	2	3
Bank 4	0	0	0	0	0	0	0	0	0
Bank 5	0	0	0	0	0	0	0	0	0
VCC	2	2	2	2	2	2	2	2	4
GND <sup>2</sup>	2	1	8	8	8	1	8	10	12
NC	0	0	1	26	58	0	3	32	8
Reserved for Configuration	1	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	32	49	64	100	132	49	100	132	144

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.
2. For 48 QFN package, exposed die pad is the device ground.
3. 48-pin QFN information is 'Advanced'.



	MachXO2-4000							
	84 QFN	132 csBGA	144 TQFP	184 csBGA	256 caBGA	256 ftBGA	332 caBGA	484 fpBGA
<b>General Purpose I/O per Bank</b>								
Bank 0	27	25	27	37	50	50	68	70
Bank 1	10	26	29	37	52	52	68	68
Bank 2	22	28	29	39	52	52	70	72
Bank 3	0	7	9	10	16	16	24	24
Bank 4	9	8	10	12	16	16	16	16
Bank 5	0	10	10	15	20	20	28	28
Total General Purpose Single Ended I/O	68	104	114	150	206	206	274	278
<b>Differential I/O per Bank</b>								
Bank 0	13	13	14	18	25	25	34	35
Bank 1	4	13	14	18	26	26	34	34
Bank 2	11	14	14	19	26	26	35	36
Bank 3	0	3	4	4	8	8	12	12
Bank 4	4	4	5	6	8	8	8	8
Bank 5	0	5	5	7	10	10	14	14
Total General Purpose Differential I/O	32	52	56	72	103	103	137	139
<b>Dual Function I/O</b>								
	28	37	37	37	37	37	37	37
<b>High-speed Differential I/O</b>								
Bank 0	8	8	9	8	18	18	18	18
<b>Gearboxes</b>								
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	8	8	9	9	18	18	18	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	11	14	14	12	18	18	18	18
<b>DQS Groups</b>								
Bank 1	1	2	2	2	2	2	2	2
<b>VCCIO Pins</b>								
Bank 0	3	3	3	3	4	4	4	10
Bank 1	1	3	3	3	4	4	4	10
Bank 2	2	3	3	3	4	4	4	10
Bank 3	1	1	1	1	1	1	2	3
Bank 4	1	1	1	1	2	2	1	4
Bank 5	1	1	1	1	1	1	2	3
<b>VCC</b>								
	4	4	4	4	8	8	8	12
<b>GND</b>								
	4	10	12	16	24	24	27	48
<b>NC</b>								
	1	1	1	1	1	1	5	105
<b>Reserved for configuration</b>								
	1	1	1	1	1	1	1	1
Total Count of Bonded Pins	84	132	144	184	256	256	332	484

## Ordering Information

MachXO2 devices have top-side markings, for commercial and industrial grades, as shown below:

<b>LATTICE</b> LCMXO2-1200ZE 1TG100C Datecode	LCMXO2 256ZE 1UG64C Datecode
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Notes:

1. Markings are abbreviated for small packages.
2. See [PCN 05A-12](#) for information regarding a change to the top-side mark logo.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32C	1280	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	COM
LCMXO2-1200HC-5SG32C	1280	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	COM
LCMXO2-1200HC-6SG32C	1280	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	COM
LCMXO2-1200HC-4TG100C	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-5TG100C	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-6TG100C	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-4MG132C	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-5MG132C	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-6MG132C	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-4TG144C	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-5TG144C	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-6TG144C	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256C	1280	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-1200UHC-5FTG256C	1280	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-1200UHC-6FTG256C	1280	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100C	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-5TG100C	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-6TG100C	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-4MG132C	2112	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-5MG132C	2112	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-6MG132C	2112	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-4TG144C	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-5TG144C	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-6TG144C	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-4BG256C	2112	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-5BG256C	2112	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-6BG256C	2112	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-4FTG256C	2112	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HC-5FTG256C	2112	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HC-6FTG256C	2112	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100IR1 <sup>1</sup>	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100IR1 <sup>1</sup>	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100IR1 <sup>1</sup>	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132IR1 <sup>1</sup>	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132IR1 <sup>1</sup>	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132IR1 <sup>1</sup>	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144IR1 <sup>1</sup>	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144IR1 <sup>1</sup>	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144IR1 <sup>1</sup>	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200ZE-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100IR1 <sup>1</sup>	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100IR1 <sup>1</sup>	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100IR1 <sup>1</sup>	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132IR1 <sup>1</sup>	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132IR1 <sup>1</sup>	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132IR1 <sup>1</sup>	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144IR1 <sup>1</sup>	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144IR1 <sup>1</sup>	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144IR1 <sup>1</sup>	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200HC-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.