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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	79
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmx02-1200hc-5tg100i

Table 1-1. MachXO2™ Family Selection Guide

		XO2-256	XO2-640	XO2-640U ¹	XO2-1200	XO2-1200U ¹	XO2-2000	XO2-2000U ¹	XO2-4000	XO2-7000
LUTs		256	640	640	1280	1280	2112	2112	4320	6864
Distributed RAM (kbits)		2	5	5	10	10	16	16	34	54
EBR SRAM (kbits)		0	18	64	64	74	74	92	92	240
Number of EBR SRAM Blocks (9 kbits/block)		0	2	7	7	8	8	10	10	26
UFM (kbits)		0	24	64	64	80	80	96	96	256
Device Options:	HC ²	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	HE ³						Yes	Yes	Yes	Yes
	ZE ⁴	Yes	Yes		Yes		Yes		Yes	Yes
Number of PLLs		0	0	1	1	1	1	2	2	2
Hardened Functions:	I2C	2	2	2	2	2	2	2	2	2
	SPI	1	1	1	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1	1	1	1
Packages		IO								
25-ball WLCSP ⁵ (2.5 mm x 2.5 mm, 0.4 mm)					18					
32 QFN ⁶ (5 mm x 5 mm, 0.5 mm)		21			21					
48 QFN ^{8,9} (7 mm x 7 mm, 0.5 mm)		40	40							
49-ball WLCSP ⁵ (3.2 mm x 3.2 mm, 0.4 mm)							38			
64-ball ucBGA (4 mm x 4 mm, 0.4 mm)		44								
84 QFN ⁷ (7 mm x 7 mm, 0.5 mm)									68	
100-pin TQFP (14 mm x 14 mm)		55	78		79		79			
132-ball csBGA (8 mm x 8 mm, 0.5 mm)		55	79		104		104		104	
144-pin TQFP (20 mm x 20 mm)				107	107		111		114	114
184-ball csBGA ⁷ (8 mm x 8 mm, 0.5 mm)									150	
256-ball caBGA (14 mm x 14 mm, 0.8 mm)							206		206	206
256-ball ftBGA (17 mm x 17 mm, 1.0 mm)						206	206		206	206
332-ball caBGA (17 mm x 17 mm, 0.8 mm)									274	278
484-ball ftBGA (23 mm x 23 mm, 1.0 mm)							278		278	334

1. Ultra high I/O device.
2. High performance with regulator – VCC = 2.5 V, 3.3 V
3. High performance without regulator – V_{CC} = 1.2 V
4. Low power without regulator – V_{CC} = 1.2 V
5. WLCSP package only available for ZE devices.
6. 32 QFN package only available for HC and ZE devices.
7. 184 csBGA package only available for HE devices.
8. 48-pin QFN information is 'Advanced'.
9. 48 QFN package only available for HC devices.

Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I²C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external V_{CC} supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external V_{CC} supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a “per-pin” basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I²C port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

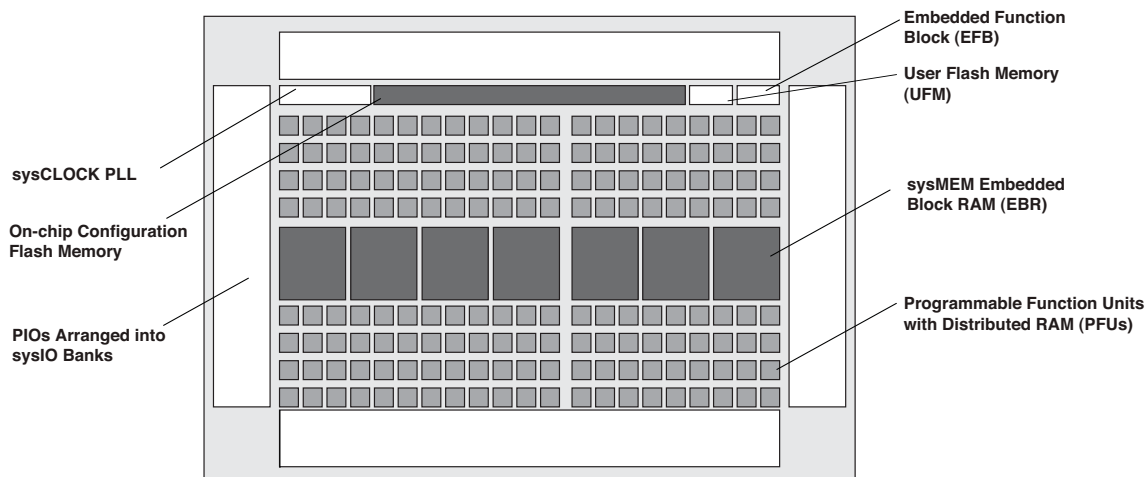
Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

Architecture Overview

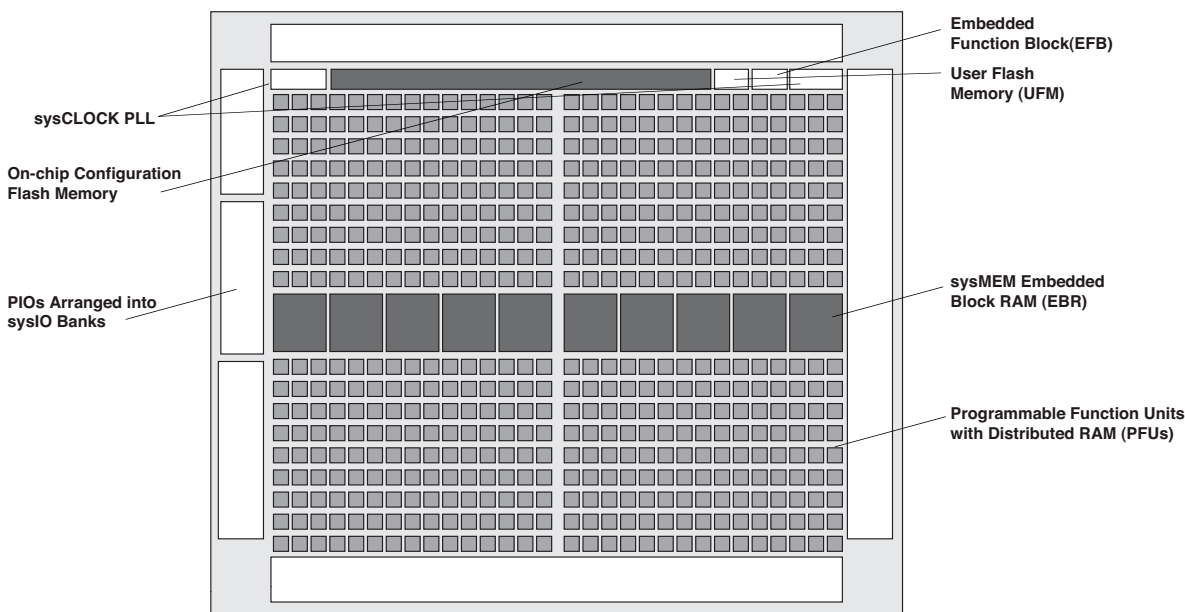
The MachXO2 family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have sysCLOCK™ PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.

Figure 2-1. Top View of the MachXO2-1200 Device



Note: MachXO2-256, and MachXO2-640/U are similar to MachXO2-1200. MachXO2-256 has a lower LUT count and no PLL or EBR blocks. MachXO2-640 has no PLL, a lower LUT count and two EBR blocks. MachXO2-640U has a lower LUT count, one PLL and seven EBR blocks.

Figure 2-2. Top View of the MachXO2-4000 Device



Note: MachXO2-1200U, MachXO2-2000/U and MachXO2-7000 are similar to MachXO2-4000. MachXO2-1200U and MachXO2-2000 have a lower LUT count, one PLL, and eight EBR blocks. MachXO2-2000U has a lower LUT count, two PLLs, and 10 EBR blocks. MachXO2-7000 has a higher LUT count, two PLLs, and 26 EBR blocks.

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO2 devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Table 2-8. PIO Signal List

Pin Name	I/O Type	Description
CE	Input	Clock Enable
D	Input	Pin input from sysIO buffer.
INDD	Output	Register bypassed input.
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysIO Buffer
TQ	Output	Tri-state output signals to sysIO Buffer
DQSR90 ¹	Input	DQS shift 90-degree read clock
DQSW90 ¹	Input	DQS shift 90-degree write clock
DDRCLKPOL ¹	Input	DDR input register polarity control signal from DQS
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

1. Available in PIO on right edge only.

Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition to this functionality, the input register blocks for the PIOs on the right edge include built-in logic to interface to DDR memory.

Figure 2-12 shows the input register block for the PIOs located on the left, top and bottom edges. Figure 2-13 shows the input register block for the PIOs on the right edge.

Left, Top, Bottom Edges

Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

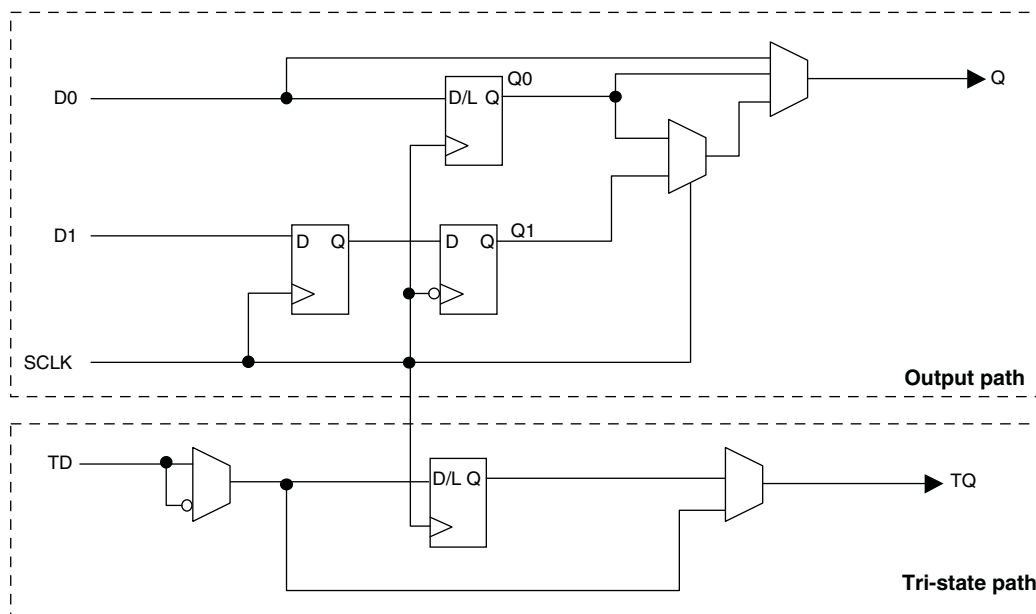
Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-14 shows the output register block on the left, top and bottom edges.

Figure 2-14. MachXO2 Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)



Right Edge

The output register block on the right edge is a superset of the output register on left, top and bottom edges of the device. In addition to supporting SDR and Generic DDR modes, the output register blocks for PIOs on the right edge include additional logic to support DDR-memory interfaces. Operation of this block is similar to that of the output register block on other edges.

In DDR memory mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the DQSW90 signal is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-15 shows the output register block on the right edge.

Table 2-11. I/O Support Device by Device

	MachXO2-256, MachXO2-640	MachXO2-640U, MachXO2-1200	MachXO2-1200U MachXO2-2000/U, MachXO2-4000, MachXO2-7000
Number of I/O Banks	4	4	6
Type of Input Buffers	Single-ended (all I/O banks) Differential Receivers (all I/O banks)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)
Types of Output Buffers	Single-ended buffers with complementary outputs (all I/O banks)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)
Differential Output Emulation Capability	All I/O banks	All I/O banks	All I/O banks
PCI Clamp Support	No	Clamp on bottom side only	Clamp on bottom side only

Table 2-12. Supported Input Standards

Input Standard	VCCIO (Typ.)				
	3.3 V	2.5 V	1.8 V	1.5	1.2 V
Single-Ended Interfaces					
LVTTTL	✓	✓ ²	✓ ²	✓ ²	
LVC MOS33	✓	✓ ²	✓ ²	✓ ²	
LVC MOS25	✓ ²	✓	✓ ²	✓ ²	
LVC MOS18	✓ ²	✓ ²	✓	✓ ²	
LVC MOS15	✓ ²	✓ ²	✓ ²	✓	✓ ²
LVC MOS12	✓ ²	✓ ²	✓ ²	✓ ²	✓
PCI ¹	✓				
SSTL18 (Class I, Class II)	✓	✓	✓		
SSTL25 (Class I, Class II)	✓	✓			
HSTL18 (Class I, Class II)	✓	✓	✓		
Differential Interfaces					
LVDS	✓	✓			
BLVDS, MVDS, LVPECL, RSDS	✓	✓			
MIPI ³	✓	✓			
Differential SSTL18 Class I, II	✓	✓	✓		
Differential SSTL25 Class I, II	✓	✓			
Differential HSTL18 Class I, II	✓	✓	✓		

1. Bottom banks of MachXO2-640U, MachXO2-1200/U and higher density devices only.

2. Reduced functionality. Refer to TN1202, [MachXO2 sysIO Usage Guide](#) for more detail.

3. These interfaces can be emulated with external resistors in all devices.

There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#) (Appendix B)
- TN1205, [Using User Flash Memory and Hardened Control Functions in MachXO2 Devices](#)

Figure 2-22. SPI Core Block Diagram

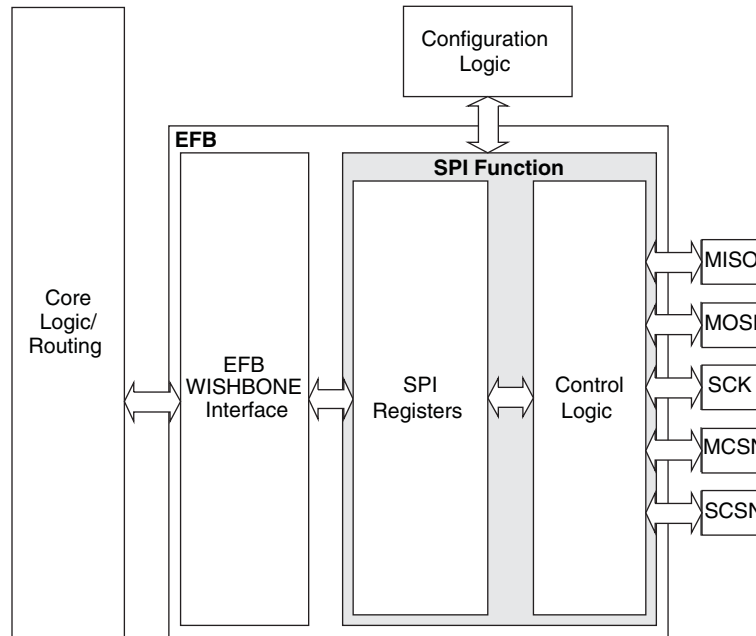


Table 2-16 describes the signals interfacing with the SPI cores.

Table 2-16. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	O	Master	SPI master chip-select output
spi_csn[1..7]	O	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	O	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
ufm_sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the User Flash Memory (UFM).
cfg_stdbby	O	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.
cfg_wake	O	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.

Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, [Boundary Scan Testability with Lattice sysIO Capability](#) and TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#).

Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I²C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

1. Internal Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I²C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, [MachXO2 Programming and Configuration Usage Guide](#) for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, [MachXO2 Programming and Configuration Usage Guide](#).

TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#) for details.

Absolute Maximum Ratings^{1, 2, 3}

	MachXO2 ZE/HE (1.2 V)	MachXO2 HC (2.5 V / 3.3 V)
Supply Voltage V_{CC}	–0.5 V to 1.32 V	–0.5 V to 3.75 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied ^{4, 5}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied ⁴	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature (T_J)	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to ($V_{IHMAX} + 2$) volts is permitted for a duration of <20 ns.
5. The dual function I²C pins SCL and SDA are limited to –0.25 V to 3.75 V or to –0.3 V with a duration of <20 ns.

Recommended Operating Conditions¹

Symbol	Parameter	Min.	Max.	Units
V_{CC}^1	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V / 3.3 V Devices	2.375	3.6	V
$V_{CCIO}^{1, 2, 3}$	I/O Driver Supply Voltage	1.14	3.6	V
t_{JCOM}	Junction Temperature Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature Industrial Operation	–40	100	°C

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.

Power Supply Ramp Rates¹

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.01	—	100	V/ms

1. Assumes monotonic ramp rates.

sysIO Single-Ended DC Electrical Characteristics^{1, 2}

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max. ⁴ (mA)	I_{OH} Max. ⁴ (mA)
	Min. (V) ³	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3 LVTTL	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
							8	-8
							12	-12
							16	-16
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
							8	-8
							12	-12
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
					0.2	$V_{CCIO} - 0.2$	8	-8
							12	-12
LVCMOS 1.2	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	4	-2
							8	-6
							0.1	-0.1
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5
SSTL25 Class I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCIO} - 0.62$	8	8
SSTL25 Class II	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	NA	NA	NA	NA
SSTL18 Class I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	0.40	$V_{CCIO} - 0.40$	8	8
SSTL18 Class II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	NA	NA	NA	NA
HSTL18 Class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.40	$V_{CCIO} - 0.40$	8	8
HSTL18 Class II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS25R33	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS18R33	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS18R25	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS15R33	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS15R25	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS12R33	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS12R25	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain
LVCMOS10R33	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered ^{9, 12}									
t _{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.535	—	0.670	—	0.830	—	ns
t _{DVA}	Output Data Valid After CLK Output		0.535	—	0.670	—	0.830	—	ns
f _{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	—	462	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	332	—	277	—	231	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned ^{9, 12}									
t _{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.200	—	0.215	—	0.230	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.230	ns
f _{DATA}	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency		—	378	—	315	—	262	MHz
f _{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered ^{9, 12}									
t _{DVB}	Output Data Valid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	0.455	—	0.570	—	0.710	—	ns
t _{DVA}	Output Data Valid After CLK Output		0.455	—	0.570	—	0.710	—	ns
f _{DATA}	DDRX4 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	378	—	315	—	262	MHz
f _{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1 ^{9, 12}									
t _{DIB}	Output Data Invalid Before CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.160	—	0.180	—	0.200	ns
t _{DIA}	Output Data Invalid After CLK Output		—	0.160	—	0.180	—	0.200	ns
f _{DATA}	DDR71 Serial Output Data Speed		—	756	—	630	—	524	Mbps
f _{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	262	MHz
f _{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	75	MHz

Figure 3-5. Receiver RX.CLK.Aligned and MEM DDR Input Waveforms

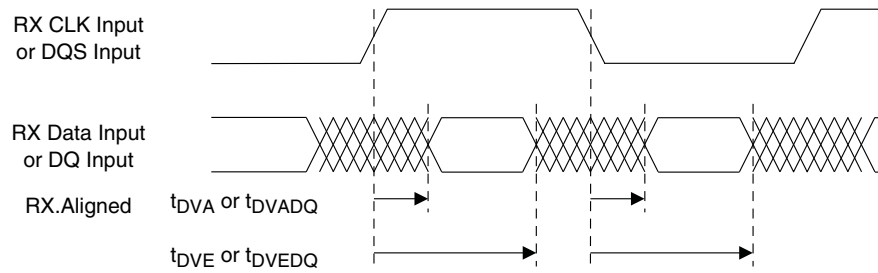


Figure 3-6. Receiver RX.CLK.Centered Waveforms

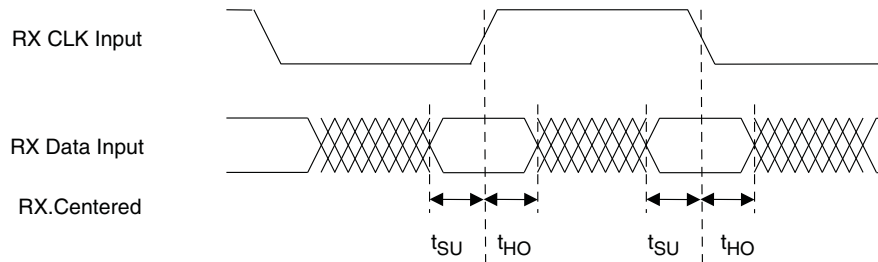


Figure 3-7. Transmitter TX.CLK.Aligned Waveforms

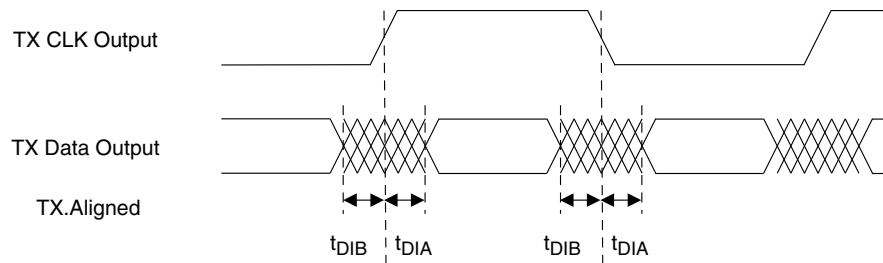
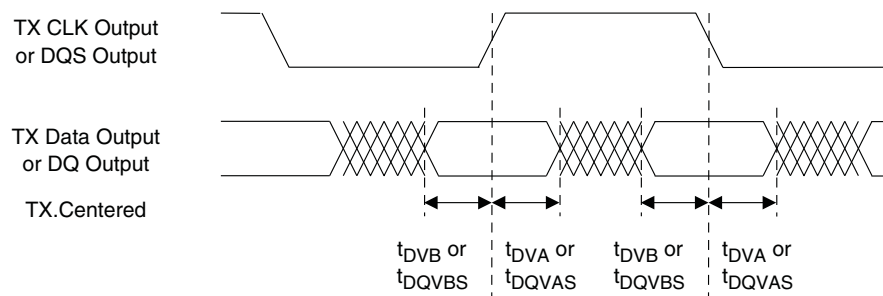


Figure 3-8. Transmitter TX.CLK.Centered and MEM DDR Output Waveforms

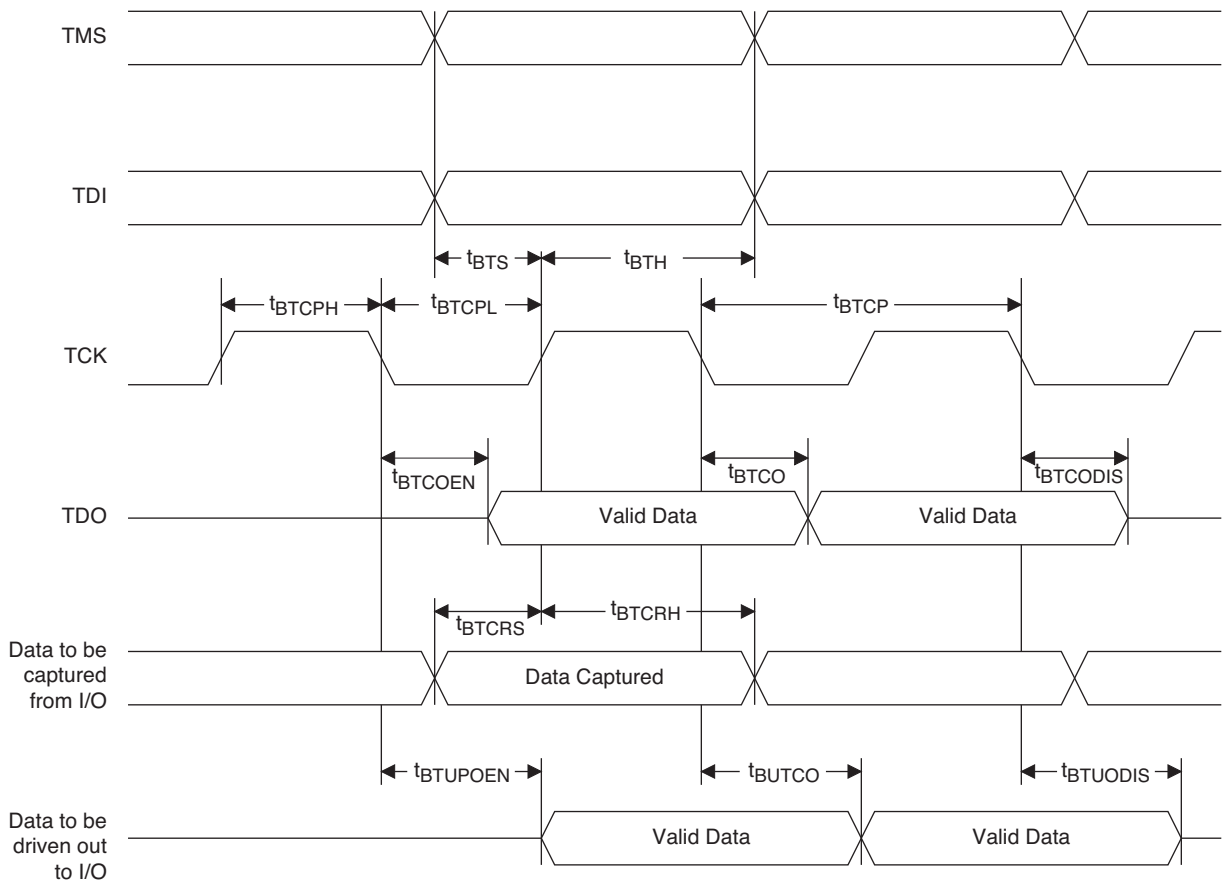


sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)		1.5625	400	MHz
f_{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
f_{VCO}	PLL VCO Frequency		200	800	MHz
f_{PFD}	Phase Detector Input Frequency		7	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Without duty trim selected ³	45	55	%
$t_{DT_TRIM}^7$	Edge Duty Trim Accuracy		-75	75	%
t_{PH}^4	Output Phase Accuracy		-6	6	%
$t_{OPJIT}^{1,8}$	Output Clock Period Jitter	$f_{OUT} > 100$ MHz	—	150	ps p-p
		$f_{OUT} < 100$ MHz	—	0.007	UIPP
	Output Clock Cycle-to-cycle Jitter	$f_{OUT} > 100$ MHz	—	180	ps p-p
		$f_{OUT} < 100$ MHz	—	0.009	UIPP
	Output Clock Phase Jitter	$f_{PFD} > 100$ MHz	—	160	ps p-p
		$f_{PFD} < 100$ MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	$f_{OUT} > 100$ MHz	—	230	ps p-p
		$f_{OUT} < 100$ MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter (Fractional-N)	$f_{OUT} > 100$ MHz	—	230	ps p-p
		$f_{OUT} < 100$ MHz	—	0.12	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	-120	120	ps
t_W	Output Clock Pulse Width	At 90% or 10% ³	0.9	—	ns
$t_{LOCK}^{2,5}$	PLL Lock-in Time		—	15	ms
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}^6	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{STABLE}^5	STANDBY High to PLL Stable		—	15	ms
t_{RST}	RST/RESETM Pulse Width		1	—	ns
t_{RSTREC}	RST Recovery Time		1	—	ns
t_{RST_DIV}	RESETC/D Pulse Width		10	—	ns
t_{RSTREC_DIV}	RESETC/D Recovery Time		1	—	ns
$t_{ROTATE-SETUP}$	PHASESTEP Setup Time		10	—	ns

Figure 3-12. JTAG Port Timing Waveforms



I²C Port Timing Specifications^{1, 2}

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	Maximum SCL clock frequency	—	400	kHz

- MachXO2 supports the following modes:
 - Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)
 - Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)
- Refer to the I²C specification for timing requirements.

SPI Port Timing Specifications¹

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	Maximum SCK clock frequency	—	45	MHz

- Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

Switching Test Conditions

Figure 3-13 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-5.

Figure 3-13. Output Test Load, LVTTTL and LVCMOS Standards

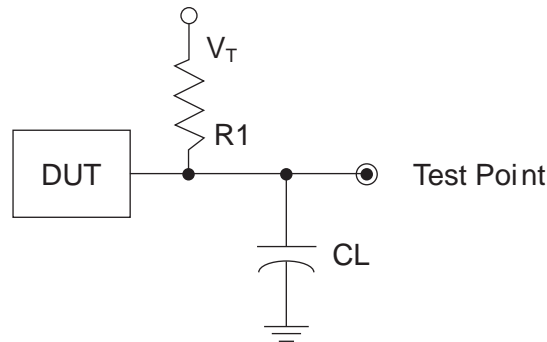


Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R1	CL	Timing Ref.	VT
LVTTTL and LVCMOS settings (L -> H, H -> L)	∞	0pF	LVTTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = V _{CCIO} /2	—
			LVCMOS 1.8 = V _{CCIO} /2	—
			LVCMOS 1.5 = V _{CCIO} /2	—
			LVCMOS 1.2 = V _{CCIO} /2	—
LVTTTL and LVCMOS 3.3 (Z -> H)	188	0pF	1.5 V	V _{OL}
LVTTTL and LVCMOS 3.3 (Z -> L)			1.5 V	V _{OH}
Other LVCMOS (Z -> H)			V _{CCIO} /2	V _{OL}
Other LVCMOS (Z -> L)			V _{CCIO} /2	V _{OH}
LVTTTL + LVCMOS (H -> Z)			V _{OH} - 0.15 V	V _{OL}
LVTTTL + LVCMOS (L -> Z)			V _{OL} - 0.15 V	V _{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32C	256	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-256ZE-2SG32C	256	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-256ZE-3SG32C	256	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-256ZE-1UMG64C	256	1.2 V	–1	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-2UMG64C	256	1.2 V	–2	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-3UMG64C	256	1.2 V	–3	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-1TG100C	256	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-2TG100C	256	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-3TG100C	256	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-1MG132C	256	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-2MG132C	256	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-3MG132C	256	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100C	640	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-2TG100C	640	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-3TG100C	640	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-1MG132C	640	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-2MG132C	640	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-3MG132C	640	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1SG32C	1280	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-2SG32C	1280	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-3SG32C	1280	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-1TG100C	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100C	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100C	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132C	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132C	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132C	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144C	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144C	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144C	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484C	2112	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-5FG484C	2112	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHC-6FG484C	2112	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84C	4320	2.5 V / 3.3 V	–4	Halogen-Free QFN	84	COM
LCMXO2-4000HC-5QN84C	4320	2.5 V / 3.3 V	–5	Halogen-Free QFN	84	COM
LCMXO2-4000HC-6QN84C	4320	2.5 V / 3.3 V	–6	Halogen-Free QFN	84	COM
LCMXO2-4000HC-4MG132C	4320	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-5MG132C	4320	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-6MG132C	4320	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-4000HC-4TG144C	4320	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-5TG144C	4320	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-6TG144C	4320	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-4000HC-4BG256C	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-5BG256C	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-6BG256C	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-4000HC-4FTG256C	4320	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-5FTG256C	4320	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-6FTG256C	4320	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HC-4BG332C	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-5BG332C	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-6BG332C	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-4000HC-4FG484C	4320	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-5FG484C	4320	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HC-6FG484C	4320	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100IR1 ¹	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100IR1 ¹	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100IR1 ¹	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132IR1 ¹	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132IR1 ¹	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132IR1 ¹	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144IR1 ¹	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144IR1 ¹	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144IR1 ¹	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200ZE-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.

For Further Information

A variety of technical notes for the MachXO2 family are available on the Lattice web site.

- TN1198, [Power Estimation and Management for MachXO2 Devices](#)
- TN1199, [MachXO2 sysCLOCK PLL Design and Usage Guide](#)
- TN1201, [Memory Usage Guide for MachXO2 Devices](#)
- TN1202, [MachXO2 sysIO Usage Guide](#)
- TN1203, [Implementing High-Speed Interfaces with MachXO2 Devices](#)
- TN1204, [MachXO2 Programming and Configuration Usage Guide](#)
- TN1205, [Using User Flash Memory and Hardened Control Functions in MachXO2 Devices](#)
- TN1206, [MachXO2 SRAM CRC Error Detection Usage Guide](#)
- TN1207, [Using TraceID in MachXO2 Devices](#)
- TN1074, [PCB Layout Recommendations for BGA Packages](#)
- TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#)
- AN8086, [Designing for Migration from MachXO2-1200-R1 to Standard \(non-R1\) Devices](#)
- AN8066, [Boundary Scan Testability with Lattice sysIO Capability](#)
- [MachXO2 Device Pinout Files](#)
- [Thermal Management](#) document
- [Lattice design tools](#)

For further information on interface standards, refer to the following web sites:

- JEDEC Standards (LVTTTL, LVCMOS, LVDS, DDR, DDR2, LPDDR): www.jedec.org
- PCI: www.pcisig.com