# Lattice Semiconductor Corporation - LCMXO2-1200HC-6TG100CR1 Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 160 |
| Number of Logic Elements/Cells | 1280 |
| Total RAM Bits | 65536 |
| Number of I/O | 79 |
| Number of Gates | - |
| Voltage - Supply | 2.375V ~ 3.465V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-1200hc-6tg100cr1 |

# Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, $I^2C$ controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external $V_{CC}$ supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external $V_{CC}$ supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a “per-pin” basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the $I^2C$ port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO2 family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found in MachXO2-640/U and larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT usage.

The MachXO2 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO2 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks on MachXO2-640U, MachXO2-1200/U and larger devices. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

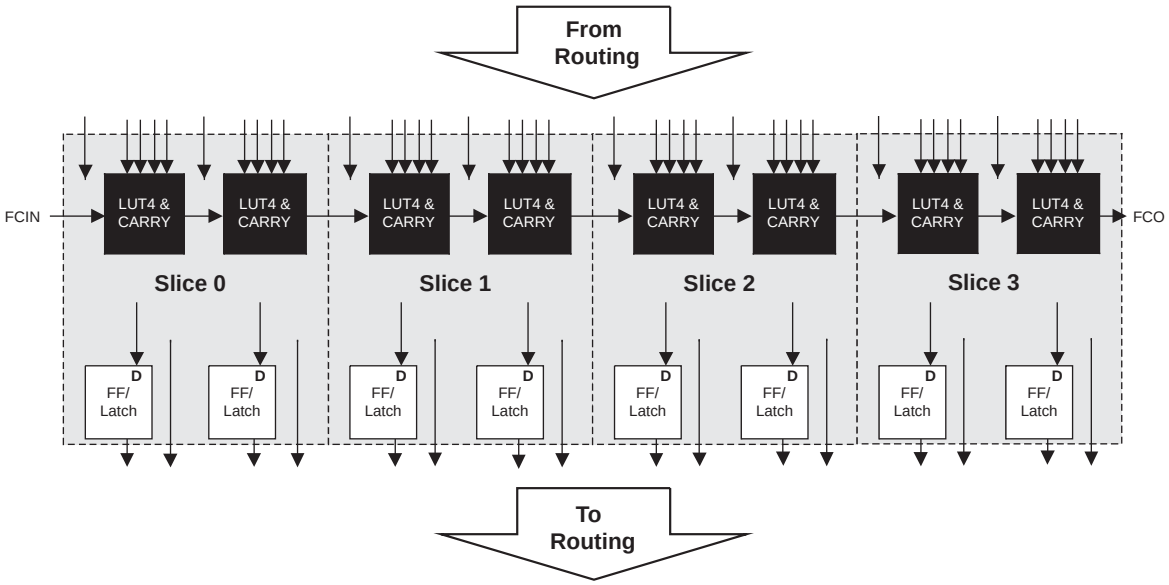
MachXO2 devices provide commonly used hardened functions such as SPI controller, $I^2C$ controller and timer/counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, $I^2C$ and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO2 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

## PFU Blocks

The core of the MachXO2 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

*Figure 2-3. PFU Block Diagram*




## Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

*Table 2-1. Resources and Modes Available per Slice*

| Slice | PFU Block | |
|---|---|---|
| | Resources | Modes |
| Slice 0 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 1 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 2 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 3 | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.

## Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

**Logic Mode**
In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

**Ripple Mode**
Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  — A greater-than-or-equal-to B
  — A not-equal-to B
  — A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

## RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO2 devices support distributed memory initialization.

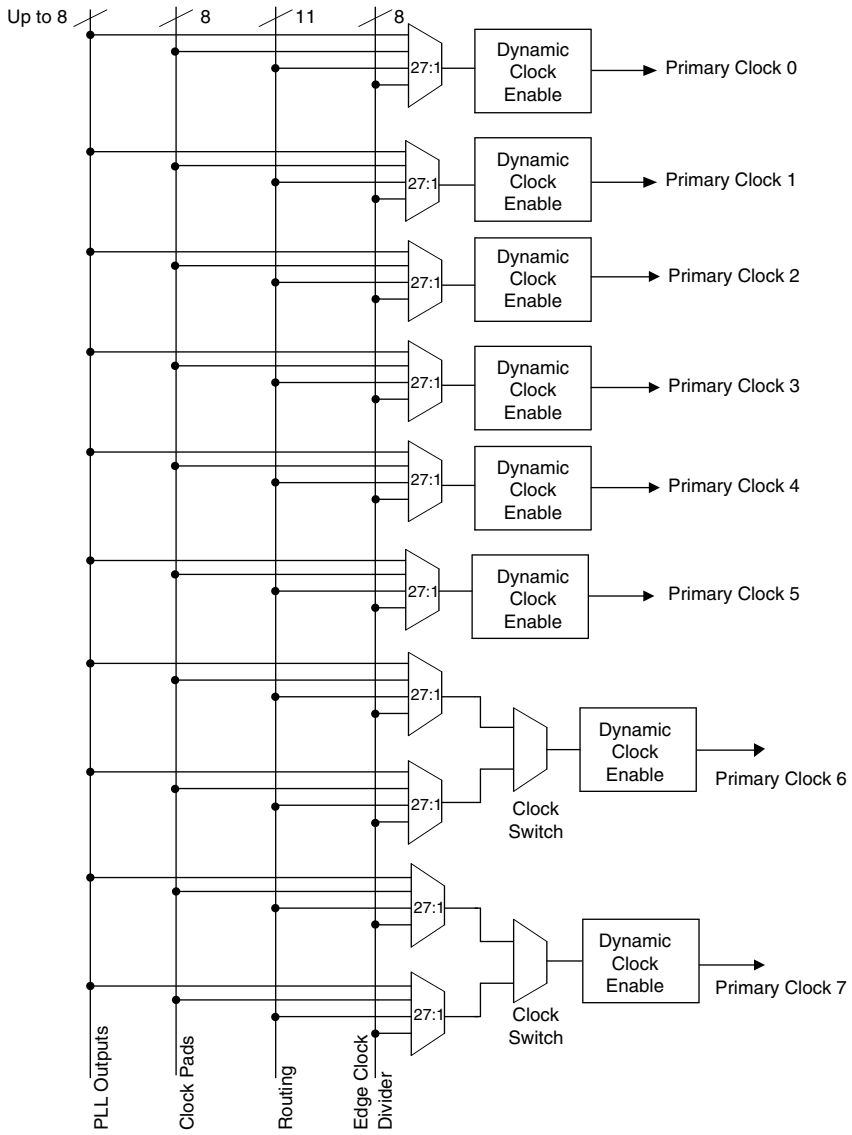
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO2 devices, please see TN1201, Memory Usage Guide for MachXO2 Devices.

***Table 2-3. Number of Slices Required For Implementing Distributed RAM***

| | SPR 16x4 | PDPR 16x4 |
|---|---|---|
| Number of slices | 3 | 3 |

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

*Figure 2-5. Primary Clocks for MachXO2 Devices*




Primary clocks for MachXO2-640U, MachXO2-1200/U and larger devices.

Note: MachXO2-640 and smaller devices do not have inputs from the Edge Clock Divider or PLL and fewer routing inputs. These devices have 17:1 muxes instead of 27:1 muxes.

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO2 External Switching Characteristics table.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.

3. **Read-Before-Write** – When new data is being written, the old contents of the address appears at the output.

**FIFO Configuration**

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

***Table 2-7. Programmable FIFO Flag Ranges***

| Flag Name | Programming Range |
|---|---|
| Full (FF) | 1 to max (up to $2^N$-1) |
| Almost Full (AF) | 1 to Full-1 |
| Almost Empty (AE) | 1 to Full-1 |
| Empty (EF) | 0 |

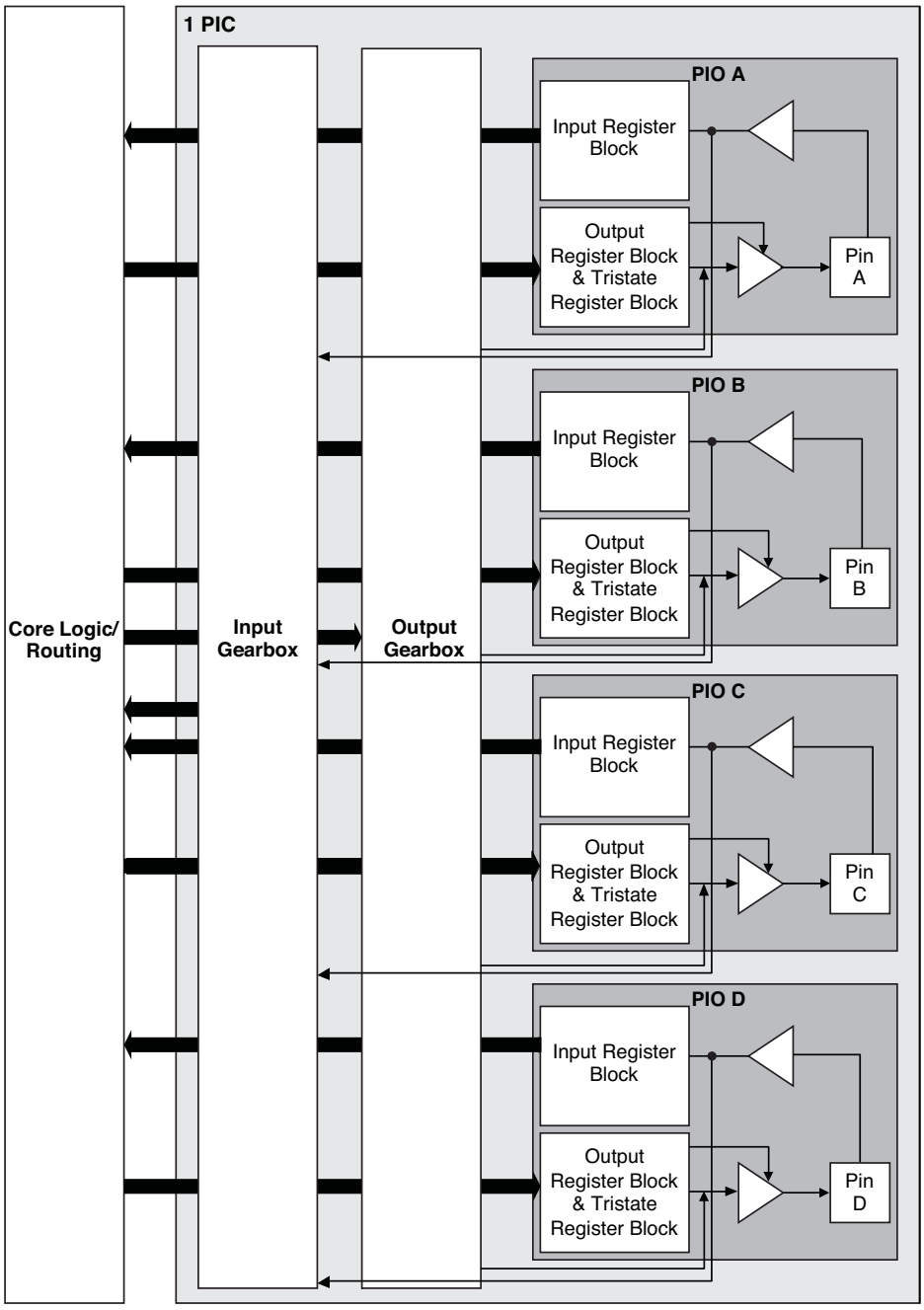
N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

**Memory Core Reset**

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

*Figure 2-11. Group of Four Programmable I/O Cells*




Notes:
1. Input gearbox is available only in PIC on the bottom edge of MachXO2-640U, MachXO2-1200/U and larger devices.
2. Output gearbox is available only in PIC on the top edge of MachXO2-640U, MachXO2-1200/U and larger devices.

*Table 2-13. Supported Output Standards*

| Output Standard | $V_{CCIO}$ (Typ.) |
|---|---|
| **Single-Ended Interfaces** | |
| LVTTL | 3.3 |
| LVCMOS33 | 3.3 |
| LVCMOS25 | 2.5 |
| LVCMOS18 | 1.8 |
| LVCMOS15 | 1.5 |
| LVCMOS12 | 1.2 |
| LVCMOS33, Open Drain | — |
| LVCMOS25, Open Drain | — |
| LVCMOS18, Open Drain | — |
| LVCMOS15, Open Drain | — |
| LVCMOS12, Open Drain | — |
| PCI33 | 3.3 |
| SSTL25 (Class I) | 2.5 |
| SSTL18 (Class I) | 1.8 |
| HSTL18(Class I) | 1.8 |
| **Differential Interfaces** | |
| LVDS[1, 2] | 2.5, 3.3 |
| BLVDS, MLVDS, RSDS [2] | 2.5 |
| LVPECL[2] | 3.3 |
| MIPI[2] | 2.5 |
| Differential SSTL18 | 1.8 |
| Differential SSTL25 | 2.5 |
| Differential HSTL18 | 1.8 |

1. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.
2. These interfaces can be emulated with external resistors in all devices.

## sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO2-1200U, MachXO2-2000/U and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO2-1200 and lower density devices have four banks (one bank per side). Figures 2-18 and 2-19 show the sysIO banks and their associated supplies for all devices.

## RSDS

The MachXO2 family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

***Figure 3-4. RSDS (Reduced Swing Differential Standard)***

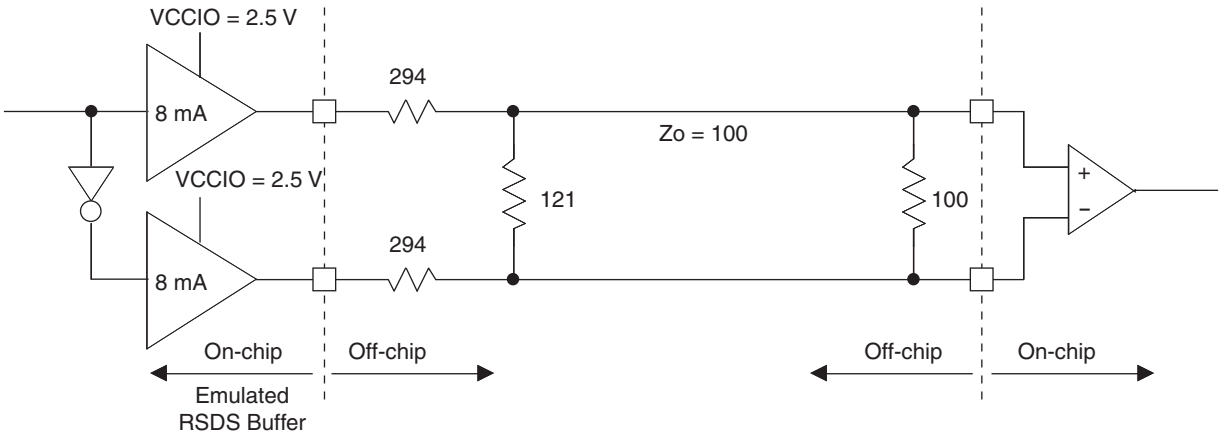



***Table 3-4. RSDS DC Conditions***

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ohms |
| $R_S$ | Driver series resistor | 294 | Ohms |
| $R_P$ | Driver parallel resistor | 121 | Ohms |
| $R_T$ | Receiver termination | 100 | Ohms |
| $V_{OH}$ | Output high voltage | 1.35 | V |
| $V_{OL}$ | Output low voltage | 1.15 | V |
| $V_{OD}$ | Output differential voltage | 0.20 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 101.5 | Ohms |
| $I_{DC}$ | DC output current | 3.66 | mA |

# Typical Building Block Function Performance – HC/HE Devices[1]

## Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

| Function | -6 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit decoder | 8.9 | ns |
| 4:1 MUX | 7.5 | ns |
| 16:1 MUX | 8.3 | ns |

## Register-to-Register Performance

| Function | -6 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16:1 MUX | 412 | MHz |
| 16-bit adder | 297 | MHz |
| 16-bit counter | 324 | MHz |
| 64-bit counter | 161 | MHz |
| **Embedded Memory Functions** | | |
| 1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers) | 183 | MHz |
| **Distributed Memory Functions** | | |
| 16x4 Pseudo-Dual Port RAM (one PFU) | 500 | MHz |

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

## Maximum sysIO Buffer Performance

| I/O Standard | Max. Speed | Units |
|---|---|---|
| LVDS25 | 400 | MHz |
| LVDS25E | 150 | MHz |
| RSDS25 | 150 | MHz |
| RSDS25E | 150 | MHz |
| BLVDS25 | 150 | MHz |
| BLVDS25E | 150 | MHz |
| MLVDS25 | 150 | MHz |
| MLVDS25E | 150 | MHz |
| LVPECL33 | 150 | MHz |
| LVPECL33E | 150 | MHz |
| SSTL25_I | 150 | MHz |
| SSTL25_II | 150 | MHz |
| SSTL25D_I | 150 | MHz |
| SSTL25D_II | 150 | MHz |
| SSTL18_I | 150 | MHz |
| SSTL18_II | 150 | MHz |
| SSTL18D_I | 150 | MHz |
| SSTL18D_II | 150 | MHz |
| HSTL18_I | 150 | MHz |
| HSTL18_II | 150 | MHz |
| HSTL18D_I | 150 | MHz |
| HSTL18D_II | 150 | MHz |
| PCI33 | 134 | MHz |
| LVTTL33 | 150 | MHz |
| LVTTL33D | 150 | MHz |
| LVCMOS33 | 150 | MHz |
| LVCMOS33D | 150 | MHz |
| LVCMOS25 | 150 | MHz |
| LVCMOS25D | 150 | MHz |
| LVCMOS25R33 | 150 | MHz |
| LVCMOS18 | 150 | MHz |
| LVCMOS18D | 150 | MHz |
| LVCMOS18R33 | 150 | MHz |
| LVCMOS18R25 | 150 | MHz |
| LVCMOS15 | 150 | MHz |
| LVCMOS15D | 150 | MHz |
| LVCMOS15R33 | 150 | MHz |
| LVCMOS15R25 | 150 | MHz |
| LVCMOS12 | 91 | MHz |
| LVCMOS12D | 91 | MHz |

# MachXO2 External Switching Characteristics – HC/HE Devices[1, 2, 3, 4, 5, 6, 7]

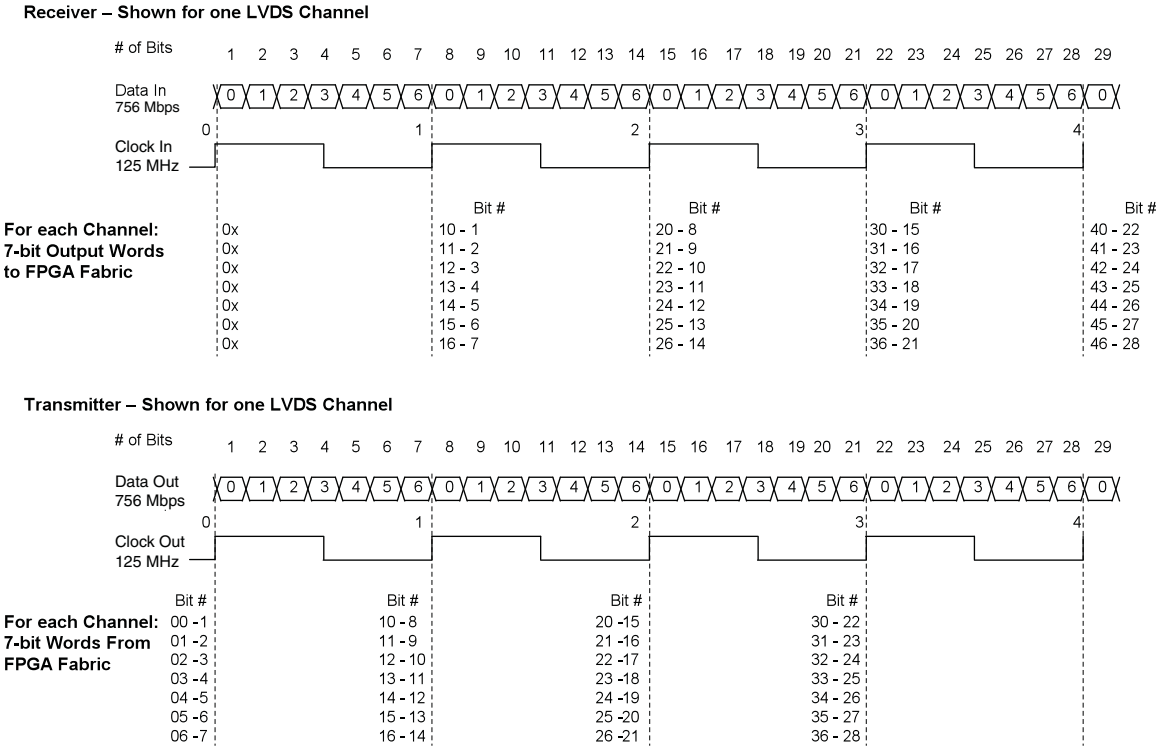
**Over Recommended Operating Conditions**

| Parameter | Description | Device | –6 | | –5 | | –4 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Clocks** | | | | | | | | | |
| **Primary Clocks** | | | | | | | | | |
| $f_{MAX\_PRI}$[8] | Frequency for Primary Clock Tree | All MachXO2 devices | — | 388 | — | 323 | — | 269 | MHz |
| $t_{W\_PRI}$ | Clock Pulse Width for Primary Clock | All MachXO2 devices | 0.5 | — | 0.6 | — | 0.7 | — | ns |
| $t_{SKEW\_PRI}$ | Primary Clock Skew Within a Device | MachXO2-256HC-HE | — | 912 | — | 939 | — | 975 | ps |
| | | MachXO2-640HC-HE | — | 844 | — | 871 | — | 908 | ps |
| | | MachXO2-1200HC-HE | — | 868 | — | 902 | — | 951 | ps |
| | | MachXO2-2000HC-HE | — | 867 | — | 897 | — | 941 | ps |
| | | MachXO2-4000HC-HE | — | 865 | — | 892 | — | 931 | ps |
| | | MachXO2-7000HC-HE | — | 902 | — | 942 | — | 989 | ps |
| **Edge Clock** | | | | | | | | | |
| $f_{MAX\_EDGE}$[8] | Frequency for Edge Clock | MachXO2-1200 and larger devices | — | 400 | — | 333 | — | 278 | MHz |
| **Pin-LUT-Pin Propagation Delay** | | | | | | | | | |
| $t_{PD}$ | Best case propagation delay through one LUT-4 | All MachXO2 devices | — | 6.72 | — | 6.96 | — | 7.24 | ns |
| **General I/O Pin Parameters (Using Primary Clock without PLL)** | | | | | | | | | |
| $t_{CO}$ | Clock to Output – PIO Output Register | MachXO2-256HC-HE | — | 7.13 | — | 7.30 | — | 7.57 | ns |
| | | MachXO2-640HC-HE | — | 7.15 | — | 7.30 | — | 7.57 | ns |
| | | MachXO2-1200HC-HE | — | 7.44 | — | 7.64 | — | 7.94 | ns |
| | | MachXO2-2000HC-HE | — | 7.46 | — | 7.66 | — | 7.96 | ns |
| | | MachXO2-4000HC-HE | — | 7.51 | — | 7.71 | — | 8.01 | ns |
| | | MachXO2-7000HC-HE | — | 7.54 | — | 7.75 | — | 8.06 | ns |
| $t_{SU}$ | Clock to Data Setup – PIO Input Register | MachXO2-256HC-HE | –0.06 | — | –0.06 | — | –0.06 | — | ns |
| | | MachXO2-640HC-HE | –0.06 | — | –0.06 | — | –0.06 | — | ns |
| | | MachXO2-1200HC-HE | –0.17 | — | –0.17 | — | –0.17 | — | ns |
| | | MachXO2-2000HC-HE | –0.20 | — | –0.20 | — | –0.20 | — | ns |
| | | MachXO2-4000HC-HE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| | | MachXO2-7000HC-HE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| $t_{H}$ | Clock to Data Hold – PIO Input Register | MachXO2-256HC-HE | 1.75 | — | 1.95 | — | 2.16 | — | ns |
| | | MachXO2-640HC-HE | 1.75 | — | 1.95 | — | 2.16 | — | ns |
| | | MachXO2-1200HC-HE | 1.88 | — | 2.12 | — | 2.36 | — | ns |
| | | MachXO2-2000HC-HE | 1.89 | — | 2.13 | — | 2.37 | — | ns |
| | | MachXO2-4000HC-HE | 1.94 | — | 2.18 | — | 2.43 | — | ns |
| | | MachXO2-7000HC-HE | 1.98 | — | 2.23 | — | 2.49 | — | ns |

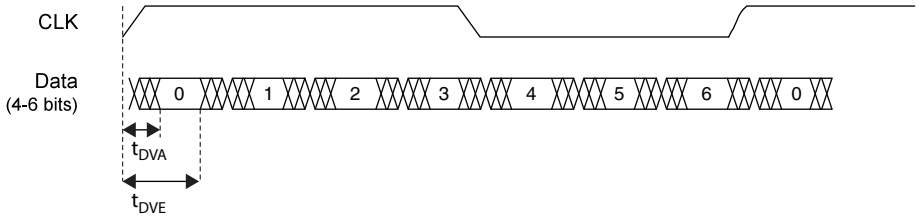
| Parameter | Description | Device | –3 | | –2 | | –1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **LPDDR**[9, 12] | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only.[13] | — | 0.349 | — | 0.381 | — | 0.396 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.665 | — | 0.630 | — | 0.613 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM LPDDR Serial Data Speed | | — | 120 | — | 110 | — | 96 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 60 | — | 55 | — | 48 | MHz |
| $f_{LPDDR}$ | LPDDR Data Transfer Rate | | 0 | 120 | 0 | 110 | 0 | 96 | Mbps |
| **DDR**[9, 12] | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only.[13] | — | 0.347 | — | 0.374 | — | 0.393 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.665 | — | 0.637 | — | 0.616 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM DDR Serial Data Speed | | — | 140 | — | 116 | — | 98 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 70 | — | 58 | — | 49 | MHz |
| $f_{MEM\_DDR}$ | MEM DDR Data Transfer Rate | | N/A | 140 | N/A | 116 | N/A | 98 | Mbps |
| **DDR2**[9, 12] | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only.[13] | — | 0.372 | — | 0.394 | — | 0.410 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.690 | — | 0.658 | — | 0.618 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM DDR Serial Data Speed | | — | 140 | — | 116 | — | 98 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 70 | — | 58 | — | 49 | MHz |
| $f_{MEM\_DDR2}$ | MEM DDR2 Data Transfer Rate | | N/A | 140 | N/A | 116 | N/A | 98 | Mbps |

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\ ns)/2$.
7. The $t_{SU\_DEL}$ and $t_{H\_DEL}$ values use the SCLK_ZERHOLD default step size. Each step is 167 ps (–3), 182 ps (–2), 195 ps (–1).
8. This number for general purpose usage. Duty cycle tolerance is +/–10%.
9. Duty cycle is +/– 5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. High-speed DDR and LVDS not supported in SG32 (32-Pin QFN) packages.
12. Advance information for MachXO2 devices in 48 QFN packages.
13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

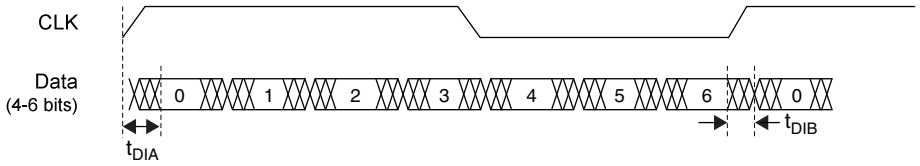
### Figure 3-9. GDDR71 Video Timing Waveforms




### Figure 3-10. Receiver GDDR71_RX. Waveforms




### Figure 3-11. Transmitter GDDR71_TX. Waveforms



## Flash Download Time[1, 2]

| Symbol | Parameter | Device | Typ. | Units |
|---|---|---|---|---|
| $t_{REFRESH}$ | POR to Device I/O Active | LCMXO2-256 | 0.6 | ms |
| | | LCMXO2-640 | 1.0 | ms |
| | | LCMXO2-640U | 1.9 | ms |
| | | LCMXO2-1200 | 1.9 | ms |
| | | LCMXO2-1200U | 1.4 | ms |
| | | LCMXO2-2000 | 1.4 | ms |
| | | LCMXO2-2000U | 2.4 | ms |
| | | LCMXO2-4000 | 2.4 | ms |
| | | LCMXO2-7000 | 3.8 | ms |

1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.
2. The Flash download time is measured starting from the maximum voltage of POR trip point.

## JTAG Port Timing Specifications

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $f_{MAX}$ | TCK clock frequency | — | 25 | MHz |
| $t_{BTCPH}$ | TCK [BSCAN] clock pulse width high | 20 | — | ns |
| $t_{BTCPL}$ | TCK [BSCAN] clock pulse width low | 20 | — | ns |
| $t_{BTS}$ | TCK [BSCAN] setup time | 10 | — | ns |
| $t_{BTH}$ | TCK [BSCAN] hold time | 8 | — | ns |
| $t_{BTCO}$ | TAP controller falling edge of clock to valid output | — | 10 | ns |
| $t_{BTCODIS}$ | TAP controller falling edge of clock to valid disable | — | 10 | ns |
| $t_{BTCOEN}$ | TAP controller falling edge of clock to valid enable | — | 10 | ns |
| $t_{BTCRS}$ | BSCAN test capture register setup time | 8 | — | ns |
| $t_{BTCRH}$ | BSCAN test capture register hold time | 20 | — | ns |
| $t_{BUTCO}$ | BSCAN test update register, falling edge of clock to valid output | — | 25 | ns |
| $t_{BTUODIS}$ | BSCAN test update register, falling edge of clock to valid disable | — | 25 | ns |
| $t_{BTUPOEN}$ | BSCAN test update register, falling edge of clock to valid enable | — | 25 | ns |

## Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-256ZE-1SG32I | 256 | 1.2 V | –1 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256ZE-2SG32I | 256 | 1.2 V | –2 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256ZE-3SG32I | 256 | 1.2 V | –3 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256ZE-1UMG64I | 256 | 1.2 V | –1 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256ZE-2UMG64I | 256 | 1.2 V | –2 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256ZE-3UMG64I | 256 | 1.2 V | –3 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256ZE-1TG100I | 256 | 1.2 V | –1 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256ZE-2TG100I | 256 | 1.2 V | –2 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256ZE-3TG100I | 256 | 1.2 V | –3 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256ZE-1MG132I | 256 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-256ZE-2MG132I | 256 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-256ZE-3MG132I | 256 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-640ZE-1TG100I | 640 | 1.2 V | –1 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640ZE-2TG100I | 640 | 1.2 V | –2 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640ZE-3TG100I | 640 | 1.2 V | –3 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640ZE-1MG132I | 640 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640ZE-2MG132I | 640 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640ZE-3MG132I | 640 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-1200ZE-1UWG25ITR[1] | 1280 | 1.2 V | –1 | Halogen-Free WLCSP | 25 | IND |
| LCMXO2-1200ZE-1UWG25ITR50[3] | 1280 | 1.2 V | –1 | Halogen-Free WLCSP | 25 | IND |
| LCMXO2-1200ZE-1UWG25ITR1K[2] | 1280 | 1.2 V | –1 | Halogen-Free WLCSP | 25 | IND |
| LCMXO2-1200ZE-1SG32I | 1280 | 1.2 V | –1 | Halogen-Free QFN | 32 | IND |
| LCMXO2-1200ZE-2SG32I | 1280 | 1.2 V | –2 | Halogen-Free QFN | 32 | IND |
| LCMXO2-1200ZE-3SG32I | 1280 | 1.2 V | –3 | Halogen-Free QFN | 32 | IND |
| LCMXO2-1200ZE-1TG100I | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-2TG100I | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-3TG100I | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-1MG132I | 1280 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-2MG132I | 1280 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-3MG132I | 1280 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-1TG144I | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200ZE-2TG144I | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200ZE-3TG144I | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 144 | IND |

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000HC-4QN84I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000HC-5QN84I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000HC-6QN84I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000HC-4TG144I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HC-5TG144I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HC-6TG144I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HC-4MG132I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HC-5MG132I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HC-6MG132I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HC-4BG256I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HC-5BG256I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HC-6BG256I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HC-4FTG256I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HC-5FTG256I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HC-6FTG256I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HC-4BG332I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HC-5BG332I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HC-6BG332I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HC-4FG484I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HC-5FG484I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HC-6FG484I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-7000HC-4TG144I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HC-5TG144I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HC-6TG144I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HC-4BG256I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HC-5BG256I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HC-6BG256I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HC-4FTG256I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HC-5FTG256I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HC-6FTG256I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HC-4BG332I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HC-5BG332I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HC-6BG332I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HC-4FG400I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 400 | IND |
| LCMXO2-7000HC-5FG400I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 400 | IND |
| LCMXO2-7000HC-6FG400I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 400 | IND |
| LCMXO2-7000HC-4FG484I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HC-5FG484I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HC-6FG484I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | IND |

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-1200HC-4TG100IR1[1] | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200HC-5TG100IR1[1] | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200HC-6TG100IR1[1] | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200HC-4MG132IR1[1] | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200HC-5MG132IR1[1] | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200HC-6MG132IR1[1] | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200HC-4TG144IR1[1] | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200HC-5TG144IR1[1] | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200HC-6TG144IR1[1] | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |

1. Specifications for the “LCMXO2-1200HC-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

| Date | Version | Section | Change Summary |
|---|---|---|---|
| May 2014 | 2.5 | Architecture | Updated TransFR (Transparent Field Reconfiguration) section.<br>Updated TransFR description for PLL use during background Flash programming. |
| February 2014 | 02.4 | Introduction | Included the 49 WLCSP package in the MachXO2 Family Selection Guide table. |
| | | Architecture | Added information to Standby Mode and Power Saving Options section. |
| | | Pinout Information | Added the XO2-2000 49 WLCSP in the Pinout Information Summary table. |
| | | Ordering Information | Added UW49 package in MachXO2 Part Number Description. |
| | | | Added and LCMXO2-2000ZE-1UWG49CTR in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging section. |
| | | | Added and LCMXO2-2000ZE-1UWG49ITR in Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. |
| December 2013 | 02.3 | Architecture | Updated information on CLKOS output divider in sysCLOCK Phase Locked Loops (PLLs) section. |
| | | DC and Switching Characteristics | Updated Static Supply Current – ZE Devices table. |
| | | | Updated footnote 4 in sysIO Single-Ended DC Electrical Characteristics table; Updated $V_{IL}$ Max. (V) data for LVCMOS 25 and LVCMOS 28. |
| | | | Updated $V_{OS}$ test condition in sysIO Differential Electrical Characteristics - LVDS table. |
| September 2013 | 02.2 | Architecture | Removed $I^2C$ Clock-Stretching feature per PCN #10A-13. |
| | | | Removed information on PDPR memory in RAM Mode section. |
| | | | Updated Supported Input Standards table. |
| | | DC and Switching Characteristics | Updated Power-On-Reset Voltage Levels table. |
| June 2013 | 02.1 | Architecture | Architecture Overview – Added information on the state of the register on power up and after configuration. |
| | | | sysCLOCK Phase Locked Loops (PLLs) section – Added missing cross reference to sysCLOCK PLL Timing table. |
| | | DC and Switching Characteristics | Added slew rate information to footnote 2 of the MachXO2 External Switching Characteristics – HC/HE Devices and the MachXO2 External Switching Characteristics – ZE Devices tables. |
| | | | Power-On-Reset Voltage Levels table – Added symbols. |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| May 2011 | 01.3 | Multiple | Replaced “SED” with “SRAM CRC Error Detection” throughout the document. |
| | | DC and Switching Characteristics | Added footnote 1 to Program Erase Specifications table. |
| | | Pinout Information | Updated Pin Information Summary tables. |
| | | | Signal name SO/SISPISO changed to SO/SPISO in the Signal Descriptions table. |
| April 2011 | 01.2 | — | Data sheet status changed from Advance to Preliminary. |
| | | Introduction | Updated MachXO2 Family Selection Guide table. |
| | | Architecture | Updated Supported Input Standards table. |
| | | | Updated sysMEM Memory Primitives diagram. |
| | | | Added differential SSTL and HSTL IO standards. |
| | | DC and Switching Characteristics | Updates following parameters: POR voltage levels, DC electrical characteristics, static supply current for ZE/HE/HC devices, static power consumption contribution of different components – ZE devices, programming and erase Flash supply current. |
| | | | Added VREF specifications to sysIO recommended operating conditions. |
| | | | Updating timing information based on characterization. |
| | | | Added differential SSTL and HSTL IO standards. |
| | | Ordering Information | Added Ordering Part Numbers for R1 devices, and devices in WLCSP packages. |
| | | | Added R1 device specifications. |
| January 2011 | 01.1 | All | Included ultra-high I/O devices. |
| | | DC and Switching Characteristics | Recommended Operating Conditions table – Added footnote 3. |
| | | | DC Electrical Characteristics table – Updated data for $I_{IL}$, $I_{IH}$. $V_{HYST}$ typical values updated. |
| | | | Generic DDRX2 Outputs with Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for $T_{DIA}$ and $T_{DIB}$. |
| | | | Generic DDRX4 Outputs with Clock and Data Aligned at Pin (GDDRX4_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for $T_{DIA}$ and $T_{DIB}$. |
| | | | Power-On-Reset Voltage Levels table - clarified note 3. |
| | | | Clarified VCCIO related recommended operating conditions specifications. |
| | | | Added power supply ramp rate requirements. |
| | | | Added Power Supply Ramp Rates table. |
| | | | Updated Programming/Erase Specifications table. |
| | | | Removed references to $V_{CCP}$. |
| | | Pinout Information | Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables. |
| | | | Removed references to $V_{CCP}$. |
| November 2010 | 01.0 | — | Initial release. |