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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	75776
Number of I/O	206
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmx02-1200uhc-5ftg256i

Introduction

The MachXO2 family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I²C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external V_{CC} supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external V_{CC} supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/Os.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a “per-pin” basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I²C port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO2 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO2 devices, please see TN1201, [Memory Usage Guide for MachXO2 Devices](#).

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16x4	PDPR 16x4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.
3. **Read-Before-Write** – When new data is being written, the old contents of the address appears at the output.

FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

Table 2-7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2^N-1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

Table 2-11. I/O Support Device by Device

	MachXO2-256, MachXO2-640	MachXO2-640U, MachXO2-1200	MachXO2-1200U MachXO2-2000/U, MachXO2-4000, MachXO2-7000
Number of I/O Banks	4	4	6
Type of Input Buffers	Single-ended (all I/O banks) Differential Receivers (all I/O banks)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)
Types of Output Buffers	Single-ended buffers with complementary outputs (all I/O banks)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)
Differential Output Emulation Capability	All I/O banks	All I/O banks	All I/O banks
PCI Clamp Support	No	Clamp on bottom side only	Clamp on bottom side only

Table 2-12. Supported Input Standards

Input Standard	VCCIO (Typ.)				
	3.3 V	2.5 V	1.8 V	1.5	1.2 V
Single-Ended Interfaces					
LVTTTL	✓	✓ ²	✓ ²	✓ ²	
LVC MOS33	✓	✓ ²	✓ ²	✓ ²	
LVC MOS25	✓ ²	✓	✓ ²	✓ ²	
LVC MOS18	✓ ²	✓ ²	✓	✓ ²	
LVC MOS15	✓ ²	✓ ²	✓ ²	✓	✓ ²
LVC MOS12	✓ ²	✓ ²	✓ ²	✓ ²	✓
PCI ¹	✓				
SSTL18 (Class I, Class II)	✓	✓	✓		
SSTL25 (Class I, Class II)	✓	✓			
HSTL18 (Class I, Class II)	✓	✓	✓		
Differential Interfaces					
LVDS	✓	✓			
BLVDS, MVDS, LVPECL, RSDS	✓	✓			
MIPI ³	✓	✓			
Differential SSTL18 Class I, II	✓	✓	✓		
Differential SSTL25 Class I, II	✓	✓			
Differential HSTL18 Class I, II	✓	✓	✓		

1. Bottom banks of MachXO2-640U, MachXO2-1200/U and higher density devices only.

2. Reduced functionality. Refer to TN1202, [MachXO2 sysIO Usage Guide](#) for more detail.

3. These interfaces can be emulated with external resistors in all devices.

Table 2-13. Supported Output Standards

Output Standard	V _{CCIO} (Typ.)
Single-Ended Interfaces	
LVTTL	3.3
LVC MOS33	3.3
LVC MOS25	2.5
LVC MOS18	1.8
LVC MOS15	1.5
LVC MOS12	1.2
LVC MOS33, Open Drain	—
LVC MOS25, Open Drain	—
LVC MOS18, Open Drain	—
LVC MOS15, Open Drain	—
LVC MOS12, Open Drain	—
PCI33	3.3
SSTL25 (Class I)	2.5
SSTL18 (Class I)	1.8
HSTL18(Class I)	1.8
Differential Interfaces	
LVDS ^{1,2}	2.5, 3.3
BLVDS, MLVDS, RSDS ²	2.5
LVPECL ²	3.3
MIPI ²	2.5
Differential SSTL18	1.8
Differential SSTL25	2.5
Differential HSTL18	1.8

1. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.

2. These interfaces can be emulated with external resistors in all devices.

sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO2-1200U, MachXO2-2000/U and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO2-1200 and lower density devices have four banks (one bank per side). Figures 2-18 and 2-19 show the sysIO banks and their associated supplies for all devices.



MachXO2 Family Data Sheet

DC and Switching Characteristics

March 2017

Data Sheet DS1035

Absolute Maximum Ratings^{1, 2, 3}

	MachXO2 ZE/HE (1.2 V)	MachXO2 HC (2.5 V / 3.3 V)
Supply Voltage V_{CC}	–0.5 V to 1.32 V	–0.5 V to 3.75 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied ^{4, 5}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied ⁴	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature (T_J)	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to ($V_{IHMAX} + 2$) volts is permitted for a duration of <20 ns.
5. The dual function I²C pins SCL and SDA are limited to –0.25 V to 3.75 V or to –0.3 V with a duration of <20 ns.

Recommended Operating Conditions¹

Symbol	Parameter	Min.	Max.	Units
V_{CC}^1	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V / 3.3 V Devices	2.375	3.6	V
$V_{CCIO}^{1, 2, 3}$	I/O Driver Supply Voltage	1.14	3.6	V
t_{JCOM}	Junction Temperature Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature Industrial Operation	–40	100	°C

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.

Power Supply Ramp Rates¹

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.01	—	100	V/ms

1. Assumes monotonic ramp rates.

Static Supply Current – HC/HE Devices^{1, 2, 3, 6}

Symbol	Parameter	Device	Typ. ⁴	Units
I_{CC}	Core Power Supply	LCMXO2-256HC	1.15	mA
		LCMXO2-640HC	1.84	mA
		LCMXO2-640UHC	3.48	mA
		LCMXO2-1200HC	3.49	mA
		LCMXO2-1200UHC	4.80	mA
		LCMXO2-2000HC	4.80	mA
		LCMXO2-2000UHC	8.44	mA
		LCMXO2-4000HC	8.45	mA
		LCMXO2-7000HC	12.87	mA
		LCMXO2-2000HE	1.39	mA
		LCMXO2-4000HE	2.55	mA
		LCMXO2-7000HE	4.06	mA
I_{CCIO}	Bank Power Supply ⁵ $V_{CCIO} = 2.5\text{ V}$	All devices	0	mA

- For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).
- Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.
- Frequency = 0 MHz.
- $T_J = 25\text{ }^{\circ}\text{C}$, power supplies at nominal voltage.
- Does not include pull-up/pull-down.
- To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Programming and Erase Flash Supply Current – HC/HE Devices^{1, 2, 3, 4}

Symbol	Parameter	Device	Typ. ⁵	Units
I_{CC}	Core Power Supply	LCMXO2-256HC	14.6	mA
		LCMXO2-640HC	16.1	mA
		LCMXO2-640UHC	18.8	mA
		LCMXO2-1200HC	18.8	mA
		LCMXO2-1200UHC	22.1	mA
		LCMXO2-2000HC	22.1	mA
		LCMXO2-2000UHC	26.8	mA
		LCMXO2-4000HC	26.8	mA
		LCMXO2-7000HC	33.2	mA
		LCMXO2-2000HE	18.3	mA
		LCMXO2-2000UHE	20.4	mA
		LCMXO2-4000HE	20.4	mA
		LCMXO2-7000HE	23.9	mA
I_{CCIO}	Bank Power Supply ⁶	All devices	0	mA

- For further information on supply current, please refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).
- Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
- Typical user pattern.
- JTAG programming is at 25 MHz.
- $T_J = 25\text{ }^{\circ}\text{C}$, power supplies at nominal voltage.
- Per bank. $V_{CCIO} = 2.5\text{ V}$. Does not include pull-up/pull-down.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max. ⁴ (mA)	I_{OH} Max. ⁴ (mA)
	Min. (V) ³	Max. (V)	Min. (V)	Max. (V)				
LVC MOS10R25	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain

1. MachXO2 devices allow LVC MOS inputs to be placed in I/O banks where V_{CCIO} is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO2 devices do not meet the relevant JEDEC specification are documented in the table below.
2. MachXO2 devices allow for LVC MOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1202, [MachXO2 sysIO Usage Guide](#).
3. The dual function I²C pins SCL and SDA are limited to a V_{IL} min of -0.25 V or to -0.3 V with a duration of <10 ns.
4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive V_{CCIO} or GND pad connections, or between the last V_{CCIO} or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of $n * 8$ mA. "n" is the number of I/O pads between the two consecutive bank V_{CCIO} or GND connections or between the last V_{CCIO} and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

Input Standard	V_{CCIO} (V)	V_{IL} Max. (V)
LVC MOS 33	1.5	0.685
LVC MOS 25	1.5	0.687
LVC MOS 18	1.5	0.655

sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of MachXO2-640U, MachXO2-1200/U and higher density devices in the MachXO2 PLD family.

LVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP} V_{INM}	Input Voltage	$V_{CCIO} = 3.3$ V	0	—	2.605	V
		$V_{CCIO} = 2.5$ V	0	—	2.05	V
V_{THD}	Differential Input Threshold		±100	—		mV
V_{CM}	Input Common Mode Voltage	$V_{CCIO} = 3.3$ V	0.05	—	2.6	V
		$V_{CCIO} = 2.5$ V	0.05	—	2.0	V
I_{IN}	Input current	Power on	—	—	±10	μA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	$R_T = 100$ Ohm	—	1.375	—	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	$R_T = 100$ Ohm	0.90	1.025	—	V
V_{OD}	Output voltage differential	$(V_{OP} - V_{OM})$, $R_T = 100$ Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	$(V_{OP} + V_{OM})/2$, $R_T = 100$ Ohm	1.125	1.20	1.395	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	$V_{OD} = 0$ V driver outputs shorted	—	—	24	mA

Typical Building Block Function Performance – ZE Devices¹

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–3 Timing	Units
Basic Functions		
16-bit decoder	13.9	ns
4:1 MUX	10.9	ns
16:1 MUX	12.0	ns

Register-to-Register Performance

Function	–3 Timing	Units
Basic Functions		
16:1 MUX	191	MHz
16-bit adder	134	MHz
16-bit counter	148	MHz
64-bit counter	77	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	90	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	214	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

MachXO2 External Switching Characteristics – ZE Devices^{1, 2, 3, 4, 5, 6, 7}

Over Recommended Operating Conditions

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f _{MAX_PRI} ⁸	Frequency for Primary Clock Tree	All MachXO2 devices	—	150	—	125	—	104	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	1.00	—	1.20	—	1.40	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO2-256ZE	—	1250	—	1272	—	1296	ps
		MachXO2-640ZE	—	1161	—	1183	—	1206	ps
		MachXO2-1200ZE	—	1213	—	1267	—	1322	ps
		MachXO2-2000ZE	—	1204	—	1250	—	1296	ps
		MachXO2-4000ZE	—	1195	—	1233	—	1269	ps
		MachXO2-7000ZE	—	1243	—	1268	—	1296	ps
Edge Clock									
f _{MAX_EDGE} ⁸	Frequency for Edge Clock	MachXO2-1200 and larger devices	—	210	—	175	—	146	MHz
Pin-LUT-Pin Propagation Delay									
t _{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	—	9.35	—	9.78	—	10.21	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t _{CO}	Clock to Output – PIO Output Register	MachXO2-256ZE	—	10.46	—	10.86	—	11.25	ns
		MachXO2-640ZE	—	10.52	—	10.92	—	11.32	ns
		MachXO2-1200ZE	—	11.24	—	11.68	—	12.12	ns
		MachXO2-2000ZE	—	11.27	—	11.71	—	12.16	ns
		MachXO2-4000ZE	—	11.28	—	11.78	—	12.28	ns
		MachXO2-7000ZE	—	11.22	—	11.76	—	12.30	ns
t _{SU}	Clock to Data Setup – PIO Input Register	MachXO2-256ZE	–0.21	—	–0.21	—	–0.21	—	ns
		MachXO2-640ZE	–0.22	—	–0.22	—	–0.22	—	ns
		MachXO2-1200ZE	–0.25	—	–0.25	—	–0.25	—	ns
		MachXO2-2000ZE	–0.27	—	–0.27	—	–0.27	—	ns
		MachXO2-4000ZE	–0.31	—	–0.31	—	–0.31	—	ns
		MachXO2-7000ZE	–0.33	—	–0.33	—	–0.33	—	ns
t _H	Clock to Data Hold – PIO Input Register	MachXO2-256ZE	3.96	—	4.25	—	4.65	—	ns
		MachXO2-640ZE	4.01	—	4.31	—	4.71	—	ns
		MachXO2-1200ZE	3.95	—	4.29	—	4.73	—	ns
		MachXO2-2000ZE	3.94	—	4.29	—	4.74	—	ns
		MachXO2-4000ZE	3.96	—	4.36	—	4.87	—	ns
		MachXO2-7000ZE	3.93	—	4.37	—	4.91	—	ns

Figure 3-9. GDDR71 Video Timing Waveforms

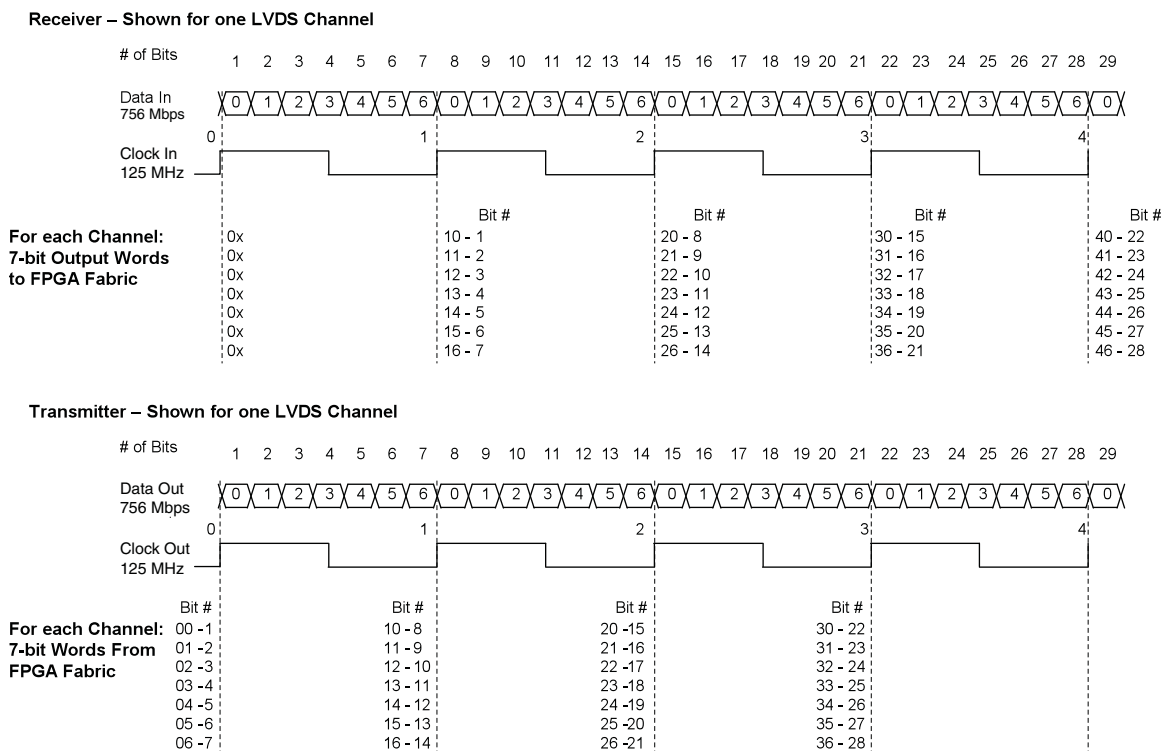


Figure 3-10. Receiver GDDR71_RX. Waveforms

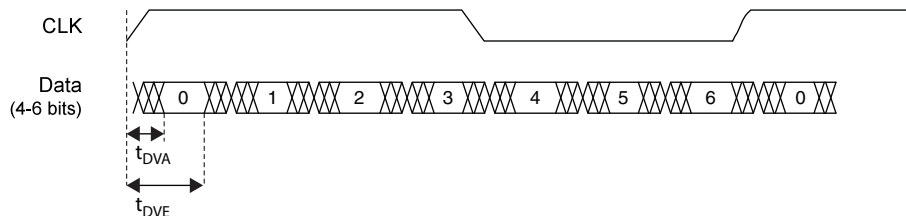
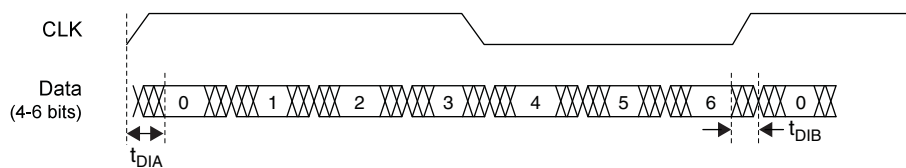


Figure 3-11. Transmitter GDDR71_TX. Waveforms



sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Modes					
t _{PRGM}	PROGRAMN low pulse accept		55	—	ns
t _{PRGMJ}	PROGRAMN low pulse rejection		—	25	ns
t _{INITL}	INITN low time	LCMXO2-256	—	30	μs
		LCMXO2-640	—	35	μs
		LCMXO2-640U/ LCMXO2-1200	—	55	μs
		LCMXO2-1200U/ LCMXO2-2000	—	70	μs
		LCMXO2-2000U/ LCMXO2-4000	—	105	μs
		LCMXO2-7000	—	130	μs
t _{DPPINIT}	PROGRAMN low to INITN low		—	150	ns
t _{DPPDONE}	PROGRAMN low to DONE low		—	150	ns
t _{IODISS}	PROGRAMN low to I/O disable		—	120	ns
Slave SPI					
f _{MAX}	CCLK clock frequency		—	66	MHz
t _{CCLKH}	CCLK clock pulse width high		7.5	—	ns
t _{CCLKL}	CCLK clock pulse width low		7.5	—	ns
t _{STSU}	CCLK setup time		2	—	ns
t _{STH}	CCLK hold time		0	—	ns
t _{STCO}	CCLK falling edge to valid output		—	10	ns
t _{STOZ}	CCLK falling edge to valid disable		—	10	ns
t _{STOV}	CCLK falling edge to valid enable		—	10	ns
t _{SCS}	Chip select high time		25	—	ns
t _{SCSS}	Chip select setup time		3	—	ns
t _{SCSH}	Chip select hold time		3	—	ns
Master SPI					
f _{MAX}	MCLK clock frequency		—	133	MHz
t _{MCLKH}	MCLK clock pulse width high		3.75	—	ns
t _{MCLKL}	MCLK clock pulse width low		3.75	—	ns
t _{STSU}	MCLK setup time		5	—	ns
t _{STH}	MCLK hold time		1	—	ns
t _{CSSPI}	INITN high to chip select low		100	200	ns
t _{MCLK}	INITN high to first MCLK edge		0.75	1	μs

For Further Information

For further information regarding logic signal connections for various packages please refer to the MachXO2 Device Pinout Files.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Users must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- [Thermal Management](#) document
- TN1198, [Power Estimation and Management for MachXO2 Devices](#)
- The Power Calculator tool is included with the Lattice design tools, or as a standalone download from www.latticesemi.com/software

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1TG100C	2112	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-2TG100C	2112	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-3TG100C	2112	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-2000ZE-1MG132C	2112	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-2MG132C	2112	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-3MG132C	2112	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-2000ZE-1TG144C	2112	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-2TG144C	2112	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-3TG144C	2112	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-2000ZE-1BG256C	2112	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-2BG256C	2112	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-3BG256C	2112	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-2000ZE-1FTG256C	2112	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-2000ZE-2FTG256C	2112	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-2000ZE-3FTG256C	2112	1.2 V	–3	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000ZE-1QN84C	4320	1.2 V	–1	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-2QN84C	4320	1.2 V	–2	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-3QN84C	4320	1.2 V	–3	Halogen-Free QFN	84	COM
LCMXO2-4000ZE-1MG132C	4320	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-2MG132C	4320	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-3MG132C	4320	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-4000ZE-1TG144C	4320	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-2TG144C	4320	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-3TG144C	4320	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-4000ZE-1BG256C	4320	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-2BG256C	4320	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-3BG256C	4320	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-4000ZE-1FTG256C	4320	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-2FTG256C	4320	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-3FTG256C	4320	1.2 V	–3	Halogen-Free ftBGA	256	COM
LCMXO2-4000ZE-1BG332C	4320	1.2 V	–1	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-2BG332C	4320	1.2 V	–2	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-3BG332C	4320	1.2 V	–3	Halogen-Free caBGA	332	COM
LCMXO2-4000ZE-1FG484C	4320	1.2 V	–1	Halogen-Free fpBGA	484	COM
LCMXO2-4000ZE-2FG484C	4320	1.2 V	–2	Halogen-Free fpBGA	484	COM
LCMXO2-4000ZE-3FG484C	4320	1.2 V	–3	Halogen-Free fpBGA	484	COM

High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256HC-4SG32C	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	COM
LCMXO2-256HC-5SG32C	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	COM
LCMXO2-256HC-6SG32C	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	COM
LCMXO2-256HC-4SG48C	256	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	COM
LCMXO2-256HC-5SG48C	256	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	COM
LCMXO2-256HC-6SG48C	256	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	COM
LCMXO2-256HC-4UMG64C	256	2.5 V / 3.3 V	–4	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-5UMG64C	256	2.5 V / 3.3 V	–5	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-6UMG64C	256	2.5 V / 3.3 V	–6	Halogen-Free ucBGA	64	COM
LCMXO2-256HC-4TG100C	256	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-256HC-5TG100C	256	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-256HC-6TG100C	256	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-256HC-4MG132C	256	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-256HC-5MG132C	256	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-256HC-6MG132C	256	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640HC-4SG48C	640	2.5 V / 3.3 V	–4	Halogen-Free QFN	48	COM
LCMXO2-640HC-5SG48C	640	2.5 V / 3.3 V	–5	Halogen-Free QFN	48	COM
LCMXO2-640HC-6SG48C	640	2.5 V / 3.3 V	–6	Halogen-Free QFN	48	COM
LCMXO2-640HC-4TG100C	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-640HC-5TG100C	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-640HC-6TG100C	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-640HC-4MG132C	640	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-640HC-5MG132C	640	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-640HC-6MG132C	640	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640UHC-4TG144C	640	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-5TG144C	640	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-640UHC-6TG144C	640	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32C	1280	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	COM
LCMXO2-1200HC-5SG32C	1280	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	COM
LCMXO2-1200HC-6SG32C	1280	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	COM
LCMXO2-1200HC-4TG100C	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-5TG100C	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-6TG100C	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-4MG132C	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-5MG132C	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-6MG132C	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-4TG144C	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-5TG144C	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-6TG144C	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256C	1280	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-1200UHC-5FTG256C	1280	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-1200UHC-6FTG256C	1280	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100C	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-5TG100C	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-6TG100C	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-2000HC-4MG132C	2112	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-5MG132C	2112	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-6MG132C	2112	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-2000HC-4TG144C	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-5TG144C	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-6TG144C	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-2000HC-4BG256C	2112	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-5BG256C	2112	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-6BG256C	2112	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-2000HC-4FTG256C	2112	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HC-5FTG256C	2112	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HC-6FTG256C	2112	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144C	6864	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-5TG144C	6864	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-6TG144C	6864	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-4BG256C	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-5BG256C	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-6BG256C	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-4FTG256C	6864	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-5FTG256C	6864	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-6FTG256C	6864	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-4BG332C	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-5BG332C	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-6BG332C	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-4FG400C	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-5FG400C	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-6FG400C	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-4FG484C	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-5FG484C	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-6FG484C	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100CR1 ¹	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-5TG100CR1 ¹	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-6TG100CR1 ¹	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-4MG132CR1 ¹	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-5MG132CR1 ¹	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-6MG132CR1 ¹	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-4TG144CR1 ¹	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-5TG144CR1 ¹	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-6TG144CR1 ¹	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200HC-speed package CR1” are the same as the “LCMXO2-1200HC-speed package C” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000ZE-1UWG49ITR ¹	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR50 ³	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1UWG49ITR1K ²	2112	1.2 V	–1	Halogen-Free WLCSP	49	IND
LCMXO2-2000ZE-1TG100I	2112	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-2TG100I	2112	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-3TG100I	2112	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-2000ZE-1MG132I	2112	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-2MG132I	2112	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-3MG132I	2112	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-2000ZE-1TG144I	2112	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-2TG144I	2112	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-3TG144I	2112	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-2000ZE-1BG256I	2112	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-2BG256I	2112	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-3BG256I	2112	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-2000ZE-1FTG256I	2112	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-2FTG256I	2112	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-2000ZE-3FTG256I	2112	1.2 V	–3	Halogen-Free ftBGA	256	IND

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.

Date	Version	Section	Change Summary
May 2014	2.5	Architecture	Updated TransFR (Transparent Field Reconfiguration) section. Updated TransFR description for PLL use during background Flash programming.
February 2014	02.4	Introduction	Included the 49 WLCSP package in the MachXO2 Family Selection Guide table.
		Architecture	Added information to Standby Mode and Power Saving Options section.
		Pinout Information	Added the XO2-2000 49 WLCSP in the Pinout Information Summary table.
		Ordering Information	Added UW49 package in MachXO2 Part Number Description.
			Added and LCMXO2-2000ZE-1UWG49CTR in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging section.
December 2013	02.3	Architecture	Added and LCMXO2-2000ZE-1UWG49ITR in Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section.
			Updated information on CLKOS output divider in sysCLOCK Phase Locked Loops (PLLs) section.
		DC and Switching Characteristics	Updated Static Supply Current – ZE Devices table.
			Updated footnote 4 in sysIO Single-Ended DC Electrical Characteristics table; Updated V_{IL} Max. (V) data for LVCMOS 25 and LVCMOS 28.
September 2013	02.2	Architecture	Updated V_{OS} test condition in sysIO Differential Electrical Characteristics - LVDS table.
			Removed I ² C Clock-Stretching feature per PCN #10A-13.
			Removed information on PDPR memory in RAM Mode section.
		DC and Switching Characteristics	Updated Supported Input Standards table.
June 2013	02.1	Architecture	Updated Power-On-Reset Voltage Levels table.
			Architecture Overview – Added information on the state of the register on power up and after configuration.
		DC and Switching Characteristics	sysCLOCK Phase Locked Loops (PLLs) section – Added missing cross reference to sysCLOCK PLL Timing table.
			Added slew rate information to footnote 2 of the MachXO2 External Switching Characteristics – HC/HE Devices and the MachXO2 External Switching Characteristics – ZE Devices tables.
			Power-On-Reset Voltage Levels table – Added symbols.

Date	Version	Section	Change Summary
May 2011	01.3	Multiple	Replaced “SED” with “SRAM CRC Error Detection” throughout the document.
		DC and Switching Characteristics	Added footnote 1 to Program Erase Specifications table.
		Pinout Information	Updated Pin Information Summary tables.
			Signal name SO/SISPISO changed to SO/SPISO in the Signal Descriptions table.
April 2011	01.2	—	Data sheet status changed from Advance to Preliminary.
		Introduction	Updated MachXO2 Family Selection Guide table.
		Architecture	Updated Supported Input Standards table.
			Updated sysMEM Memory Primitives diagram.
			Added differential SSTL and HSTL IO standards.
		DC and Switching Characteristics	Updates following parameters: POR voltage levels, DC electrical characteristics, static supply current for ZE/HE/HC devices, static power consumption contribution of different components – ZE devices, programming and erase Flash supply current.
			Added VREF specifications to sysIO recommended operating conditions.
			Updating timing information based on characterization.
			Added differential SSTL and HSTL IO standards.
		Ordering Information	Added Ordering Part Numbers for R1 devices, and devices in WLCSP packages.
			Added R1 device specifications.
January 2011	01.1	All	Included ultra-high I/O devices.
		DC and Switching Characteristics	Recommended Operating Conditions table – Added footnote 3.
			DC Electrical Characteristics table – Updated data for I_{IL} , I_{IH} , V_{HYST} typical values updated.
			Generic DDRX2 Outputs with Clock and Data Aligned at Pin (GDDR2_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and T_{DIB} .
			Generic DDRX4 Outputs with Clock and Data Aligned at Pin (GDDR4_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and T_{DIB} .
			Power-On-Reset Voltage Levels table - clarified note 3.
			Clarified VCCIO related recommended operating conditions specifications.
			Added power supply ramp rate requirements.
			Added Power Supply Ramp Rates table.
			Updated Programming/Erase Specifications table.
			Removed references to V_{CCP} .
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Removed references to V_{CCP} .
November 2010	01.0	—	Initial release.