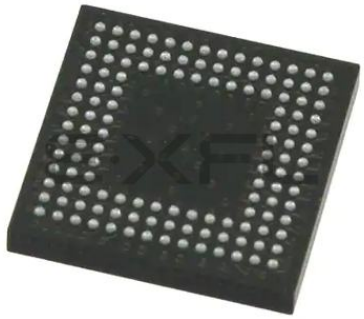
Lattice Semiconductor Corporation - LCMXO2-1200ZE-1MG132CR1 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

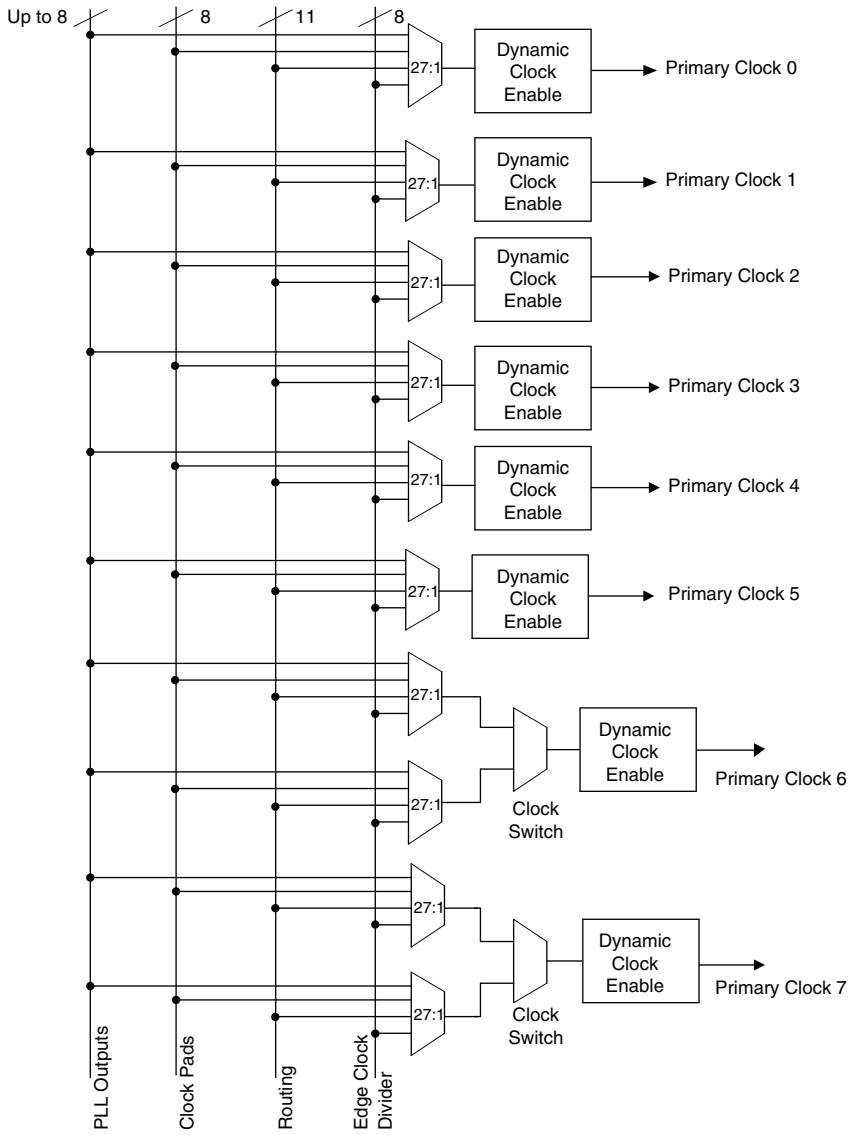
Details	
Product Status	Obsolete
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	104
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	132-LFBGA, CSPBGA
Supplier Device Package	132-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-1200ze-1mg132cr1

Table 1-1. MachXO2™ Family Selection Guide

		XO2-256	XO2-640	XO2-640U[1]	XO2-1200	XO2-1200U[1]	XO2-2000	XO2-2000U[1]	XO2-4000	XO2-7000
LUTs		256	640	640	1280	1280	2112	2112	4320	6864
Distributed RAM (kbits)		2	5	5	10	10	16	16	34	54
EBR SRAM (kbits)		0	18	64	64	74	74	92	92	240
Number of EBR SRAM Blocks (9 kbits/block)		0	2	7	7	8	8	10	10	26
UFM (kbits)		0	24	64	64	80	80	96	96	256
Device Options:	HC[2]	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	HE[3]						Yes	Yes	Yes	Yes
	ZE[4]	Yes	Yes		Yes		Yes		Yes	Yes
Number of PLLs		0	0	1	1	1	1	2	2	2
Hardened Functions:	I2C	2	2	2	2	2	2	2	2	2
	SPI	1	1	1	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1	1	1	1
Packages						**IO**				
25-ball WLCSP[5] (2.5 mm x 2.5 mm, 0.4 mm)					18					
32 QFN[6] (5 mm x 5 mm, 0.5 mm)		21			21					
48 QFN[8, 9] (7 mm x 7 mm, 0.5 mm)		40	40							
49-ball WLCSP[5] (3.2 mm x 3.2 mm, 0.4 mm)							38			
64-ball ucBGA (4 mm x 4 mm, 0.4 mm)		44								
84 QFN[7] (7 mm x 7 mm, 0.5 mm)									68	
100-pin TQFP (14 mm x 14 mm)		55	78		79		79			
132-ball csBGA (8 mm x 8 mm, 0.5 mm)		55	79		104		104		104	
144-pin TQFP (20 mm x 20 mm)				107	107		111		114	114
184-ball csBGA[7] (8 mm x 8 mm, 0.5 mm)									150	
256-ball caBGA (14 mm x 14 mm, 0.8 mm)							206		206	206
256-ball ftBGA (17 mm x 17 mm, 1.0 mm)						206	206		206	206
332-ball caBGA (17 mm x 17 mm, 0.8 mm)									274	278
484-ball ftBGA (23 mm x 23 mm, 1.0 mm)								278	278	334

1. Ultra high I/O device.
2. High performance with regulator – VCC = 2.5 V, 3.3 V
3. High performance without regulator – V_{CC} = 1.2 V
4. Low power without regulator – V_{CC} = 1.2 V
5. WLCSP package only available for ZE devices.
6. 32 QFN package only available for HC and ZE devices.
7. 184 csBGA package only available for HE devices.
8. 48-pin QFN information is ‘Advanced’.
9. 48 QFN package only available for HC devices.

Figure 2-5. Primary Clocks for MachXO2 Devices



Primary clocks for MachXO2-640U, MachXO2-1200/U and larger devices.

Note: MachXO2-640 and smaller devices do not have inputs from the Edge Clock Divider or PLL and fewer routing inputs. These devices have 17:1 muxes instead of 27:1 muxes.

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO2 External Switching Characteristics table.

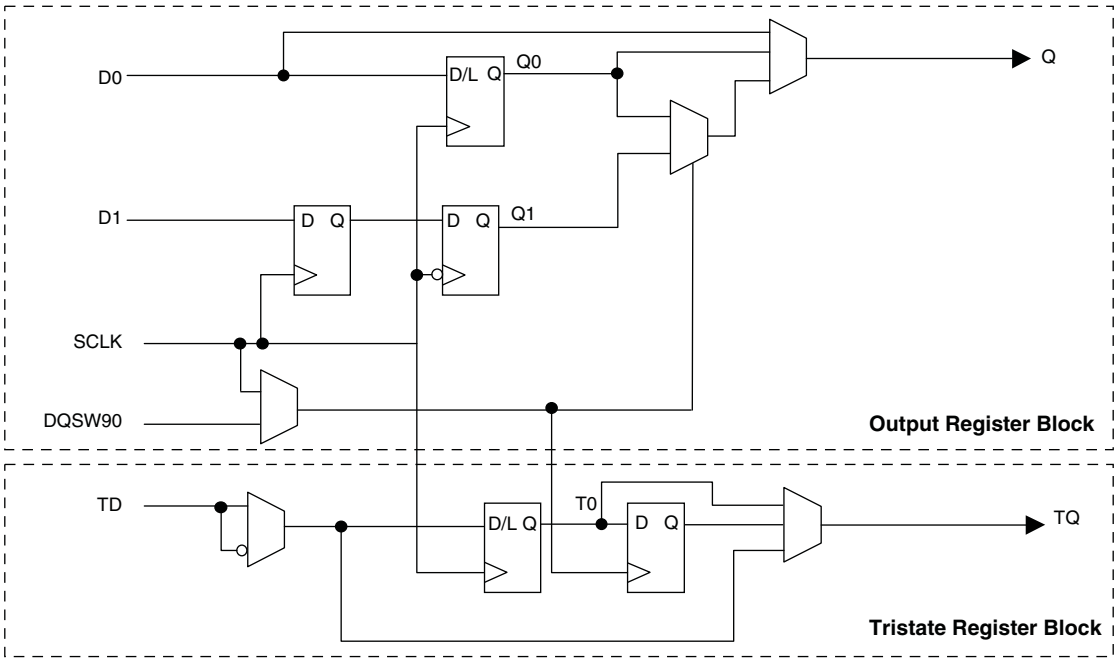
Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO2 devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO2 devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

The MachXO2-640U, MachXO2-1200/U and higher density devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these higher density devices have on-chip differential termination and also provide PCI support.

Figure 2-15. MachXO2 Output Register Block Diagram (PIO on the Right Edges)



Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

The tri-state register blocks on the right edge contain an additional register for DDR memory operation. In DDR memory mode, the register TS input is fed into another register that is clocked using the DQSW90 signal. The output of this register is used as a tri-state control.

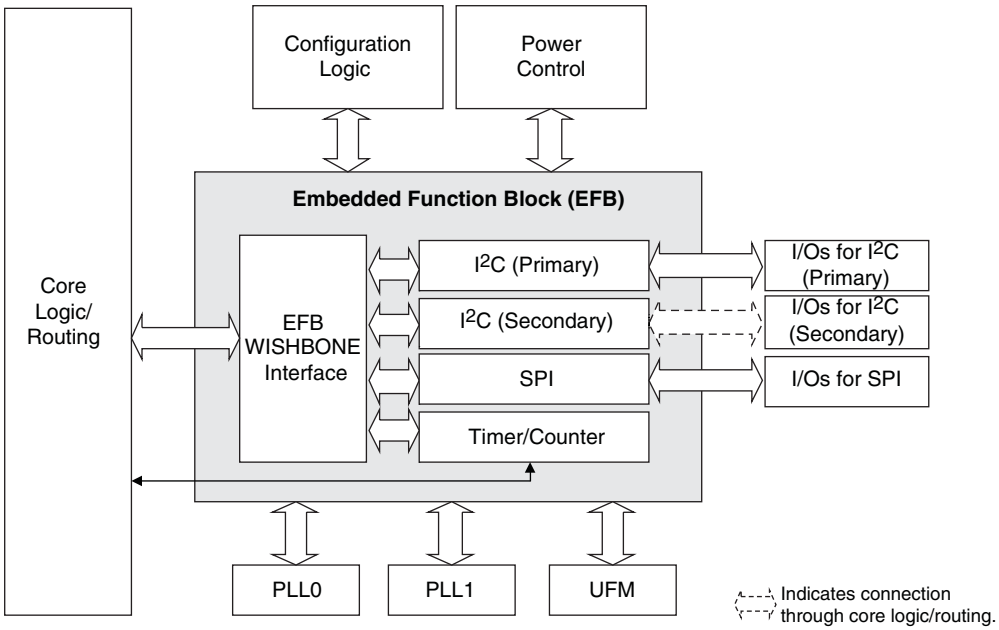
Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

Table 2-9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3

Figure 2-20. Embedded Function Block Interface



Hardened I²C IP Core

Every MachXO2 device contains two I²C IP cores. These are the primary and secondary I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I²C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface

Figure 2-21. I²C Core Block Diagram

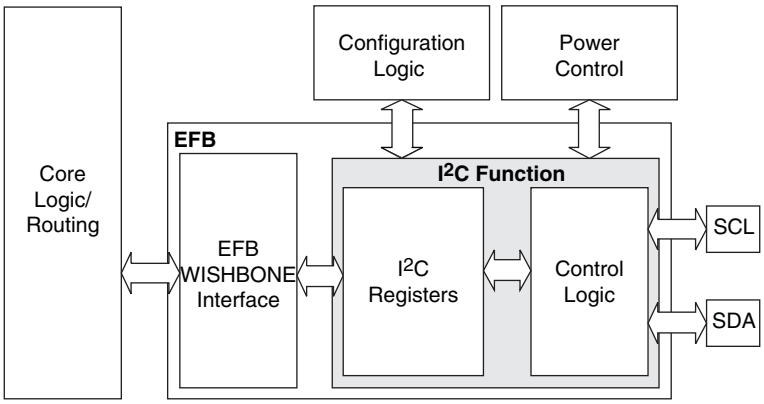


Table 2-15 describes the signals interfacing with the I²C cores.

Table 2-15. I²C Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I²C core. The signal is an output if the I²C core is in master mode. The signal is an input if the I²C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device.
i2c_sda	Bi-directional	Bi-directional data line of the I²C core. The signal is an output when data is transmitted from the I²C core. The signal is an input when data is received into the I²C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device.
i2c_irqo	Output	Interrupt request output signal of the I²C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I²C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab.

Hardened SPI IP Core

Every MachXO2 device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO2 devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface

Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I^2C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO2 device:

1. Internal Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I^2C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1204, MachXO2 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1204, MachXO2 Programming and Configuration Usage Guide.

TransFR (Transparent Field Reconfiguration)
TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

Static Supply Current – ZE Devices[1, 2, 3, 6]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO2-256ZE	18	µA
		LCMXO2-640ZE	28	µA
		LCMXO2-1200ZE	56	µA
		LCMXO2-2000ZE	80	µA
		LCMXO2-4000ZE	124	µA
		LCMXO2-7000ZE	189	µA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	1	µA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off. To estimate the impact of turning each of these items on, please refer to the following table or for more detail with your specific design use the Power Calculator tool.
3. Frequency = 0 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Static Power Consumption Contribution of Different Components – ZE Devices

The table below can be used for approximating static power consumption. For a more accurate power analysis for your design please use the Power Calculator tool.

Symbol	Parameter	Typ.	Units
I_{DCBG}	Bandgap DC power contribution	101	µA
I_{DCPOR}	POR DC power contribution	38	µA
$I_{DCIOBANKCONTROLLER}$	DC power contribution per I/O bank controller	143	µA

Static Supply Current – HC/HE Devices[1, 2, 3, 6]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO2-256HC	1.15	mA
		LCMXO2-640HC	1.84	mA
		LCMXO2-640UHC	3.48	mA
		LCMXO2-1200HC	3.49	mA
		LCMXO2-1200UHC	4.80	mA
		LCMXO2-2000HC	4.80	mA
		LCMXO2-2000UHC	8.44	mA
		LCMXO2-4000HC	8.45	mA
		LCMXO2-7000HC	12.87	mA
		LCMXO2-2000HE	1.39	mA
		LCMXO2-4000HE	2.55	mA
		LCMXO2-7000HE	4.06	mA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.
3. Frequency = 0 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

Programming and Erase Flash Supply Current – HC/HE Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO2-256HC	14.6	mA
		LCMXO2-640HC	16.1	mA
		LCMXO2-640UHC	18.8	mA
		LCMXO2-1200HC	18.8	mA
		LCMXO2-1200UHC	22.1	mA
		LCMXO2-2000HC	22.1	mA
		LCMXO2-2000UHC	26.8	mA
		LCMXO2-4000HC	26.8	mA
		LCMXO2-7000HC	33.2	mA
		LCMXO2-2000HE	18.3	mA
		LCMXO2-2000UHE	20.4	mA
		LCMXO2-4000HE	20.4	mA
		LCMXO2-7000HE	23.9	mA
I_{CCIO}	Bank Power Supply[6]	All devices	0	mA

1. For further information on supply current, please refer to TN1198, Power Estimation and Management for MachXO2 Devices.
2. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. T_J = 25 °C, power supplies at nominal voltage.
6. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.6	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.6	—	—	—
PCI[3]	3.135	3.3	3.6	—	—	—
SSTL25	2.375	2.5	2.625	1.15	1.25	1.35
SSTL18	1.71	1.8	1.89	0.833	0.9	0.969
HSTL18	1.71	1.8	1.89	0.816	0.9	1.08
LVCMOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVCMOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVCMOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVCMOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVCMOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVCMOS12R33[4]	3.135	3.3	3.6	0.45	0.6	0.75
LVCMOS12R25[4]	2.375	2.5	2.625	0.45	0.6	0.75
LVCMOS10R33[4]	3.135	3.3	3.6	0.35	0.5	0.65
LVCMOS10R25[4]	2.375	2.5	2.625	0.35	0.5	0.65
LVDS25[1, 2]	2.375	2.5	2.625	—	—	—
LVDS33[1, 2]	3.135	3.3	3.6	—	—	—
LVPECL[1]	3.135	3.3	3.6	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—
RSDS[1]	2.375	2.5	2.625	—	—	—
SSTL18D	1.71	1.8	1.89	—	—	—
SSTL25D	2.375	2.5	2.625	—	—	—
HSTL18D	1.71	1.8	1.89	—	—	—

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.
3. Input on the bottom bank of the MachXO2-640U, MachXO2-1200/U and larger devices only.
4. Supported only for inputs and BIDIs for all ZE devices, and –6 speed grade for HE and HC devices.

Parameter	Description	Device	–6		–5		–4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.369	—	0.395	—	0.421	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.529	—	0.530	—	0.527	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM LPDDR Serial Data Speed		—	280	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	140	—	125	—	104	MHz
f_{LPDDR}	LPDDR Data Transfer Rate		0	280	0	250	0	208	Mbps
DDR[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.350	—	0.387	—	0.414	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.545	—	0.538	—	0.532	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	150	—	125	—	104	MHz
f_{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps
DDR2[9, 12]									
t_{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only.[13]	—	0.360	—	0.378	—	0.406	UI
t_{DVEDQ}	Input Data Hold After DQS Input		0.555	—	0.549	—	0.542	—	UI
t_{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f_{DATA}	MEM DDR Serial Data Speed		—	300	—	250	—	208	Mbps
f_{SCLK}	SCLK Frequency		—	150	—	125	—	104	MHz
f_{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	300	N/A	250	N/A	208	Mbps

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\ ns)/2$.
7. The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 105 ps (–6), 113 ps (–5), 120 ps (–4).
8. This number for general purpose usage. Duty cycle tolerance is +/– 10%.
9. Duty cycle is +/–5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. High-speed DDR and LVDS not supported in SG32 (32 QFN) packages.
12. Advance information for MachXO2 devices in 48 QFN packages.
13. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

MachXO2 External Switching Characteristics – ZE Devices[1, 2, 3, 4, 5, 6, 7]

Over Recommended Operating Conditions

Parameter	Description	Device	–3		–2		–1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f_{MAX_PRI}[8]	Frequency for Primary Clock Tree	All MachXO2 devices	—	150	—	125	—	104	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO2 devices	1.00	—	1.20	—	1.40	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO2-256ZE	—	1250	—	1272	—	1296	ps
		MachXO2-640ZE	—	1161	—	1183	—	1206	ps
		MachXO2-1200ZE	—	1213	—	1267	—	1322	ps
		MachXO2-2000ZE	—	1204	—	1250	—	1296	ps
		MachXO2-4000ZE	—	1195	—	1233	—	1269	ps
		MachXO2-7000ZE	—	1243	—	1268	—	1296	ps
Edge Clock									
f_{MAX_EDGE}[8]	Frequency for Edge Clock	MachXO2-1200 and larger devices	—	210	—	175	—	146	MHz
Pin-LUT-Pin Propagation Delay									
t_{PD}	Best case propagation delay through one LUT-4	All MachXO2 devices	—	9.35	—	9.78	—	10.21	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t_{CO}	Clock to Output – PIO Output Register	MachXO2-256ZE	—	10.46	—	10.86	—	11.25	ns
		MachXO2-640ZE	—	10.52	—	10.92	—	11.32	ns
		MachXO2-1200ZE	—	11.24	—	11.68	—	12.12	ns
		MachXO2-2000ZE	—	11.27	—	11.71	—	12.16	ns
		MachXO2-4000ZE	—	11.28	—	11.78	—	12.28	ns
		MachXO2-7000ZE	—	11.22	—	11.76	—	12.30	ns
t_{SU}	Clock to Data Setup – PIO Input Register	MachXO2-256ZE	–0.21	—	–0.21	—	–0.21	—	ns
		MachXO2-640ZE	–0.22	—	–0.22	—	–0.22	—	ns
		MachXO2-1200ZE	–0.25	—	–0.25	—	–0.25	—	ns
		MachXO2-2000ZE	–0.27	—	–0.27	—	–0.27	—	ns
		MachXO2-4000ZE	–0.31	—	–0.31	—	–0.31	—	ns
		MachXO2-7000ZE	–0.33	—	–0.33	—	–0.33	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	MachXO2-256ZE	3.96	—	4.25	—	4.65	—	ns
		MachXO2-640ZE	4.01	—	4.31	—	4.71	—	ns
		MachXO2-1200ZE	3.95	—	4.29	—	4.73	—	ns
		MachXO2-2000ZE	3.94	—	4.29	—	4.74	—	ns
		MachXO2-4000ZE	3.96	—	4.36	—	4.87	—	ns
		MachXO2-7000ZE	3.93	—	4.37	—	4.91	—	ns

Figure 3-5. Receiver RX.CLK.Aligned and MEM DDR Input Waveforms

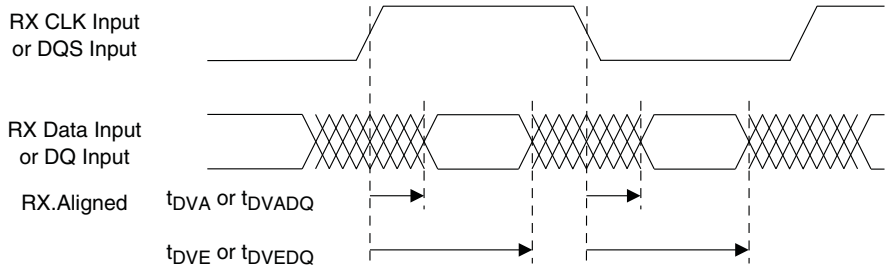


Figure 3-6. Receiver RX.CLK.Centered Waveforms

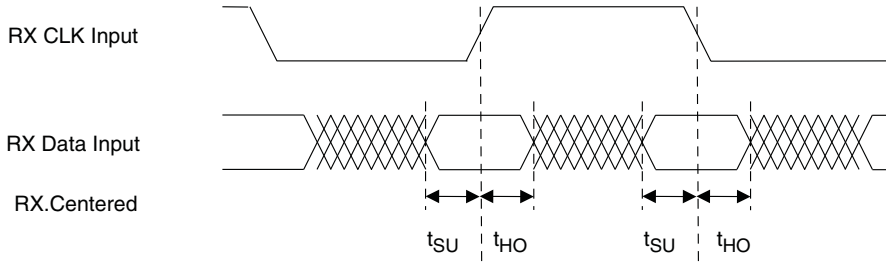


Figure 3-7. Transmitter TX.CLK.Aligned Waveforms

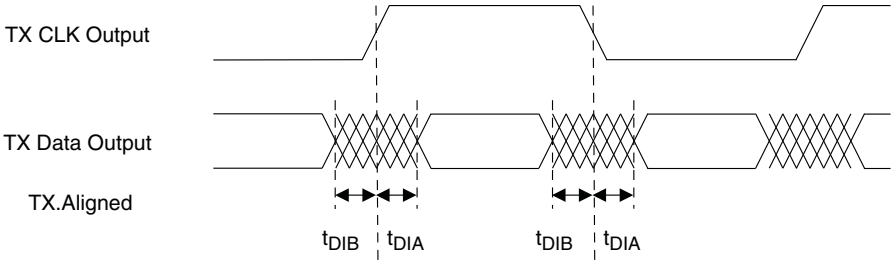
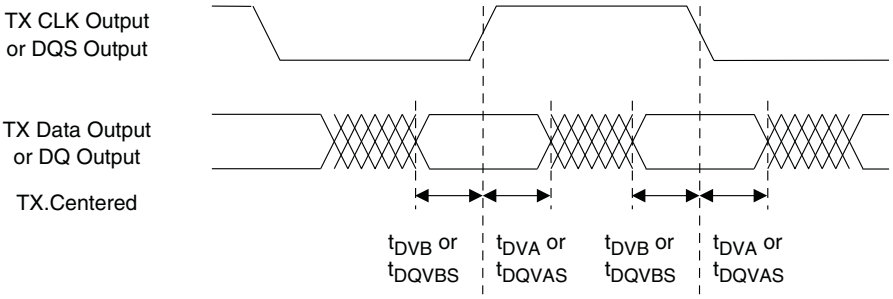


Figure 3-8. Transmitter TX.CLK.Centered and MEM DDR Output Waveforms



I²C Port Timing Specifications[1, 2]

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCL clock frequency	—	400	kHz

1. MachXO2 supports the following modes:
   • Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)
   • Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)
2. Refer to the I²C specification for timing requirements.

SPI Port Timing Specifications[1]

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCK clock frequency	—	45	MHz

1. Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

Switching Test Conditions

Figure 3-13 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-5.

Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards

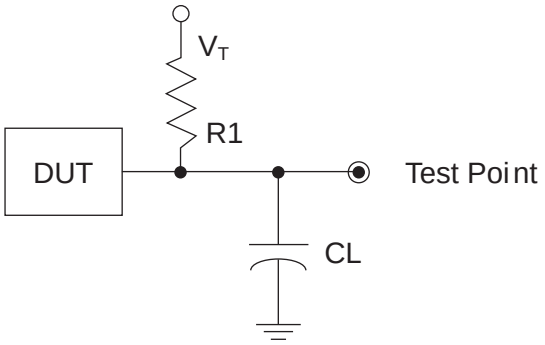


Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R1	CL	Timing Ref.	VT
LVTTL and LVCMOS settings (L -> H, H -> L)	∞	0pF	LVTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVTTL and LVCMOS 3.3 (Z -> H)	188	0pF	1.5 V	V_{OL}
LVTTL and LVCMOS 3.3 (Z -> L)			1.5 V	V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVTTL + LVCMOS (H -> Z)			V_{OH} – 0.15 V	V_{OL}
LVTTL + LVCMOS (L -> Z)			V_{OL} – 0.15 V	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

	MachXO2-2000						MachXO2-2000U
	49 WLCSP	100 TQFP	132 csBGA	144 TQFP	256 caBGA	256 ftBGA	484 ftBGA
General Purpose I/O per Bank							
Bank 0	19	18	25	27	50	50	70
Bank 1	0	21	26	28	52	52	68
Bank 2	13	20	28	28	52	52	72
Bank 3	0	6	7	8	16	16	24
Bank 4	0	6	8	10	16	16	16
Bank 5	6	8	10	10	20	20	28
Total General Purpose Single-Ended I/O	38	79	104	111	206	206	278
Differential I/O per Bank							
Bank 0	7	9	13	14	25	25	35
Bank 1	0	10	13	14	26	26	34
Bank 2	6	10	14	14	26	26	36
Bank 3	0	3	3	4	8	8	12
Bank 4	0	3	4	5	8	8	8
Bank 5	3	4	5	5	10	10	14
Total General Purpose Differential I/O	16	39	52	56	103	103	139
Dual Function I/O	24	31	33	33	33	33	37
High-speed Differential I/O							
Bank 0	5	4	8	9	14	14	18
Gearboxes							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	4	8	9	14	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	10	14	14	14	14	18
DQS Groups							
Bank 1	0	1	2	2	2	2	2
VCCIO Pins							
Bank 0	2	2	3	3	4	4	10
Bank 1	0	2	3	3	4	4	10
Bank 2	1	2	3	3	4	4	10
Bank 3	0	1	1	1	1	1	3
Bank 4	0	1	1	1	2	2	4
Bank 5	1	1	1	1	1	1	3
VCC	2	2	4	4	8	8	12
GND	4	8	10	12	24	24	48
NC	0	1	1	4	1	1	105
Reserved for Configuration	1	1	1	1	v	1	1
Total Count of Bonded Pins	39	100	132	144	256	256	484

For Further Information

For further information regarding logic signal connections for various packages please refer to the MachXO2 Device Pinout Files.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Users must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1198, Power Estimation and Management for MachXO2 Devices
- The Power Calculator tool is included with the Lattice design tools, or as a standalone download from www.latticesemi.com/software

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000ZE-1QN84I	4320	1.2 V	–1	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-2QN84I	4320	1.2 V	–2	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-3QN84I	4320	1.2 V	–3	Halogen-Free QFN	84	IND
LCMXO2-4000ZE-1MG132I	4320	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-2MG132I	4320	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-3MG132I	4320	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-4000ZE-1TG144I	4320	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-2TG144I	4320	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-3TG144I	4320	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-4000ZE-1BG256I	4320	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-2BG256I	4320	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-3BG256I	4320	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-4000ZE-1FTG256I	4320	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-2FTG256I	4320	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-3FTG256I	4320	1.2 V	–3	Halogen-Free ftBGA	256	IND
LCMXO2-4000ZE-1BG332I	4320	1.2 V	–1	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-2BG332I	4320	1.2 V	–2	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-3BG332I	4320	1.2 V	–3	Halogen-Free caBGA	332	IND
LCMXO2-4000ZE-1FG484I	4320	1.2 V	–1	Halogen-Free fpBGA	484	IND
LCMXO2-4000ZE-2FG484I	4320	1.2 V	–2	Halogen-Free fpBGA	484	IND
LCMXO2-4000ZE-3FG484I	4320	1.2 V	–3	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144I	6864	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-2TG144I	6864	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-3TG144I	6864	1.2 V	–3	Halogen-Free TQFP	144	IND
LCMXO2-7000ZE-1BG256I	6864	1.2 V	–1	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-2BG256I	6864	1.2 V	–2	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-3BG256I	6864	1.2 V	–3	Halogen-Free caBGA	256	IND
LCMXO2-7000ZE-1FTG256I	6864	1.2 V	–1	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-2FTG256I	6864	1.2 V	–2	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-3FTG256I	6864	1.2 V	–3	Halogen-Free ftBGA	256	IND
LCMXO2-7000ZE-1BG332I	6864	1.2 V	–1	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-2BG332I	6864	1.2 V	–2	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-3BG332I	6864	1.2 V	–3	Halogen-Free caBGA	332	IND
LCMXO2-7000ZE-1FG484I	6864	1.2 V	–1	Halogen-Free fpBGA	484	IND
LCMXO2-7000ZE-2FG484I	6864	1.2 V	–2	Halogen-Free fpBGA	484	IND
LCMXO2-7000ZE-3FG484I	6864	1.2 V	–3	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4SG32I	1280	2.5 V / 3.3 V	–4	Halogen-Free QFN	32	IND
LCMXO2-1200HC-5SG32I	1280	2.5 V / 3.3 V	–5	Halogen-Free QFN	32	IND
LCMXO2-1200HC-6SG32I	1280	2.5 V / 3.3 V	–6	Halogen-Free QFN	32	IND
LCMXO2-1200HC-4TG100I	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-5TG100I	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-6TG100I	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-1200HC-4MG132I	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-5MG132I	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-6MG132I	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-1200HC-4TG144I	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-5TG144I	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-1200HC-6TG144I	1280	2.5 V/ 3.3 V	–6	Halogen-Free TQFP	144	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200UHC-4FTG256I	1280	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-5FTG256I	1280	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-1200UHC-6FTG256I	1280	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HC-4TG100I	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-5TG100I	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-6TG100I	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	IND
LCMXO2-2000HC-4MG132I	2112	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-5MG132I	2112	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-6MG132I	2112	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-2000HC-4TG144I	2112	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-5TG144I	2112	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-6TG144I	2112	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-2000HC-4BG256I	2112	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-5BG256I	2112	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-6BG256I	2112	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-2000HC-4FTG256I	2112	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-5FTG256I	2112	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-2000HC-6FTG256I	2112	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHC-4FG484I	2112	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-5FG484I	2112	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-2000UHC-6FG484I	2112	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND

MachXO2 Family Data Sheet Supplemental Information

For Further Information

A variety of technical notes for the MachXO2 family are available on the Lattice web site.

- TN1198, Power Estimation and Management for MachXO2 Devices
- TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide
- TN1201, Memory Usage Guide for MachXO2 Devices
- TN1202, MachXO2 sysIO Usage Guide
- TN1203, Implementing High-Speed Interfaces with MachXO2 Devices
- TN1204, MachXO2 Programming and Configuration Usage Guide
- TN1205, Using User Flash Memory and Hardened Control Functions in MachXO2 Devices
- TN1206, MachXO2 SRAM CRC Error Detection Usage Guide
- TN1207, Using TraceID in MachXO2 Devices
- TN1074, PCB Layout Recommendations for BGA Packages
- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology
- AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices
- AN8066, Boundary Scan Testability with Lattice sysIO Capability
- MachXO2 Device Pinout Files
- Thermal Management document
- Lattice design tools

For further information on interface standards, refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, LVDS, DDR, DDR2, LPDDR): www.jedec.org
- PCI: www.pcisig.com

Date	Version	Section	Change Summary
February 2012	01.7	All	Updated document with new corporate logo.
	01.6	—	Data sheet status changed from preliminary to final.
		Introduction	MachXO2 Family Selection Guide table – Removed references to 49-ball WLCSP.
		DC and Switching Characteristics	Updated Flash Download Time table.
			Modified Storage Temperature in the Absolute Maximum Ratings section.
			Updated I_{DK} max in Hot Socket Specifications table.
			Modified Static Supply Current tables for ZE and HC/HE devices.
			Updated Power Supply Ramp Rates table.
			Updated Programming and Erase Supply Current tables.
			Updated data in the External Switching Characteristics table.
			Corrected Absolute Maximum Ratings for Dedicated Input Voltage Applied for LCMXO2 HC.
			DC Electrical Characteristics table – Minor corrections to conditions for I_{IL}, I_{IH}.
		Pinout Information	Removed references to 49-ball WLCSP.
			Signal Descriptions table – Updated description for GND, VCC, and VCCIOx.
			Updated Pin Information Summary table – Number of VCCIOs, GNDs, VCCs, and Total Count of Bonded Pins for MachXO2-256, 640, and 640U and Dual Function I/O for MachXO2-4000 332caBGA.
		Ordering Information	Removed references to 49-ball WLCSP
August 2011	01.5	DC and Switching Characteristics	Updated ESD information.
		Ordering Information	Updated footnote for ordering WLCSP devices.
	01.4	Architecture	Updated information in Clock/Control Distribution Network and sysCLOCK Phase Locked Loops (PLLs).
		DC and Switching Characteristics	Updated I_{IL} and I_{IH} conditions in the DC Electrical Characteristics table.
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Updated Pin Information Summary table: Dual Function I/O, DQS Groups Bank 1, Total General Purpose Single-Ended I/O, Differential I/O Per Bank, Total Count of Bonded Pins, Gearboxes. Added column of data for MachXO2-2000 49 WLCSP.
		Ordering Information	Updated R1 Device Specifications text section with information on migration from MachXO2-1200-R1 to Standard (non-R1) devices.
			Corrected Supply Voltage typo for part numbers: LCMX02-2000UHE-4FG484I, LCMX02-2000UHE-5FG484I, LCMX02-2000UHE-6FG484I.
			Added footnote for WLCSP package parts.
		Supplemental Information	Removed reference to Stand-alone Power Calculator for MachXO2 Devices. Added reference to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices.