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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

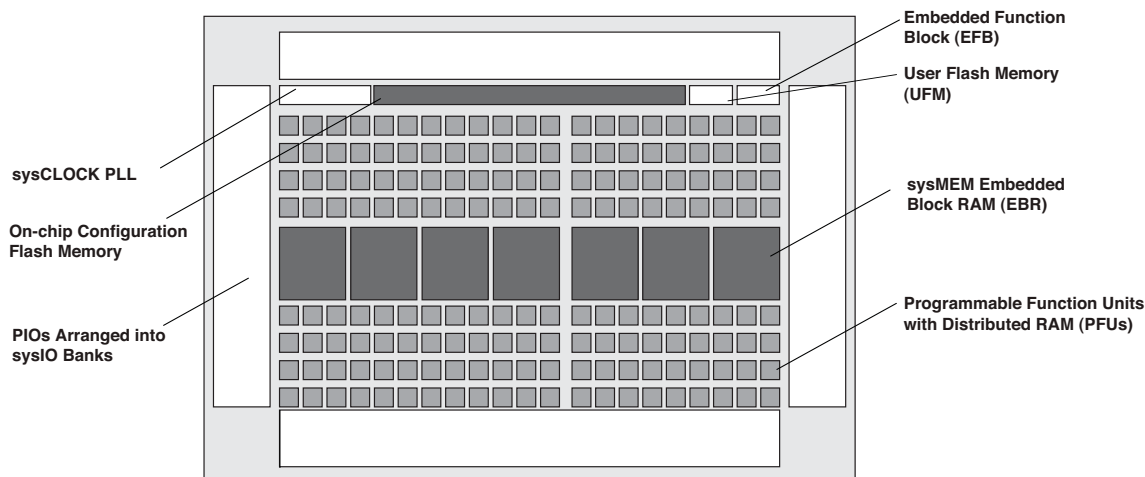
Details

Product Status	Obsolete
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	107
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-1200ze-1tg144ir1

Architecture Overview

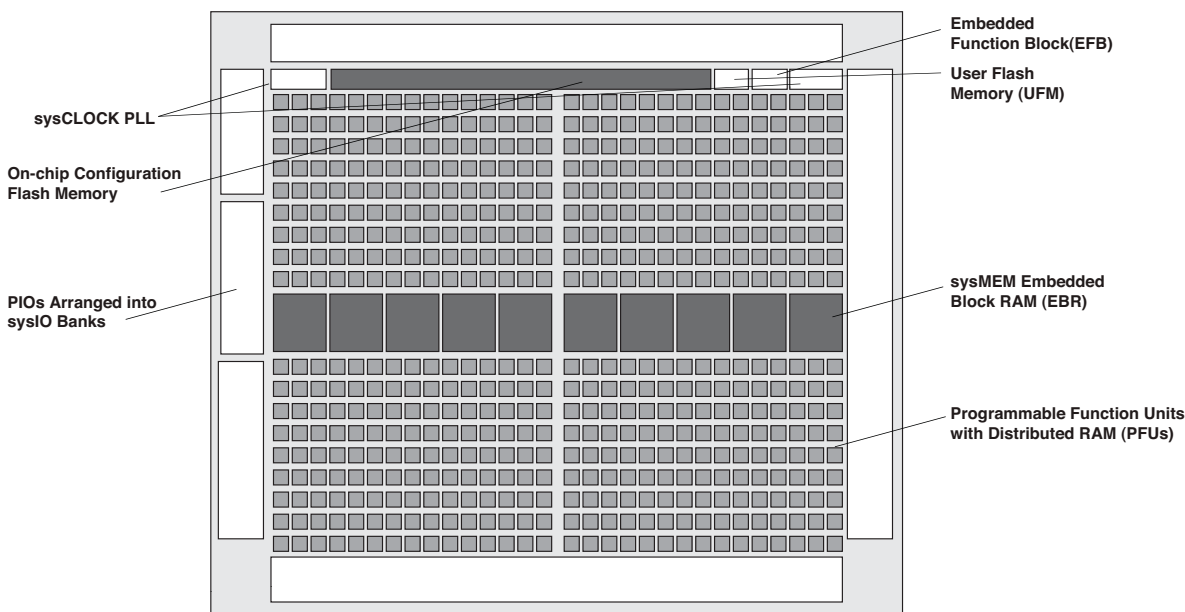
The MachXO2 family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have sysCLOCK™ PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.

Figure 2-1. Top View of the MachXO2-1200 Device



Note: MachXO2-256, and MachXO2-640/U are similar to MachXO2-1200. MachXO2-256 has a lower LUT count and no PLL or EBR blocks. MachXO2-640 has no PLL, a lower LUT count and two EBR blocks. MachXO2-640U has a lower LUT count, one PLL and seven EBR blocks.

Figure 2-2. Top View of the MachXO2-4000 Device



Note: MachXO2-1200U, MachXO2-2000/U and MachXO2-7000 are similar to MachXO2-4000. MachXO2-1200U and MachXO2-2000 have a lower LUT count, one PLL, and eight EBR blocks. MachXO2-2000U has a lower LUT count, two PLLs, and 10 EBR blocks. MachXO2-7000 has a higher LUT count, two PLLs, and 26 EBR blocks.

ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1201, [Memory Usage Guide for MachXO2 Devices](#).

Routing

There are many resources provided in the MachXO2 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

Each MachXO2 device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

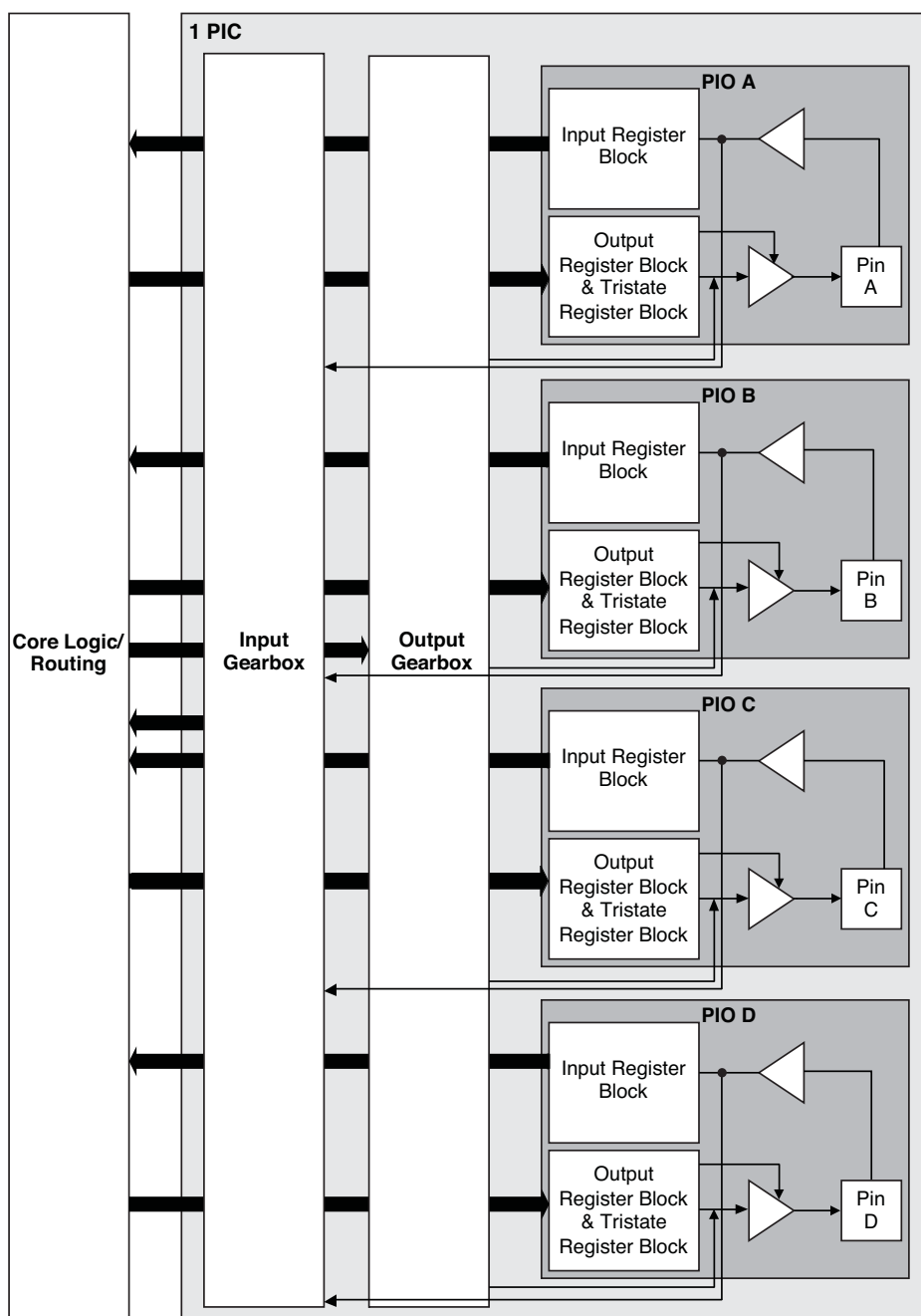
The MachXO2 architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO2-640U, MachXO2-1200/U and higher density devices have two edge clocks each on the top and bottom edges. Lower density devices have no edge clocks. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO2 devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO2 External Switching Characteristics table.

The primary clock signals for the MachXO2-256 and MachXO2-640 are generated from eight 17:1 muxes. The available clock sources include eight I/O sources and 9 routing inputs. Primary clock signals for the MachXO2-640U, MachXO2-1200/U and larger devices are generated from eight 27:1 muxes. The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.

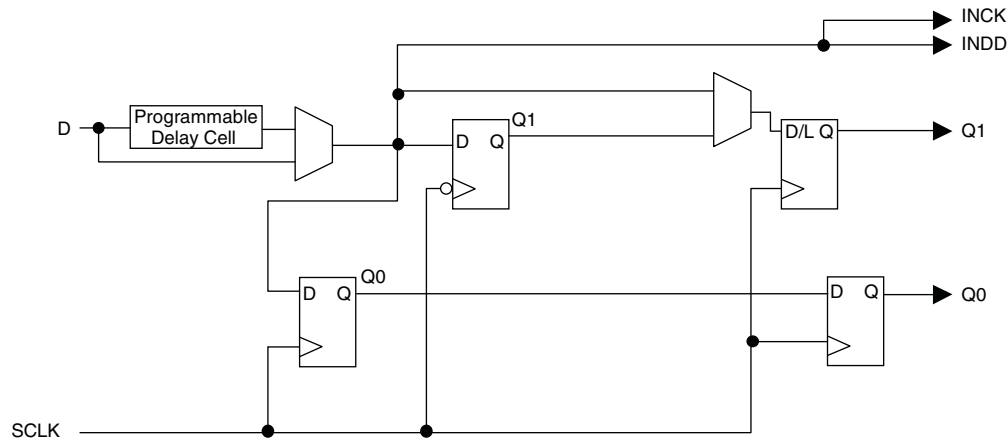
Figure 2-11. Group of Four Programmable I/O Cells



Notes:

1. Input gearbox is available only in PIC on the bottom edge of MachXO2-640U, MachXO2-1200/U and larger devices.
2. Output gearbox is available only in PIC on the top edge of MachXO2-640U, MachXO2-1200/U and larger devices.

Figure 2-12. MachXO2 Input Register Block Diagram (PIO on Left, Top and Bottom Edges)



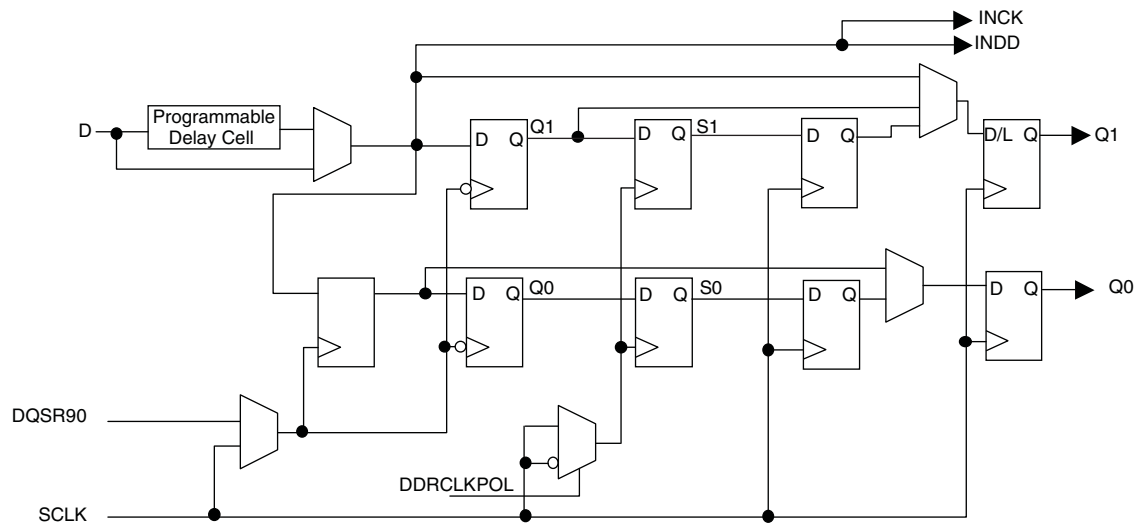
Right Edge

The input register block on the right edge is a superset of the same block on the top, bottom, and left edges. In addition to the modes described above, the input register block on the right edge also supports DDR memory mode.

In DDR memory mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (DQSR90) in the DDR Memory mode creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

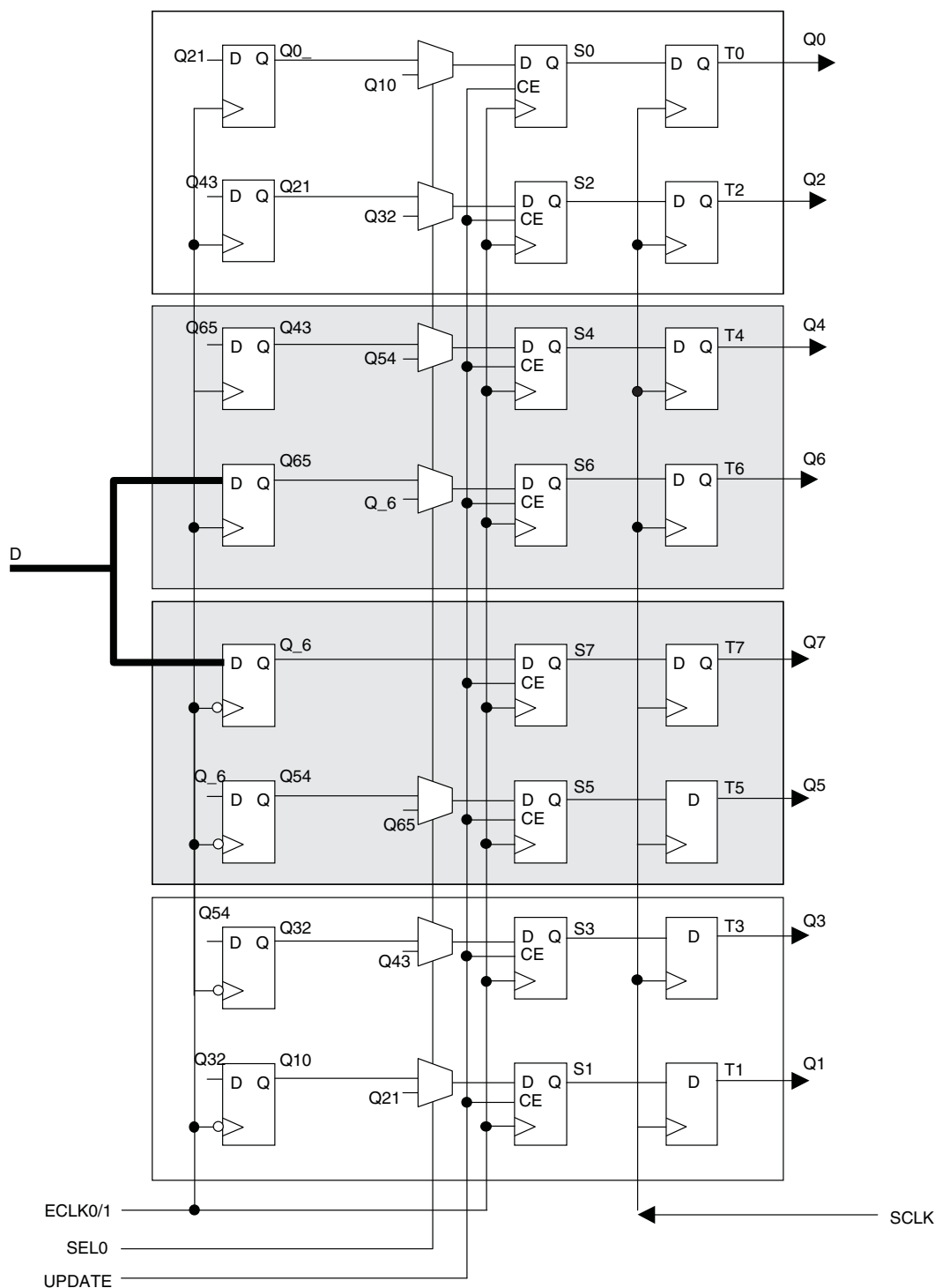
The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the DQS domain. The DQSR90 and DDRCLKPOL signals are generated in the DQS read-write block.

Figure 2-13. MachXO2 Input Register Block Diagram (PIO on Right Edge)



These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2-16 shows a block diagram of the input gearbox.

Figure 2-16. Input Gearbox



More information on the input gearbox is available in TN1203, [Implementing High-Speed Interfaces with MachXO2 Devices](#).

Output Gearbox

Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDR4 (8:1) gearbox or as two ODDR2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

Table 2-10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]		
GDDR4(8:1): D[7:0]		
GDDR2(4:1)(IOL-A): D[3:0]		
GDDR2(4:1)(IOL-C): D[7:4]		
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-17 shows the output gearbox block diagram.

Figure 2-21. I²C Core Block Diagram

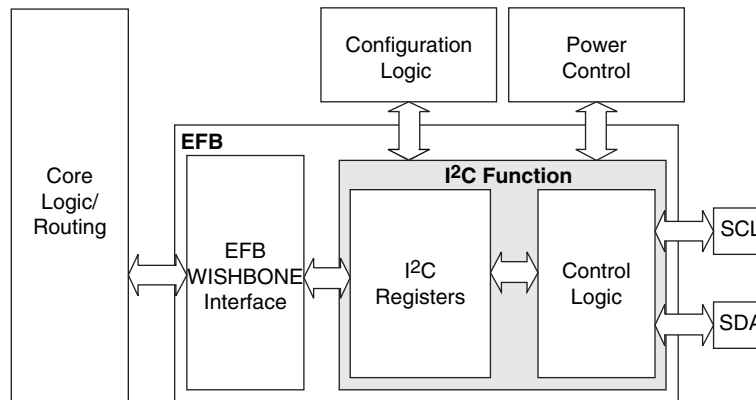


Table 2-15 describes the signals interfacing with the I²C cores.

Table 2-15. I²C Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I ² C core. The signal is an output if the I ² C core is in master mode. The signal is an input if the I ² C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I ² C ports in each MachXO2 device.
i2c_sda	Bi-directional	Bi-directional data line of the I ² C core. The signal is an output when data is transmitted from the I ² C core. The signal is an input when data is received into the I ² C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I ² C ports in each MachXO2 device.
i2c_irqo	Output	Interrupt request output signal of the I ² C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I ² C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I ² C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I ² C Tab.

Hardened SPI IP Core

Every MachXO2 device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO2 devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface

sysIO Single-Ended DC Electrical Characteristics^{1, 2}

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max. ⁴ (mA)	I_{OH} Max. ⁴ (mA)
	Min. (V) ³	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3 LVTTL	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
							8	-8
							12	-12
							16	-16
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
							8	-8
							12	-12
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
					0.2	$V_{CCIO} - 0.2$	8	-8
							12	-12
LVCMOS 1.2	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	4	-2
							8	-6
							0.1	-0.1
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5
SSTL25 Class I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCIO} - 0.62$	8	8
SSTL25 Class II	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	NA	NA	NA	NA
SSTL18 Class I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	0.40	$V_{CCIO} - 0.40$	8	8
SSTL18 Class II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	NA	NA	NA	NA
HSTL18 Class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.40	$V_{CCIO} - 0.40$	8	8
HSTL18 Class II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS25R33	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS18R33	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS18R25	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS15R33	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS15R25	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	NA	NA	NA	NA
LVCMOS12R33	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS12R25	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain
LVCMOS10R33	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain

Parameter	Description	Device	-6		-5		-4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{HPLL}	Clock to Data Hold – PIO Input Register	MachXO2-1200HC-HE	0.41	—	0.48	—	0.55	—	ns
		MachXO2-2000HC-HE	0.42	—	0.49	—	0.56	—	ns
		MachXO2-4000HC-HE	0.43	—	0.50	—	0.58	—	ns
		MachXO2-7000HC-HE	0.46	—	0.54	—	0.62	—	ns
t _{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200HC-HE	2.88	—	3.19	—	3.72	—	ns
		MachXO2-2000HC-HE	2.87	—	3.18	—	3.70	—	ns
		MachXO2-4000HC-HE	2.96	—	3.28	—	3.81	—	ns
		MachXO2-7000HC-HE	3.05	—	3.35	—	3.87	—	ns
t _{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-2000HC-HE	–0.83	—	–0.83	—	–0.83	—	ns
		MachXO2-4000HC-HE	–0.87	—	–0.87	—	–0.87	—	ns
		MachXO2-7000HC-HE	–0.91	—	–0.91	—	–0.91	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Aligned ^{9, 12}									
t _{DVA}	Input Data Valid After CLK	All MachXO2 devices, all sides	—	0.317	—	0.344	—	0.368	UI
t _{DVE}	Input Data Hold After CLK		0.742	—	0.702	—	0.668	—	UI
f _{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Centered ^{9, 12}									
t _{SU}	Input Data Setup Before CLK	All MachXO2 devices, all sides	0.566	—	0.560	—	0.538	—	ns
t _{HO}	Input Data Hold After CLK		0.778	—	0.879	—	1.090	—	ns
f _{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	208	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	104	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Aligned ^{9, 12}									
t _{DVA}	Input Data Valid After CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only ¹¹	—	0.316	—	0.342	—	0.364	UI
t _{DVE}	Input Data Hold After CLK		0.710	—	0.675	—	0.679	—	UI
f _{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Centered ^{9, 12}									
t _{SU}	Input Data Setup Before CLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only ¹¹	0.233	—	0.219	—	0.198	—	ns
t _{HO}	Input Data Hold After CLK		0.287	—	0.287	—	0.344	—	ns
f _{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	462	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	231	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz

Parameter	Description	Device	-3		-2		-1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-256ZE	2.62	—	2.91	—	3.14	—	ns
		MachXO2-640ZE	2.56	—	2.85	—	3.08	—	ns
		MachXO2-1200ZE	2.30	—	2.57	—	2.79	—	ns
		MachXO2-2000ZE	2.25	—	2.50	—	2.70	—	ns
		MachXO2-4000ZE	2.39	—	2.60	—	2.76	—	ns
		MachXO2-7000ZE	2.17	—	2.33	—	2.43	—	ns
t _{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-256ZE	–0.44	—	–0.44	—	–0.44	—	ns
		MachXO2-640ZE	–0.43	—	–0.43	—	–0.43	—	ns
		MachXO2-1200ZE	–0.28	—	–0.28	—	–0.28	—	ns
		MachXO2-2000ZE	–0.31	—	–0.31	—	–0.31	—	ns
		MachXO2-4000ZE	–0.34	—	–0.34	—	–0.34	—	ns
		MachXO2-7000ZE	–0.21	—	–0.21	—	–0.21	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices	—	150	—	125	—	104	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)									
t _{COE}	Clock to Output – PIO Output Register	MachXO2-1200ZE	—	11.10	—	11.51	—	11.91	ns
		MachXO2-2000ZE	—	11.10	—	11.51	—	11.91	ns
		MachXO2-4000ZE	—	10.89	—	11.28	—	11.67	ns
		MachXO2-7000ZE	—	11.10	—	11.51	—	11.91	ns
t _{SUE}	Clock to Data Setup – PIO Input Register	MachXO2-1200ZE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-2000ZE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000ZE	–0.15	—	–0.15	—	–0.15	—	ns
		MachXO2-7000ZE	–0.23	—	–0.23	—	–0.23	—	ns
t _{HE}	Clock to Data Hold – PIO Input Register	MachXO2-1200ZE	3.81	—	4.11	—	4.52	—	ns
		MachXO2-2000ZE	3.81	—	4.11	—	4.52	—	ns
		MachXO2-4000ZE	3.60	—	3.89	—	4.28	—	ns
		MachXO2-7000ZE	3.81	—	4.11	—	4.52	—	ns
t _{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200ZE	2.78	—	3.11	—	3.40	—	ns
		MachXO2-2000ZE	2.78	—	3.11	—	3.40	—	ns
		MachXO2-4000ZE	3.11	—	3.48	—	3.79	—	ns
		MachXO2-7000ZE	2.94	—	3.30	—	3.60	—	ns
t _{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200ZE	–0.29	—	–0.29	—	–0.29	—	ns
		MachXO2-2000ZE	–0.29	—	–0.29	—	–0.29	—	ns
		MachXO2-4000ZE	–0.46	—	–0.46	—	–0.46	—	ns
		MachXO2-7000ZE	–0.37	—	–0.37	—	–0.37	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)									
t _{COPLL}	Clock to Output – PIO Output Register	MachXO2-1200ZE	—	7.95	—	8.07	—	8.19	ns
		MachXO2-2000ZE	—	7.97	—	8.10	—	8.22	ns
		MachXO2-4000ZE	—	7.98	—	8.10	—	8.23	ns
		MachXO2-7000ZE	—	8.02	—	8.14	—	8.26	ns
t _{SUPLL}	Clock to Data Setup – PIO Input Register	MachXO2-1200ZE	0.85	—	0.85	—	0.89	—	ns
		MachXO2-2000ZE	0.84	—	0.84	—	0.86	—	ns
		MachXO2-4000ZE	0.84	—	0.84	—	0.85	—	ns
		MachXO2-7000ZE	0.83	—	0.83	—	0.81	—	ns

Parameter	Description	Device	-3		-2		-1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LPDDR ^{9, 12}									
t _{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. ¹³	—	0.349	—	0.381	—	0.396	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.630	—	0.613	—	UI
t _{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f _{DATA}	MEM LPDDR Serial Data Speed		—	120	—	110	—	96	Mbps
f _{SCLK}	SCLK Frequency		—	60	—	55	—	48	MHz
f _{LPDDR}	LPDDR Data Transfer Rate		0	120	0	110	0	96	Mbps
DDR ^{9, 12}									
t _{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. ¹³	—	0.347	—	0.374	—	0.393	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.665	—	0.637	—	0.616	—	UI
t _{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f _{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f _{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f _{MEM_DDR}	MEM DDR Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps
DDR2 ^{9, 12}									
t _{DVADQ}	Input Data Valid After DQS Input	MachXO2-1200/U and larger devices, right side only. ¹³	—	0.372	—	0.394	—	0.410	UI
t _{DVEDQ}	Input Data Hold After DQS Input		0.690	—	0.658	—	0.618	—	UI
t _{DQVBS}	Output Data Invalid Before DQS Output		0.25	—	0.25	—	0.25	—	UI
t _{DQVAS}	Output Data Invalid After DQS Output		0.25	—	0.25	—	0.25	—	UI
f _{DATA}	MEM DDR Serial Data Speed		—	140	—	116	—	98	Mbps
f _{SCLK}	SCLK Frequency		—	70	—	58	—	49	MHz
f _{MEM_DDR2}	MEM DDR2 Data Transfer Rate		N/A	140	N/A	116	N/A	98	Mbps

- Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
- General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pF load, fast slew rate.
- Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
- DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
- 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
- For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$.
- The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 167 ps (–3), 182 ps (–2), 195 ps (–1).
- This number for general purpose usage. Duty cycle tolerance is +/-10%.
- Duty cycle is +/- 5% for system usage.
- The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
- High-speed DDR and LVDS not supported in SG32 (32-Pin QFN) packages.
- Advance information for MachXO2 devices in 48 QFN packages.
- DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

	MachXO2-2000						MachXO2-2000U
	49 WLCSP	100 TQFP	132 csBGA	144 TQFP	256 caBGA	256 ftBGA	484 ftBGA
General Purpose I/O per Bank							
Bank 0	19	18	25	27	50	50	70
Bank 1	0	21	26	28	52	52	68
Bank 2	13	20	28	28	52	52	72
Bank 3	0	6	7	8	16	16	24
Bank 4	0	6	8	10	16	16	16
Bank 5	6	8	10	10	20	20	28
Total General Purpose Single-Ended I/O	38	79	104	111	206	206	278
Differential I/O per Bank							
Bank 0	7	9	13	14	25	25	35
Bank 1	0	10	13	14	26	26	34
Bank 2	6	10	14	14	26	26	36
Bank 3	0	3	3	4	8	8	12
Bank 4	0	3	4	5	8	8	8
Bank 5	3	4	5	5	10	10	14
Total General Purpose Differential I/O	16	39	52	56	103	103	139
Dual Function I/O							
	24	31	33	33	33	33	37
High-speed Differential I/O							
Bank 0	5	4	8	9	14	14	18
Gearboxes							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	4	8	9	14	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	10	14	14	14	14	18
DQS Groups							
Bank 1	0	1	2	2	2	2	2
VCCIO Pins							
Bank 0	2	2	3	3	4	4	10
Bank 1	0	2	3	3	4	4	10
Bank 2	1	2	3	3	4	4	10
Bank 3	0	1	1	1	1	1	3
Bank 4	0	1	1	1	2	2	4
Bank 5	1	1	1	1	1	1	3
VCC	2	2	4	4	8	8	12
GND	4	8	10	12	24	24	48
NC	0	1	1	4	1	1	105
Reserved for Configuration	1	1	1	1	v	1	1
Total Count of Bonded Pins	39	100	132	144	256	256	484



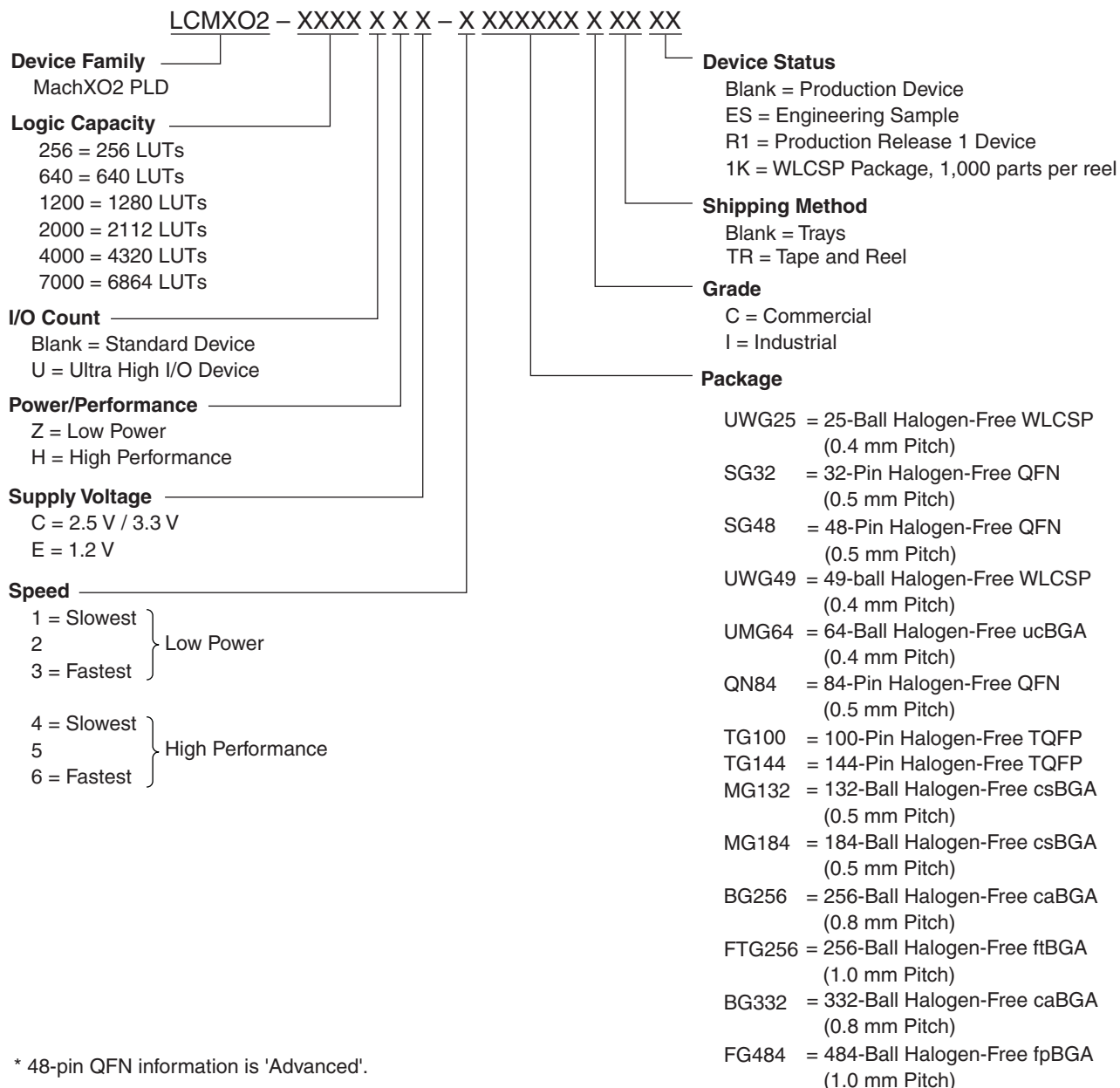
MachXO2 Family Data Sheet

Ordering Information

March 2017

Data Sheet DS1035

MachXO2 Part Number Description



Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-256ZE-1SG32C	256	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-256ZE-2SG32C	256	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-256ZE-3SG32C	256	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-256ZE-1UMG64C	256	1.2 V	–1	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-2UMG64C	256	1.2 V	–2	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-3UMG64C	256	1.2 V	–3	Halogen-Free ucBGA	64	COM
LCMXO2-256ZE-1TG100C	256	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-2TG100C	256	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-3TG100C	256	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-256ZE-1MG132C	256	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-2MG132C	256	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-256ZE-3MG132C	256	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-640ZE-1TG100C	640	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-2TG100C	640	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-3TG100C	640	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-640ZE-1MG132C	640	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-2MG132C	640	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-640ZE-3MG132C	640	1.2 V	–3	Halogen-Free csBGA	132	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1SG32C	1280	1.2 V	–1	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-2SG32C	1280	1.2 V	–2	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-3SG32C	1280	1.2 V	–3	Halogen-Free QFN	32	COM
LCMXO2-1200ZE-1TG100C	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100C	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100C	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132C	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132C	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132C	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144C	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144C	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144C	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000ZE-1TG144C	6864	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-2TG144C	6864	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-3TG144C	6864	1.2 V	–3	Halogen-Free TQFP	144	COM
LCMXO2-7000ZE-1BG256C	6864	1.2 V	–1	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-2BG256C	6864	1.2 V	–2	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-3BG256C	6864	1.2 V	–3	Halogen-Free caBGA	256	COM
LCMXO2-7000ZE-1FTG256C	6864	1.2 V	–1	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-2FTG256C	6864	1.2 V	–2	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-3FTG256C	6864	1.2 V	–3	Halogen-Free ftBGA	256	COM
LCMXO2-7000ZE-1BG332C	6864	1.2 V	–1	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-2BG332C	6864	1.2 V	–2	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-3BG332C	6864	1.2 V	–3	Halogen-Free caBGA	332	COM
LCMXO2-7000ZE-1FG484C	6864	1.2 V	–1	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-2FG484C	6864	1.2 V	–2	Halogen-Free fpBGA	484	COM
LCMXO2-7000ZE-3FG484C	6864	1.2 V	–3	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100CR1 ¹	1280	1.2 V	–1	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-2TG100CR1 ¹	1280	1.2 V	–2	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-3TG100CR1 ¹	1280	1.2 V	–3	Halogen-Free TQFP	100	COM
LCMXO2-1200ZE-1MG132CR1 ¹	1280	1.2 V	–1	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-2MG132CR1 ¹	1280	1.2 V	–2	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-3MG132CR1 ¹	1280	1.2 V	–3	Halogen-Free csBGA	132	COM
LCMXO2-1200ZE-1TG144CR1 ¹	1280	1.2 V	–1	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-2TG144CR1 ¹	1280	1.2 V	–2	Halogen-Free TQFP	144	COM
LCMXO2-1200ZE-3TG144CR1 ¹	1280	1.2 V	–3	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200ZE-speed package CR1” are the same as the “LCMXO2-1200ZE-speed package C” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-6BG332C	4320	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-4FG484C	4320	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-5FG484C	4320	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-4000HE-6FG484C	4320	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144C	6864	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-5TG144C	6864	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-6TG144C	6864	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-7000HE-4BG256C	6864	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-5BG256C	6864	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-6BG256C	6864	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-7000HE-4FTG256C	6864	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-5FTG256C	6864	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-6FTG256C	6864	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HE-4BG332C	6864	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-5BG332C	6864	1.2 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-6BG332C	6864	1.2 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-7000HE-4FG484C	6864	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-5FG484C	6864	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HE-6FG484C	6864	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200ZE-1TG100IR1 ¹	1280	1.2 V	–1	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-2TG100IR1 ¹	1280	1.2 V	–2	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-3TG100IR1 ¹	1280	1.2 V	–3	Halogen-Free TQFP	100	IND
LCMXO2-1200ZE-1MG132IR1 ¹	1280	1.2 V	–1	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-2MG132IR1 ¹	1280	1.2 V	–2	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-3MG132IR1 ¹	1280	1.2 V	–3	Halogen-Free csBGA	132	IND
LCMXO2-1200ZE-1TG144IR1 ¹	1280	1.2 V	–1	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-2TG144IR1 ¹	1280	1.2 V	–2	Halogen-Free TQFP	144	IND
LCMXO2-1200ZE-3TG144IR1 ¹	1280	1.2 V	–3	Halogen-Free TQFP	144	IND

1. Specifications for the “LCMXO2-1200ZE-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HC-4QN84I	4320	2.5 V / 3.3 V	–4	Halogen-Free QFN	84	IND
LCMXO2-4000HC-5QN84I	4320	2.5 V / 3.3 V	–5	Halogen-Free QFN	84	IND
LCMXO2-4000HC-6QN84I	4320	2.5 V / 3.3 V	–6	Halogen-Free QFN	84	IND
LCMXO2-4000HC-4TG144I	4320	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-5TG144I	4320	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-6TG144I	4320	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-4000HC-4MG132I	4320	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-5MG132I	4320	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-6MG132I	4320	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-4000HC-4BG256I	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-5BG256I	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-6BG256I	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-4000HC-4FTG256I	4320	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-5FTG256I	4320	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-6FTG256I	4320	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HC-4BG332I	4320	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-5BG332I	4320	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-6BG332I	4320	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-4000HC-4FG484I	4320	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-5FG484I	4320	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HC-6FG484I	4320	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144I	6864	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-5TG144I	6864	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-6TG144I	6864	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-7000HC-4BG256I	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-5BG256I	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-6BG256I	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-7000HC-4FTG256I	6864	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-5FTG256I	6864	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-6FTG256I	6864	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HC-4BG332I	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-5BG332I	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-6BG332I	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-7000HC-4FG400I	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-5FG400I	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-6FG400I	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	400	IND
LCMXO2-7000HC-4FG484I	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-5FG484I	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HC-6FG484I	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	IND

MachXO2 Family Data Sheet

Revision History

March 2017

Data Sheet DS1035

Date	Version	Section	Change Summary
March 2017	3.3	DC and Switching Characteristics	Updated the Absolute Maximum Ratings section. Added standards.
			Updated the sysIO Recommended Operating Conditions section. Added standards.
			Updated the sysIO Single-Ended DC Electrical Characteristics section. Added standards.
			Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA} . The parameter descriptions were also modified.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the D_{VB} and the D_{VA} parameters were changed to D_{IB} and D_{IA} . The parameter descriptions were also modified.
			Updated the sysCONFIG Port Timing Specifications section. Corrected the t_{INITL} units from ns to μ s.
	Pinout Information	Pinout Information	Updated the Signal Descriptions section. Revised the descriptions of the PROGRAMN, INITN, and DONE signals.
			Updated the Pinout Information Summary section. Added footnote to MachXO2-1200 32 QFN.
	Ordering Information	Ordering Information	Updated the MachXO2 Part Number Description section. Corrected the MG184, BG256, FTG256 package information. Added “(0.8 mm Pitch)” to BG332.
			Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. — Updated LCMXO2-1200ZE-1UWG25ITR50 footnote. — Corrected footnote numbering typo. — Added the LCMXO2-2000ZE-1UWG49ITR50 and LCMXO2-2000ZE-1UWG49ITR1K part numbers. Updated/added footnote/s.

Date	Version	Section	Change Summary
May 2016	3.2	All	Moved designation for 84 QFN package information from 'Advanced' to 'Final'.
		Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 'Advanced' 48 QFN package. — Revised footnote 6. — Added footnote 9.
		DC and Switching Characteristics	Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Added footnote 12.
			Updated the MachXO2 External Switching Characteristics – ZE Devices section. Added footnote 12.
		Pinout Information	Updated the Signal Descriptions section. Added information on GND signal.
			Updated the Pinout Information Summary section. — Added 'Advanced' MachXO2-256 48 QFN values. — Added 'Advanced' MachXO2-640 48 QFN values. — Added footnote to GND. — Added footnotes 2 and 3.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added 'Advanced' SG48 package and revised footnote.
			Updated the Ordering Information section. — Added part numbers for 'Advanced' QFN 48 package.
March 2016	3.1	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Added 32 QFN value for XO2-1200. — Added 84 QFN (7 mm x 7 mm, 0.5 mm) package. — Modified package name to 100-pin TQFP. — Modified package name to 144-pin TQFP. — Added footnote.
		Architecture	Updated the Typical I/O Behavior During Power-up section. Removed reference to TN1202.
		DC and Switching Characteristics	Updated the sysCONFIG Port Timing Specifications section. Revised $t_{DPPDONE}$ and $t_{DPPINIT}$ Max. values per PCN 03A-16, released March 2016.
		Pinout Information	Updated the Pinout Information Summary section. — Added MachXO2-1200 32 QFN values. — Added 'Advanced' MachXO2-4000 84 QFN values.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added 'Advanced' QN84 package and footnote.
			Updated the Ordering Information section. — Added part numbers for 1280 LUTs QFN 32 package. — Added part numbers for 4320 LUTs QFN 84 package.
March 2015	3.0	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Changed 64-ball ucBGA dimension.
		Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.