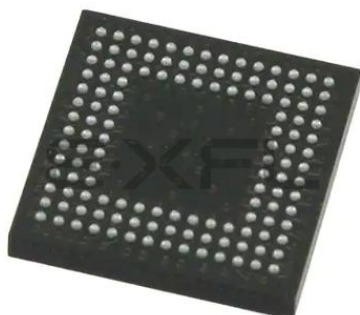




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

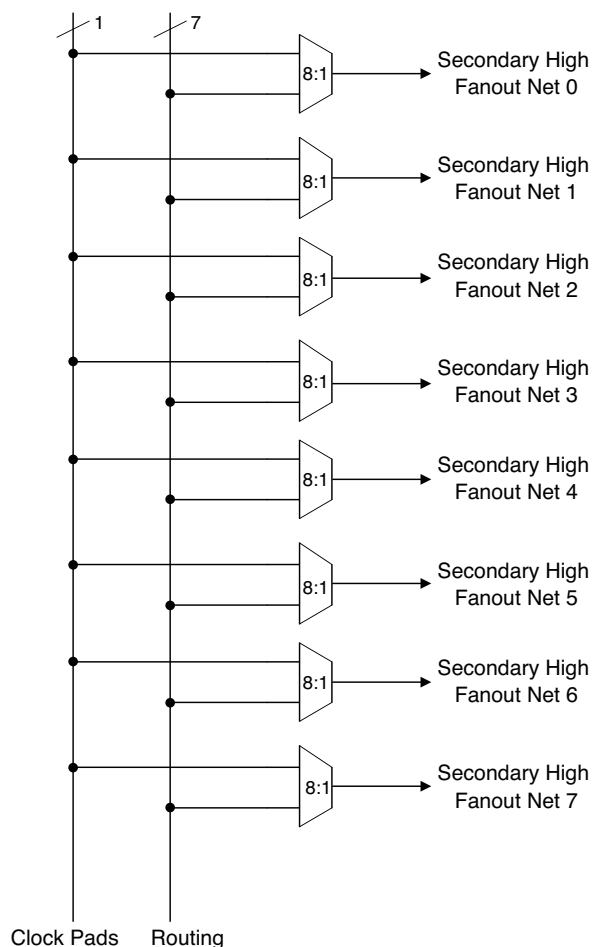
Product Status	Obsolete
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	104
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	132-LFBGA, CSPBGA
Supplier Device Package	132-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo2-1200ze-2mg132cr1

Table 1-1. MachXO2™ Family Selection Guide

		XO2-256	XO2-640	XO2-640U ¹	XO2-1200	XO2-1200U ¹	XO2-2000	XO2-2000U ¹	XO2-4000	XO2-7000
LUTs		256	640	640	1280	1280	2112	2112	4320	6864
Distributed RAM (kbits)		2	5	5	10	10	16	16	34	54
EBR SRAM (kbits)		0	18	64	64	74	74	92	92	240
Number of EBR SRAM Blocks (9 kbits/block)		0	2	7	7	8	8	10	10	26
UFM (kbits)		0	24	64	64	80	80	96	96	256
Device Options:	HC ²	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	HE ³						Yes	Yes	Yes	Yes
	ZE ⁴	Yes	Yes		Yes		Yes		Yes	Yes
Number of PLLs		0	0	1	1	1	1	2	2	2
Hardened Functions:	I2C	2	2	2	2	2	2	2	2	2
	SPI	1	1	1	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1	1	1	1
Packages		IO								
25-ball WLCSP ⁵ (2.5 mm x 2.5 mm, 0.4 mm)					18					
32 QFN ⁶ (5 mm x 5 mm, 0.5 mm)		21			21					
48 QFN ^{8,9} (7 mm x 7 mm, 0.5 mm)		40	40							
49-ball WLCSP ⁵ (3.2 mm x 3.2 mm, 0.4 mm)							38			
64-ball ucBGA (4 mm x 4 mm, 0.4 mm)		44								
84 QFN ⁷ (7 mm x 7 mm, 0.5 mm)									68	
100-pin TQFP (14 mm x 14 mm)		55	78		79		79			
132-ball csBGA (8 mm x 8 mm, 0.5 mm)		55	79		104		104		104	
144-pin TQFP (20 mm x 20 mm)				107	107		111		114	114
184-ball csBGA ⁷ (8 mm x 8 mm, 0.5 mm)									150	
256-ball caBGA (14 mm x 14 mm, 0.8 mm)							206		206	206
256-ball ftBGA (17 mm x 17 mm, 1.0 mm)						206	206		206	206
332-ball caBGA (17 mm x 17 mm, 0.8 mm)									274	278
484-ball ftBGA (23 mm x 23 mm, 1.0 mm)								278	278	334

1. Ultra high I/O device.
2. High performance with regulator – VCC = 2.5 V, 3.3 V
3. High performance without regulator – V_{CC} = 1.2 V
4. Low power without regulator – V_{CC} = 1.2 V
5. WLCSP package only available for ZE devices.
6. 32 QFN package only available for HC and ZE devices.
7. 184 csBGA package only available for HE devices.
8. 48-pin QFN information is 'Advanced'.
9. 48 QFN package only available for HC devices.

Figure 2-6. Secondary High Fanout Nets for MachXO2 Devices



sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The MachXO2-640U, MachXO2-1200/U and larger devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO2 sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1199, [MachXO2 sysCLOCK PLL Design and Usage Guide](#).

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO2 clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.

Figure 2-8. sysMEM Memory Primitives

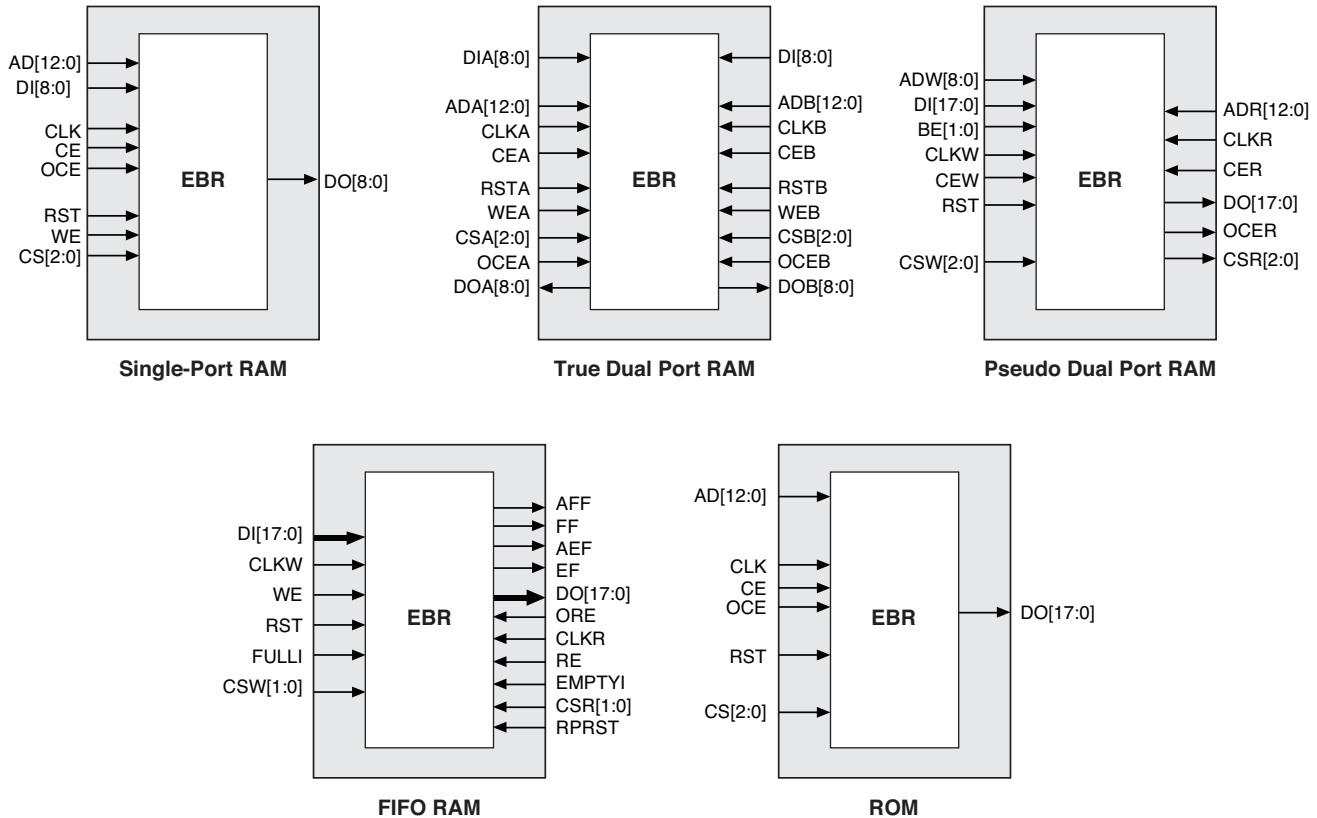


Table 2-6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE ¹	Output Clock Enable	Active High
RST	Reset	Active High
BE ¹	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	—
DI	Data In	—
DO	Data Out	—
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	—
FF	FIFO RAM Full Flag	—
AEF	FIFO RAM Almost Empty Flag	—
EF	FIFO RAM Empty Flag	—
RPRST	FIFO RAM Read Pointer Reset	—

1. Optional signals.

2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.

3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.

4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).

5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

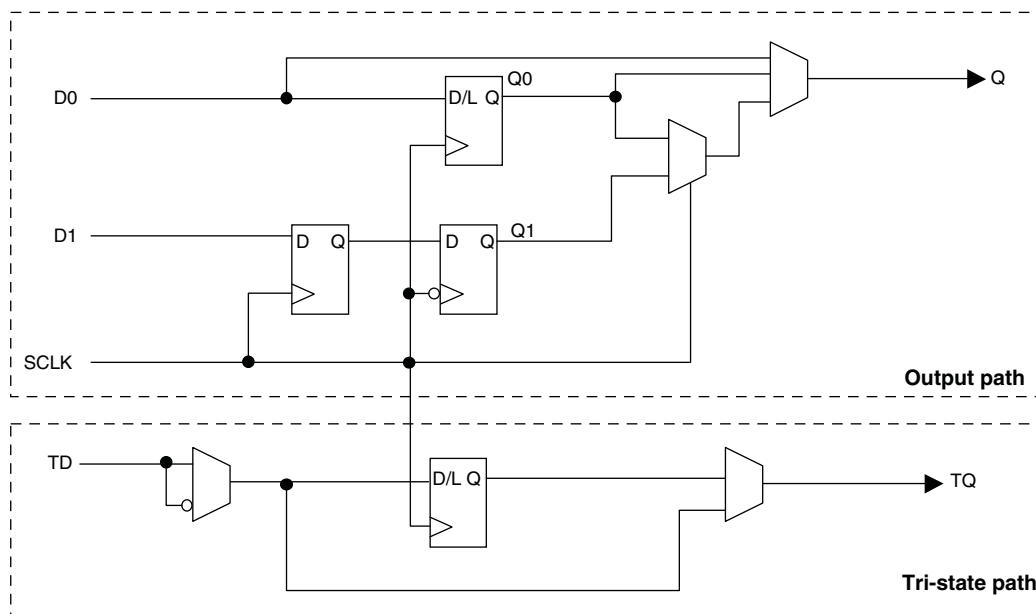
Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-14 shows the output register block on the left, top and bottom edges.

Figure 2-14. MachXO2 Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)



Right Edge

The output register block on the right edge is a superset of the output register on left, top and bottom edges of the device. In addition to supporting SDR and Generic DDR modes, the output register blocks for PIOs on the right edge include additional logic to support DDR-memory interfaces. Operation of this block is similar to that of the output register block on other edges.

In DDR memory mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the DQSW90 signal is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-15 shows the output register block on the right edge.

Table 2-11. I/O Support Device by Device

	MachXO2-256, MachXO2-640	MachXO2-640U, MachXO2-1200	MachXO2-1200U MachXO2-2000/U, MachXO2-4000, MachXO2-7000
Number of I/O Banks	4	4	6
Type of Input Buffers	Single-ended (all I/O banks) Differential Receivers (all I/O banks)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)	Single-ended (all I/O banks) Differential Receivers (all I/O banks) Differential input termination (bottom side)
Types of Output Buffers	Single-ended buffers with complementary outputs (all I/O banks)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)	Single-ended buffers with complementary outputs (all I/O banks) Differential buffers with true LVDS outputs (50% on top side)
Differential Output Emulation Capability	All I/O banks	All I/O banks	All I/O banks
PCI Clamp Support	No	Clamp on bottom side only	Clamp on bottom side only

Table 2-12. Supported Input Standards

Input Standard	VCCIO (Typ.)				
	3.3 V	2.5 V	1.8 V	1.5	1.2 V
Single-Ended Interfaces					
LVTTTL	✓	✓ ²	✓ ²	✓ ²	
LVC MOS33	✓	✓ ²	✓ ²	✓ ²	
LVC MOS25	✓ ²	✓	✓ ²	✓ ²	
LVC MOS18	✓ ²	✓ ²	✓	✓ ²	
LVC MOS15	✓ ²	✓ ²	✓ ²	✓	✓ ²
LVC MOS12	✓ ²	✓ ²	✓ ²	✓ ²	✓
PCI ¹	✓				
SSTL18 (Class I, Class II)	✓	✓	✓		
SSTL25 (Class I, Class II)	✓	✓			
HSTL18 (Class I, Class II)	✓	✓	✓		
Differential Interfaces					
LVDS	✓	✓			
BLVDS, MVDS, LVPECL, RSDS	✓	✓			
MIPI ³	✓	✓			
Differential SSTL18 Class I, II	✓	✓	✓		
Differential SSTL25 Class I, II	✓	✓			
Differential HSTL18 Class I, II	✓	✓	✓		

1. Bottom banks of MachXO2-640U, MachXO2-1200/U and higher density devices only.

2. Reduced functionality. Refer to TN1202, [MachXO2 sysIO Usage Guide](#) for more detail.

3. These interfaces can be emulated with external resistors in all devices.

Figure 2-18. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 Banks

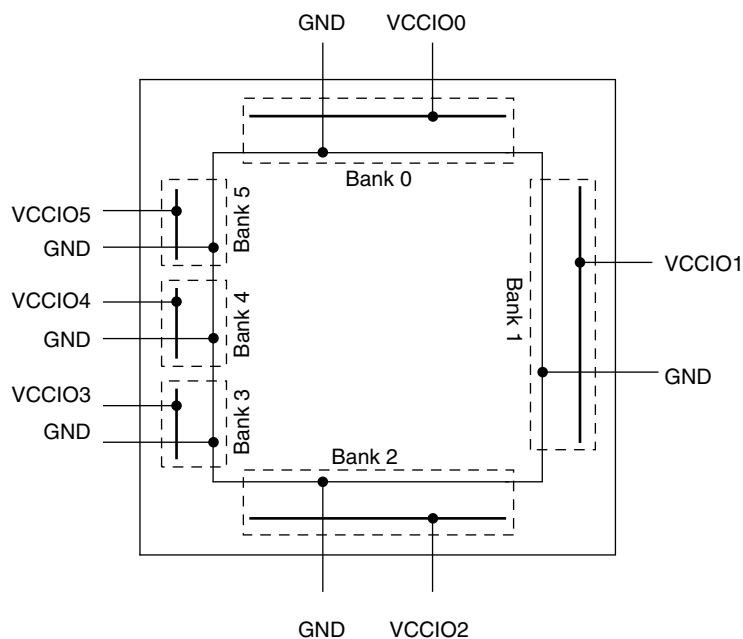


Figure 2-19. MachXO2-256, MachXO2-640/U and MachXO2-1200 Banks

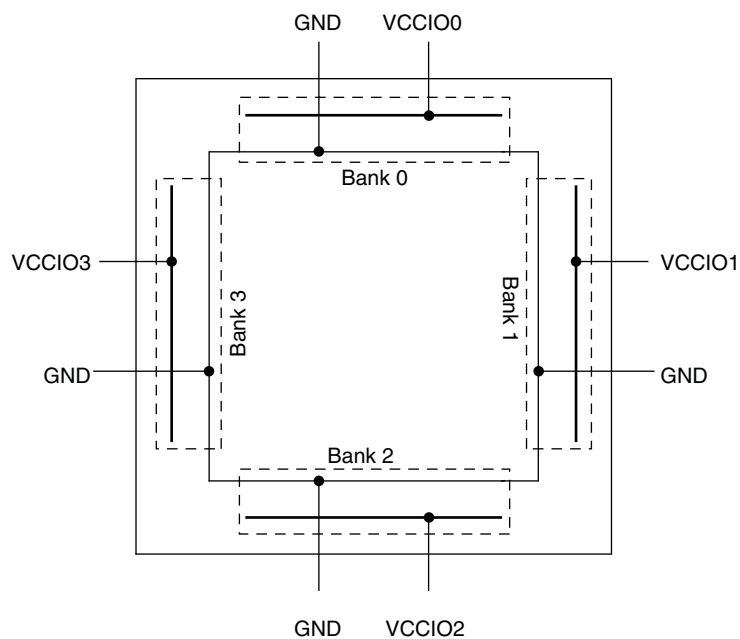
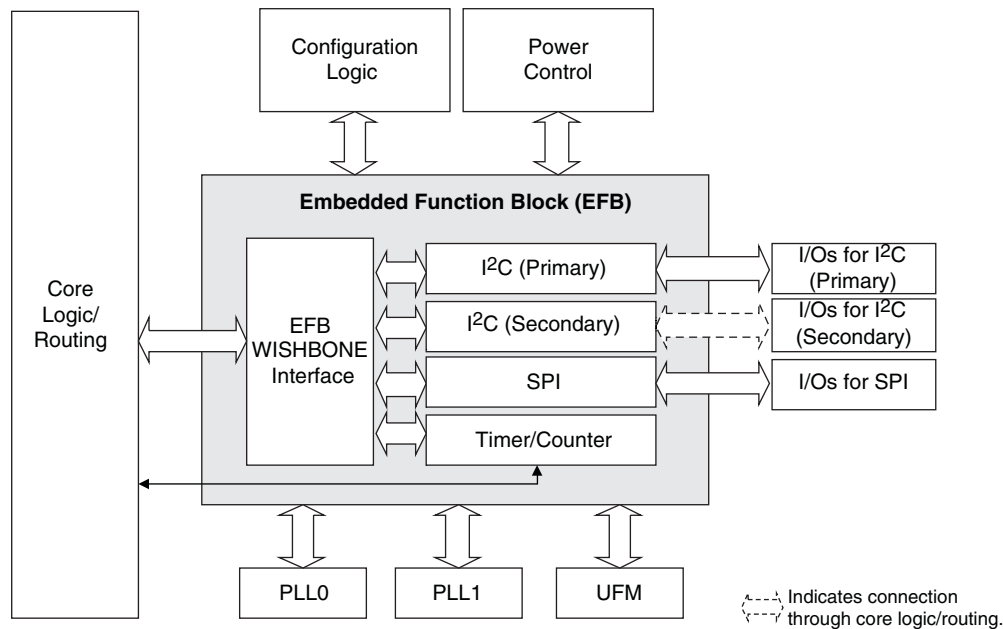


Figure 2-20. Embedded Function Block Interface



Hardened I²C IP Core

Every MachXO2 device contains two I²C IP cores. These are the primary and secondary I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I²C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface

Table 2-18. MachXO2 Power Saving Features Description

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors V _{CC} levels. In the event of unsafe V _{CC} drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1198, [Power Estimation and Management for MachXO2 Devices](#).

Power On Reset

MachXO2 devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the V_{PORUP} level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices), V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators (HC devices), V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time (t_{REFRESH}) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below V_{PORDNBG} level (with the bandgap circuitry switched on) or below V_{PORDNSRAM} level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. V_{PORDNBG} and V_{PORDNSRAM} are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the V_{PORDNSRAM} reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V_{CC} supply dropping below V_{CC} (min) they should not shut down the bandgap or POR circuit.

Typical Building Block Function Performance – ZE Devices¹

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–3 Timing	Units
Basic Functions		
16-bit decoder	13.9	ns
4:1 MUX	10.9	ns
16:1 MUX	12.0	ns

Register-to-Register Performance

Function	–3 Timing	Units
Basic Functions		
16:1 MUX	191	MHz
16-bit adder	134	MHz
16-bit counter	148	MHz
64-bit counter	77	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	90	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	214	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Parameter	Description	Device	-6		-5		-4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-256HC-HE	1.42	—	1.59	—	1.96	—	ns
		MachXO2-640HC-HE	1.41	—	1.58	—	1.96	—	ns
		MachXO2-1200HC-HE	1.63	—	1.79	—	2.17	—	ns
		MachXO2-2000HC-HE	1.61	—	1.76	—	2.13	—	ns
		MachXO2-4000HC-HE	1.66	—	1.81	—	2.19	—	ns
		MachXO2-7000HC-HE	1.53	—	1.67	—	2.03	—	ns
t _{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-256HC-HE	–0.24	—	–0.24	—	–0.24	—	ns
		MachXO2-640HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-1200HC-HE	–0.24	—	–0.24	—	–0.24	—	ns
		MachXO2-2000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000HC-HE	–0.25	—	–0.25	—	–0.25	—	ns
		MachXO2-7000HC-HE	–0.21	—	–0.21	—	–0.21	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices	—	388	—	323	—	269	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)									
t _{COE}	Clock to Output – PIO Output Register	MachXO2-1200HC-HE	—	7.53	—	7.76	—	8.10	ns
		MachXO2-2000HC-HE	—	7.53	—	7.76	—	8.10	ns
		MachXO2-4000HC-HE	—	7.45	—	7.68	—	8.00	ns
		MachXO2-7000HC-HE	—	7.53	—	7.76	—	8.10	ns
t _{SUE}	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
		MachXO2-2000HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
		MachXO2-4000HC-HE	–0.16	—	–0.16	—	–0.16	—	ns
		MachXO2-7000HC-HE	–0.19	—	–0.19	—	–0.19	—	ns
t _{HE}	Clock to Data Hold – PIO Input Register	MachXO2-1200HC-HE	1.97	—	2.24	—	2.52	—	ns
		MachXO2-2000HC-HE	1.97	—	2.24	—	2.52	—	ns
		MachXO2-4000HC-HE	1.89	—	2.16	—	2.43	—	ns
		MachXO2-7000HC-HE	1.97	—	2.24	—	2.52	—	ns
t _{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200HC-HE	1.56	—	1.69	—	2.05	—	ns
		MachXO2-2000HC-HE	1.56	—	1.69	—	2.05	—	ns
		MachXO2-4000HC-HE	1.74	—	1.88	—	2.25	—	ns
		MachXO2-7000HC-HE	1.66	—	1.81	—	2.17	—	ns
t _{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-2000HC-HE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000HC-HE	–0.34	—	–0.34	—	–0.34	—	ns
		MachXO2-7000HC-HE	–0.29	—	–0.29	—	–0.29	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)									
t _{COPLL}	Clock to Output – PIO Output Register	MachXO2-1200HC-HE	—	5.97	—	6.00	—	6.13	ns
		MachXO2-2000HC-HE	—	5.98	—	6.01	—	6.14	ns
		MachXO2-4000HC-HE	—	5.99	—	6.02	—	6.16	ns
		MachXO2-7000HC-HE	—	6.02	—	6.06	—	6.20	ns
t _{SUPLL}	Clock to Data Setup – PIO Input Register	MachXO2-1200HC-HE	0.36	—	0.36	—	0.65	—	ns
		MachXO2-2000HC-HE	0.36	—	0.36	—	0.63	—	ns
		MachXO2-4000HC-HE	0.35	—	0.35	—	0.62	—	ns
		MachXO2-7000HC-HE	0.34	—	0.34	—	0.59	—	ns

Parameter	Description	Device	-6		-5		-4		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR4_RX.ECLK.Aligned ^{9, 12}									
t _{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only. ¹¹	—	0.290	—	0.320	—	0.345	UI
t _{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	0.703	—	UI
f _{DATA}	DDR4 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f _{DDR4}	DDR4 ECLK Frequency		—	378	—	315	—	262	MHz
f _{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR4_RX.ECLK.Centered ^{9, 12}									
t _{SU}	Input Data Setup Before ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only. ¹¹	0.233	—	0.219	—	0.198	—	ns
t _{HO}	Input Data Hold After ECLK		0.287	—	0.287	—	0.344	—	ns
f _{DATA}	DDR4 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f _{DDR4}	DDR4 ECLK Frequency		—	378	—	315	—	262	MHz
f _{SCLK}	SCLK Frequency		—	95	—	79	—	66	MHz
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1) ^{9, 12}									
t _{DVA}	Input Data Valid After ECLK	MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only. ¹¹	—	0.290	—	0.320	—	0.345	UI
t _{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	0.703	—	UI
f _{DATA}	DDR71 Serial Input Data Speed		—	756	—	630	—	524	Mbps
f _{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	262	MHz
f _{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	75	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_TX.SCLK.Aligned ^{9, 12}									
t _{DIA}	Output Data Invalid After CLK Output	All MachXO2 devices, all sides.	—	0.520	—	0.550	—	0.580	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.520	—	0.550	—	0.580	ns
f _{DATA}	DDR1 Output Data Speed		—	300	—	250	—	208	Mbps
f _{DDR1}	DDR1 SCLK frequency		—	150	—	125	—	104	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_TX.SCLK.Centered ^{9, 12}									
t _{DVB}	Output Data Valid Before CLK Output	All MachXO2 devices, all sides.	1.210	—	1.510	—	1.870	—	ns
t _{DVA}	Output Data Valid After CLK Output		1.210	—	1.510	—	1.870	—	ns
f _{DATA}	DDR1 Output Data Speed		—	300	—	250	—	208	Mbps
f _{DDR1}	DDR1 SCLK Frequency (minimum limited by PLL)		—	150	—	125	—	104	MHz
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_TX.ECLK.Aligned ^{9, 12}									
t _{DIA}	Output Data Invalid After CLK Output	MachXO2-640U, MachXO2-1200/U and larger devices, top side only.	—	0.200	—	0.215	—	0.230	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.230	ns
f _{DATA}	DDR2 Serial Output Data Speed		—	664	—	554	—	462	Mbps
f _{DDR2}	DDR2 ECLK frequency		—	332	—	277	—	231	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	—	116	MHz

Parameter	Description	Device	-3		-2		-1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-256ZE	2.62	—	2.91	—	3.14	—	ns
		MachXO2-640ZE	2.56	—	2.85	—	3.08	—	ns
		MachXO2-1200ZE	2.30	—	2.57	—	2.79	—	ns
		MachXO2-2000ZE	2.25	—	2.50	—	2.70	—	ns
		MachXO2-4000ZE	2.39	—	2.60	—	2.76	—	ns
		MachXO2-7000ZE	2.17	—	2.33	—	2.43	—	ns
t _{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-256ZE	–0.44	—	–0.44	—	–0.44	—	ns
		MachXO2-640ZE	–0.43	—	–0.43	—	–0.43	—	ns
		MachXO2-1200ZE	–0.28	—	–0.28	—	–0.28	—	ns
		MachXO2-2000ZE	–0.31	—	–0.31	—	–0.31	—	ns
		MachXO2-4000ZE	–0.34	—	–0.34	—	–0.34	—	ns
		MachXO2-7000ZE	–0.21	—	–0.21	—	–0.21	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO2 devices	—	150	—	125	—	104	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)									
t _{COE}	Clock to Output – PIO Output Register	MachXO2-1200ZE	—	11.10	—	11.51	—	11.91	ns
		MachXO2-2000ZE	—	11.10	—	11.51	—	11.91	ns
		MachXO2-4000ZE	—	10.89	—	11.28	—	11.67	ns
		MachXO2-7000ZE	—	11.10	—	11.51	—	11.91	ns
t _{SUE}	Clock to Data Setup – PIO Input Register	MachXO2-1200ZE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-2000ZE	–0.23	—	–0.23	—	–0.23	—	ns
		MachXO2-4000ZE	–0.15	—	–0.15	—	–0.15	—	ns
		MachXO2-7000ZE	–0.23	—	–0.23	—	–0.23	—	ns
t _{HE}	Clock to Data Hold – PIO Input Register	MachXO2-1200ZE	3.81	—	4.11	—	4.52	—	ns
		MachXO2-2000ZE	3.81	—	4.11	—	4.52	—	ns
		MachXO2-4000ZE	3.60	—	3.89	—	4.28	—	ns
		MachXO2-7000ZE	3.81	—	4.11	—	4.52	—	ns
t _{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	MachXO2-1200ZE	2.78	—	3.11	—	3.40	—	ns
		MachXO2-2000ZE	2.78	—	3.11	—	3.40	—	ns
		MachXO2-4000ZE	3.11	—	3.48	—	3.79	—	ns
		MachXO2-7000ZE	2.94	—	3.30	—	3.60	—	ns
t _{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	MachXO2-1200ZE	–0.29	—	–0.29	—	–0.29	—	ns
		MachXO2-2000ZE	–0.29	—	–0.29	—	–0.29	—	ns
		MachXO2-4000ZE	–0.46	—	–0.46	—	–0.46	—	ns
		MachXO2-7000ZE	–0.37	—	–0.37	—	–0.37	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)									
t _{COPLL}	Clock to Output – PIO Output Register	MachXO2-1200ZE	—	7.95	—	8.07	—	8.19	ns
		MachXO2-2000ZE	—	7.97	—	8.10	—	8.22	ns
		MachXO2-4000ZE	—	7.98	—	8.10	—	8.23	ns
		MachXO2-7000ZE	—	8.02	—	8.14	—	8.26	ns
t _{SUPLL}	Clock to Data Setup – PIO Input Register	MachXO2-1200ZE	0.85	—	0.85	—	0.89	—	ns
		MachXO2-2000ZE	0.84	—	0.84	—	0.86	—	ns
		MachXO2-4000ZE	0.84	—	0.84	—	0.85	—	ns
		MachXO2-7000ZE	0.83	—	0.83	—	0.81	—	ns

sysCLOCK PLL Timing (Continued)

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
$t_{\text{ROTATE_WD}}$	PHASESTEP Pulse Width		4	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1199, [MachXO2 sysCLOCK PLL Design and Usage Guide](#) for more details.
5. At minimum f_{PFD} . As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

	MachXO2-1200					MachXO2-1200U
	100 TQFP	132 csBGA	144 TQFP	25 WLCSP	32 QFN ¹	256 ftBGA
General Purpose I/O per Bank						
Bank 0	18	25	27	11	9	50
Bank 1	21	26	26	0	2	52
Bank 2	20	28	28	7	9	52
Bank 3	20	25	26	0	2	16
Bank 4	0	0	0	0	0	16
Bank 5	0	0	0	0	0	20
Total General Purpose Single Ended I/O	79	104	107	18	22	206
Differential I/O per Bank						
Bank 0	9	13	14	5	4	25
Bank 1	10	13	13	0	1	26
Bank 2	10	14	14	2	4	26
Bank 3	10	12	13	0	1	8
Bank 4	0	0	0	0	0	8
Bank 5	0	0	0	0	0	10
Total General Purpose Differential I/O	39	52	54	7	10	103
Dual Function I/O						
	31	33	33	18	22	33
High-speed Differential I/O						
Bank 0	4	7	7	0	0	14
Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	4	7	7	0	0	14
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	5	7	7	0	2	14
DQS Groups						
Bank 1	1	2	2	0	0	2
VCCIO Pins						
Bank 0	2	3	3	1	2	4
Bank 1	2	3	3	0	1	4
Bank 2	2	3	3	1	2	4
Bank 3	3	3	3	0	1	1
Bank 4	0	0	0	0	0	2
Bank 5	0	0	0	0	0	1
VCC						
	2	4	4	2	2	8
GND						
	8	10	12	2	2	24
NC						
	1	1	8	0	0	1
Reserved for Configuration						
	1	1	1	1	1	1
Total Count of Bonded Pins	100	132	144	25	32	256

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HC-4TG144C	6864	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-5TG144C	6864	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-6TG144C	6864	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-7000HC-4BG256C	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-5BG256C	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-6BG256C	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-7000HC-4FTG256C	6864	2.5 V / 3.3 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-5FTG256C	6864	2.5 V / 3.3 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-6FTG256C	6864	2.5 V / 3.3 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-7000HC-4BG332C	6864	2.5 V / 3.3 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-5BG332C	6864	2.5 V / 3.3 V	–5	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-6BG332C	6864	2.5 V / 3.3 V	–6	Halogen-Free caBGA	332	COM
LCMXO2-7000HC-4FG400C	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-5FG400C	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-6FG400C	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	400	COM
LCMXO2-7000HC-4FG484C	6864	2.5 V / 3.3 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-5FG484C	6864	2.5 V / 3.3 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-7000HC-6FG484C	6864	2.5 V / 3.3 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-1200HC-4TG100CR1 ¹	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-5TG100CR1 ¹	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-6TG100CR1 ¹	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-1200HC-4MG132CR1 ¹	1280	2.5 V / 3.3 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-5MG132CR1 ¹	1280	2.5 V / 3.3 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-6MG132CR1 ¹	1280	2.5 V / 3.3 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-1200HC-4TG144CR1 ¹	1280	2.5 V / 3.3 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-5TG144CR1 ¹	1280	2.5 V / 3.3 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-1200HC-6TG144CR1 ¹	1280	2.5 V / 3.3 V	–6	Halogen-Free TQFP	144	COM

1. Specifications for the “LCMXO2-1200HC-speed package CR1” are the same as the “LCMXO2-1200HC-speed package C” devices respectively, except as specified in the [R1 Device Specifications](#) section of this data sheet.

High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000HE-4TG100C	2112	1.2 V	–4	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-5TG100C	2112	1.2 V	–5	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-6TG100C	2112	1.2 V	–6	Halogen-Free TQFP	100	COM
LCMXO2-2000HE-4TG144C	2112	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-5TG144C	2112	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-6TG144C	2112	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-2000HE-4MG132C	2112	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-5MG132C	2112	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-6MG132C	2112	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-2000HE-4BG256C	2112	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-5BG256C	2112	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-6BG256C	2112	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-2000HE-4FTG256C	2112	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-5FTG256C	2112	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-2000HE-6FTG256C	2112	1.2 V	–6	Halogen-Free ftBGA	256	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-2000UHE-4FG484C	2112	1.2 V	–4	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-5FG484C	2112	1.2 V	–5	Halogen-Free fpBGA	484	COM
LCMXO2-2000UHE-6FG484C	2112	1.2 V	–6	Halogen-Free fpBGA	484	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4TG144C	4320	1.2 V	–4	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-5TG144C	4320	1.2 V	–5	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-6TG144C	4320	1.2 V	–6	Halogen-Free TQFP	144	COM
LCMXO2-4000HE-4MG132C	4320	1.2 V	–4	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-5MG132C	4320	1.2 V	–5	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-6MG132C	4320	1.2 V	–6	Halogen-Free csBGA	132	COM
LCMXO2-4000HE-4BG256C	4320	1.2 V	–4	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4MG184C	4320	1.2 V	–4	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5MG184C	4320	1.2 V	–5	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-6MG184C	4320	1.2 V	–6	Halogen-Free csBGA	184	COM
LCMXO2-4000HE-5BG256C	4320	1.2 V	–5	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-6BG256C	4320	1.2 V	–6	Halogen-Free caBGA	256	COM
LCMXO2-4000HE-4FTG256C	4320	1.2 V	–4	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-5FTG256C	4320	1.2 V	–5	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-6FTG256C	4320	1.2 V	–6	Halogen-Free ftBGA	256	COM
LCMXO2-4000HE-4BG332C	4320	1.2 V	–4	Halogen-Free caBGA	332	COM
LCMXO2-4000HE-5BG332C	4320	1.2 V	–5	Halogen-Free caBGA	332	COM

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-4000HE-4MG132I	4320	1.2 V	–4	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-5MG132I	4320	1.2 V	–5	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-6MG132I	4320	1.2 V	–6	Halogen-Free csBGA	132	IND
LCMXO2-4000HE-4TG144I	4320	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-5TG144I	4320	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-6TG144I	4320	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-4000HE-4MG184I	4320	1.2 V	–4	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-5MG184I	4320	1.2 V	–5	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-6MG184I	4320	1.2 V	–6	Halogen-Free csBGA	184	IND
LCMXO2-4000HE-4BG256I	4320	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-5BG256I	4320	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-6BG256I	4320	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-4000HE-4FTG256I	4320	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-5FTG256I	4320	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-6FTG256I	4320	1.2 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-4000HE-4BG332I	4320	1.2 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-5BG332I	4320	1.2 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-6BG332I	4320	1.2 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-4000HE-4FG484I	4320	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-5FG484I	4320	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-4000HE-6FG484I	4320	1.2 V	–6	Halogen-Free fpBGA	484	IND

Part Number	LUTs	Supply Voltage	Grade	Package	Leads	Temp.
LCMXO2-7000HE-4TG144I	6864	1.2 V	–4	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-5TG144I	6864	1.2 V	–5	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-6TG144I	6864	1.2 V	–6	Halogen-Free TQFP	144	IND
LCMXO2-7000HE-4BG256I	6864	1.2 V	–4	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-5BG256I	6864	1.2 V	–5	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-6BG256I	6864	1.2 V	–6	Halogen-Free caBGA	256	IND
LCMXO2-7000HE-4FTG256I	6864	1.2 V	–4	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-5FTG256I	6864	1.2 V	–5	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-6FTG256I	6864	1.2 V	–6	Halogen-Free ftBGA	256	IND
LCMXO2-7000HE-4BG332I	6864	1.2 V	–4	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-5BG332I	6864	1.2 V	–5	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-6BG332I	6864	1.2 V	–6	Halogen-Free caBGA	332	IND
LCMXO2-7000HE-4FG484I	6864	1.2 V	–4	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-5FG484I	6864	1.2 V	–5	Halogen-Free fpBGA	484	IND
LCMXO2-7000HE-6FG484I	6864	1.2 V	–6	Halogen-Free fpBGA	484	IND

For Further Information

A variety of technical notes for the MachXO2 family are available on the Lattice web site.

- TN1198, [Power Estimation and Management for MachXO2 Devices](#)
- TN1199, [MachXO2 sysCLOCK PLL Design and Usage Guide](#)
- TN1201, [Memory Usage Guide for MachXO2 Devices](#)
- TN1202, [MachXO2 sysIO Usage Guide](#)
- TN1203, [Implementing High-Speed Interfaces with MachXO2 Devices](#)
- TN1204, [MachXO2 Programming and Configuration Usage Guide](#)
- TN1205, [Using User Flash Memory and Hardened Control Functions in MachXO2 Devices](#)
- TN1206, [MachXO2 SRAM CRC Error Detection Usage Guide](#)
- TN1207, [Using TraceID in MachXO2 Devices](#)
- TN1074, [PCB Layout Recommendations for BGA Packages](#)
- TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#)
- AN8086, [Designing for Migration from MachXO2-1200-R1 to Standard \(non-R1\) Devices](#)
- AN8066, [Boundary Scan Testability with Lattice sysIO Capability](#)
- [MachXO2 Device Pinout Files](#)
- [Thermal Management](#) document
- [Lattice design tools](#)

For further information on interface standards, refer to the following web sites:

- JEDEC Standards (LVTTTL, LVCMOS, LVDS, DDR, DDR2, LPDDR): www.jedec.org
- PCI: www.pcisig.com

Date	Version	Section	Change Summary
December 2014	2.9	Introduction	Updated the Features section. Revised Table 1-1, MachXO2 Family Selection Guide. — Removed XO2-4000U data. — Removed 400-ball ftBGA. — Removed 25-ball WLCSP value for XO2-2000U.
		DC and Switching Characteristics	Updated the Recommended Operating Conditions section. Adjusted Max. values for V_{CC} and V_{CCIO} . Updated the sysIO Recommended Operating Conditions section. Adjusted Max. values for LVCMOS 3.3, LVTTTL, PCI, LVDS33 and LVPECL.
		Pinout Information	Updated the Pinout Information Summary section. Removed MachXO2-4000U.
		Ordering Information	Updated the MachXO2 Part Number Description section. Removed BG400 package.
			Updated the High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers. Updated the High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.
November 2014	2.8	Introduction	Updated the Features section. — Revised I/Os under Flexible Logic Architecture. — Revised standby power under Ultra Low Power Devices. — Revise input frequency range under Flexible On-Chip Clocking. Updated Table 1-1, MachXO2 Family Selection Guide. — Added XO2-4000U data. — Removed HE and ZE device options for XO2-4000. — Added 400-ball ftBGA.
			Updated the Pinout Information Summary section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400.
		Ordering Information	Updated the MachXO2 Part Number Description section. Added BG400 package.
			Updated the Ordering Information section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400 part numbers.
		Architecture	Updated the Supported Standards section. Added MIPI information to Table 2-12. Supported Input Standards and Table 2-13. Supported Output Standards.
October 2014	2.7	Ordering Information	Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Fixed typo in LCMXO2-2000ZE-1UWG49ITR part number package.
		DC and Switching Characteristics	Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition. Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition. Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.
		Architecture	Updated the Supported Standards section. Added MIPI information to Table 2-12. Supported Input Standards and Table 2-13. Supported Output Standards.
July 2014	2.6	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics ^{1,2} section. Updated footnote 4. Updated Register-to-Register Performance section. Updated footnote.
			Updated UW49 package to UWG49 in MachXO2 Part Number Description.
		Ordering Information	Updated LCMXO2-2000ZE-1UWG49CTR package in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging.

Date	Version	Section	Change Summary
May 2011	01.3	Multiple	Replaced “SED” with “SRAM CRC Error Detection” throughout the document.
		DC and Switching Characteristics	Added footnote 1 to Program Erase Specifications table.
		Pinout Information	Updated Pin Information Summary tables.
			Signal name SO/SISPISO changed to SO/SPISO in the Signal Descriptions table.
April 2011	01.2	—	Data sheet status changed from Advance to Preliminary.
		Introduction	Updated MachXO2 Family Selection Guide table.
		Architecture	Updated Supported Input Standards table.
			Updated sysMEM Memory Primitives diagram.
			Added differential SSTL and HSTL IO standards.
		DC and Switching Characteristics	Updates following parameters: POR voltage levels, DC electrical characteristics, static supply current for ZE/HE/HC devices, static power consumption contribution of different components – ZE devices, programming and erase Flash supply current.
			Added VREF specifications to sysIO recommended operating conditions.
			Updating timing information based on characterization.
			Added differential SSTL and HSTL IO standards.
		Ordering Information	Added Ordering Part Numbers for R1 devices, and devices in WLCSP packages.
			Added R1 device specifications.
January 2011	01.1	All	Included ultra-high I/O devices.
		DC and Switching Characteristics	Recommended Operating Conditions table – Added footnote 3.
			DC Electrical Characteristics table – Updated data for I_{IL} , I_{IH} , V_{HYST} typical values updated.
			Generic DDRX2 Outputs with Clock and Data Aligned at Pin (GDDR2_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and T_{DIB} .
			Generic DDRX4 Outputs with Clock and Data Aligned at Pin (GDDR4_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for T_{DIA} and T_{DIB} .
			Power-On-Reset Voltage Levels table - clarified note 3.
			Clarified VCCIO related recommended operating conditions specifications.
			Added power supply ramp rate requirements.
			Added Power Supply Ramp Rates table.
			Updated Programming/Erase Specifications table.
			Removed references to V_{CCP} .
		Pinout Information	Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.
			Removed references to V_{CCP} .
November 2010	01.0	—	Initial release.